

ELIMINATION OF LEAKAGE CURRENT IN SINGLE PHASE GRID TIED INVERTER WITH PN-NPC TOPOLOGY

¹ K Nauhida Tabassum, ² A Mahesh Kumar Reddy, ³ V Vishnu Vardhan,

¹M.Tech Student, Department of EEE, Sri Sai Institute of Technology and Science
JNTUA University, Anantapuram, AP, India₁

²Assistant professor, Department of EEE, Sri Sai Institute Of Technology And Science
JNTUA University, Anantapur, AP, India₂

³Assistant professor, Department of EEE, Sri Sai Institute Of Technology And Science
JNTUA University, Anantapur, AP, India₂

Abstract— In this paper, a family of NPC switching cells are proposed for the mitigation of leakage current in transformerless PV grid connected inverters. Due to the characteristics of low cost, smaller size and higher efficiency the transformerless PV grid connected inverters have attracted more attention in the application of solar electric generation system. However, the leakage current through the parasitic capacitors and the utility grid is harmful. Neutral point clamped (NPC) topology is an effective way to eliminate the leakage current. In this paper, two types of basic switching cells, the positive and the negative neutral point clamped cell are developed to build NPC topologies, with the systematic method of topology generation given. The basic modes of operation of NPC switching cells are analyzed along with the existing OH5 and other topologies. The performance of proposed topologies is confirmed through simulation investigations.

Index Terms— Common-mode voltage, grid-tied inverter, leakage current, neutral point clamped inverter, photovoltaic (PV) generation system.

I. INTRODUCTION

Solar photovoltaic's power generation has long been seen as a clean energy technology which draws upon the planet's most plentiful and widely distributed renewable energy source. But, the initial investment and generation cost of solar PV generation system is still too high compared with other renewable energy sources thus, the efficiency improvement of grid tied PV inverters is a significant effort to shorten the payback time and gain the economic benefits faster. Transformerless grid tied PV inverters, such as full

bridge topology have many advantages e.g., higher efficiency, lower cost, smaller size, and weight. However, the common mode voltage of VAN and VBN may induce a leakage current flowing through the loop. In an isolated topology, the loop for the leakage current is broken by the transformer, and the leakage current is very low. But in a transformerless topology, the leakage current may be too high to induce serious safety and radiated interference issues. Therefore, the leakage current must be limited within a reasonable margin.

The instantaneous common-mode voltage V_{CM} in the full bridge topology shown in Fig. 1 is represented as follows,

$$V_{CM} = 0.5(v_{AN} + v_{BN}) \quad (1)$$

Where v_{AN} and v_{BN} are voltages from mid-point A and B of the bridge leg to terminal N, respectively.

In order to eliminate the leakage current, the common-mode voltage V_{CM} must be kept constant during all operation modes and many solutions have been proposed as follows:

1) Bipolar sinusoidal pulse width modulated (SPWM) full bridge type inverter topologies:

The leakage current characteristic of this topology is excellent because, the common mode voltage of this inverter is kept constant during all operating modes. But, switching losses are large and the current ripples across the filter inductors are large.

2) Improved unipolar SPWM full-bridge inverters:

The unipolar SPWM full bridge inverters are attractive for its excellent differential modes characteristics such as higher dc voltage utilization, smaller inductor current ripple and higher power efficiency. In active modes, the V_{cm} is equal to $0.5U_{pv}$, in freewheeling modes V_{cm} is equal to U_{pv} or zero depending on the leg midpoint connected to the positive or negative terminal of the input. So, the V_{cm} of this inverter varies at switching frequency which leads to high leakage current.

By providing the new freewheeling paths in order to separate the PV array from the utility grid in the freewheeling modes the problems arise in above

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K.Nauhida Tabassum, M.Tech(PE), EEE(dept), SSITS, JNTUA University, Rayachoty, India, 8142737768,
A. Mahesh Kumar(Assist. Professor),dept of EEE JNTUA University Rayachoty, India, 9032214393.
V.Vardhan Vardhan (Assit professor), dept of EEE, JNTUA University. Rayachoty, India, 9441695364.

topologies will be solve .with the HERIC topology the problem of above topologies can be solve .in the freewheeling modes of HERIC inverter ,the inductor current flowing through S5 and S6;thus the PV array is disconnected from the utility grid .Although ,these topologies proposed earlier feature the simple circuit structure ,the common mode voltage depends on both of the parasitic parameters of the leakage current loop and the voltage amplitude of the utility grid which is not good for the leakage current reduction.

II. NEUTRAL POINT CLAMPED CELLS

A. IDEA OF THE NPCC

Thus, from the above analysis, there are some principles with which the leakage current can be reduce, those are 1) disconnection of PV array from the utility grid with the help of the power switch during the freewheeling path.2) After disconnecting from the utility grid the common mode voltage has to maintain to half of the input voltage, with the other power switch.

Thus, two power switches are required to reduce the leakage current, those are basic NPC switching cells which are shown in the figure 1. The two switches are P-NPCC and N-NPCC, these two switching cells contains three terminals (P+) or (P-), (N+) or (N-), and (O1) or (O2). In order to build a full bridge NPC inverter topology using above cells the following rules has to be followed .

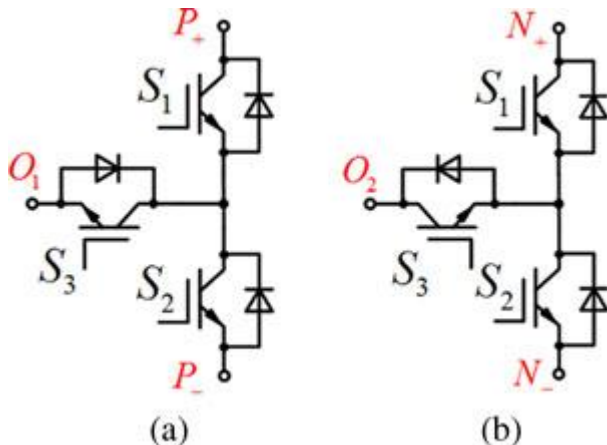


Fig.1. Two basic NPC switching cells. (a) P-NPCC. (b) N-NPCC

Rule 1: Midpoint terminals (O1) and (O2) has to be connected to the neutral point of the input split capacitors and the voltage across the O1, O2 is $V_{(O1)} = v_{(O2)} = 0.5U_{PV}$. Where U_{PV} is the voltage of PV array.

Rule 2: The P-NPCC has its (P+) and (P-) to be connected to the positive terminal of PV array and output filter inductor, respectively. On the other hand, the N-NPCC has its (N-) and (N+) to be connected to the negative terminal of PV array and output filter inductor, respectively.

Rule 3: Since, we need three switches to separate the grid from the PV array and still to maintain the inductor current a

loop during freewheeling mode. So, at least one NPCC should appear in each phase leg.

B. MODELING OF PROPOSED TOPOLOGY

Fig. 2. represents the universal topological structure of a single phase transformerless full bridge inverter, where upper and lower terms of A and B phases "AU", "AD", "BU", "BD", are four leg switch modules of the full bridge inverter, respectively .

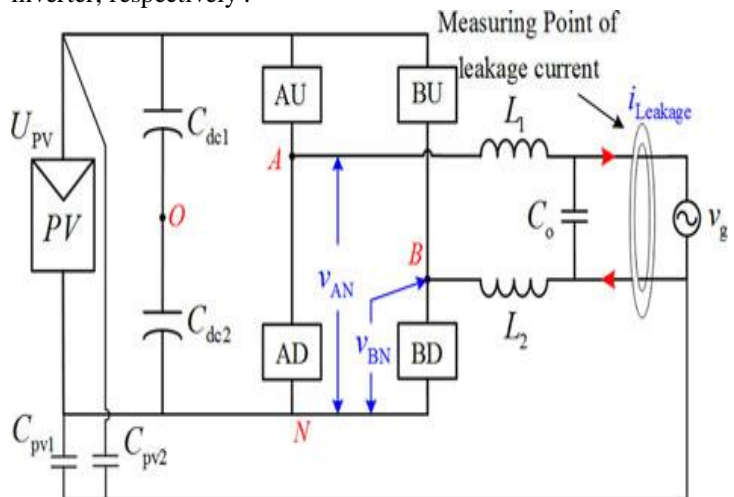


Fig.2. Topology structure of single-phase transformerless full bridge inverter.

Full bridge inverter topology of single phase PV grid employs single power switch in each of a switch module. Instead of this if there is only one P-NPCC or N-NPCC employed in the inverter ,the PV array from the utility grid during the freewheeling period cannot be disconnect through which leakage current cannot be tackled . Therefore, two NPCC'S should be employed in phase-A and phase-B, respectively. The rest still employ the original power switches. As a result, a family of novel single phase transformerless full bridge NPC inverters is generated as shown in the fig. 3.

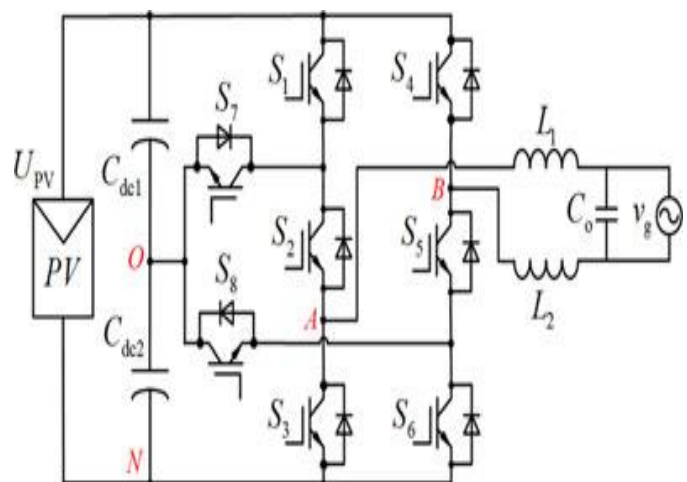


Fig.3. Topology of the proposed PN-NPC. Modes of operations

III. MODES OF OPERATIONS:

Usually, grid tied solar PV systems operate with unity power factor. The gate drive signals for the proposed topology are shown in the fig.4.

In Fig.4. Vr is the output signal of inductor current regulator can also be named as modulation signal. The gate drive signal of the power switches S1-S8 are represented by the Vgs1 to Vgs8 respectively.

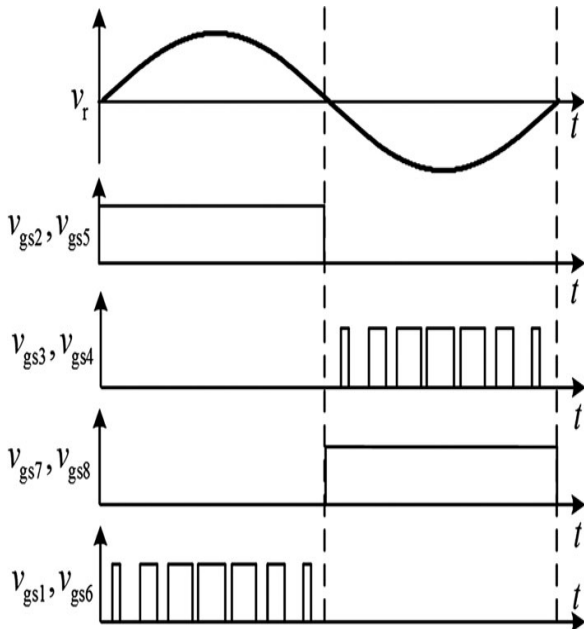


Fig.4. Schematic of gate drive signals with unity Power Factor.

The operation principle contains four operation modes in each period of utility grid as shown in fig.5. where, V_{AN} is the voltage between terminal A and N, and V_{BN} is the voltage between terminal B and terminal N, and V_{AB} is the differential mode voltage of the topology V_{AB}=V_{AN}-V_{BN}.

1) **MODE-I** is the active mode in the positive half period of the utility grid as shown in the fig.5.a. in this mode the turn ON switches are s1, s2, s5 and s6 and remaining switches are turned off. the voltage across the phase A and B are V_{AN}=U_{PV} and V_{BN}=0 thus V_{AB}=U_{PV}, and the common mode voltage is V_{CM}=(V_{AN}+V_{BN})/2=0.5U_{PV}.

2) **MODE-II** is the freewheeling mode in the positive half period of the utility grid as shown in fig.5.b. the activating switches in this mode are s2 and s5, the other remaining switches are turned off. the inductor current flows through the anti parallel diode of s7 and s8. Therefore, the voltage across the phase A and B are V_{AN}=0.5U_{PV} and V_{BN}=0.5U_{PV}, thus V_{AB}=0, and the common mode voltage V_{CM}=(V_{AN}+V_{BN})/2=0.5U_{PV}.

3) **MODE-III** is the active mode in the negative half period of the utility grid, as shown in fig.5.c. the turn ON switches are s3, s4, s7 and s8 and the other switches are turned off. Even though the s7 and s8 are turned ON, there is no inductor current flowing through these two switches. the voltage across the phases are V_{AN}=0, V_{BN}=U_{PV}, thus,

V_{AB}=-U_{PV}, and the common mode voltage V_{CM}=(V_{AN}+V_{BN})/2=0.5U_{PV}.

4) **MODE-IV** is the freewheeling mode in the negative half period of the utility grid as shown in fig.5.d. The turned on switches are s7 and s8 and the other switches are turned OFF. The inductor current flows through the anti parallel diode of s2 and s5 and the voltage across the phase A and B are V_{AN}=0.5U_{PV}, V_{BN}=0.5U_{PV}, thus, V_{AB}=0 and the common mode voltage V_{CM}=(V_{AN}+V_{BN})/2=0.5U_{PV}.

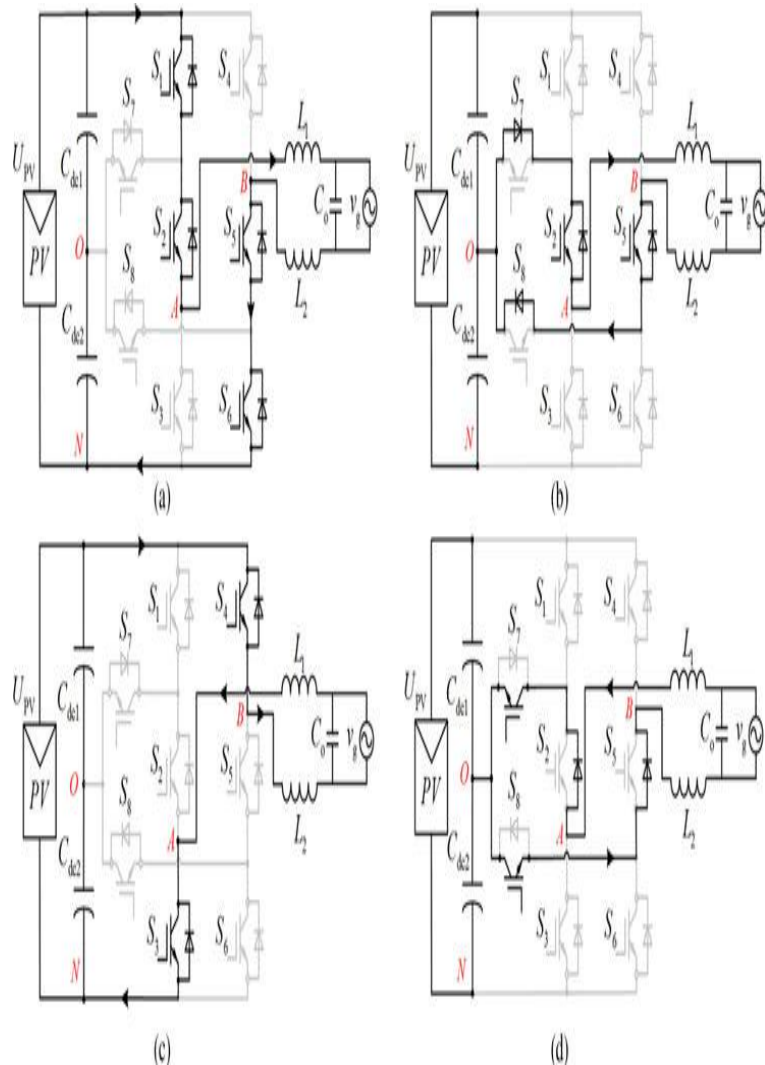


Fig.5. Equivalent circuits of operation modes (a) Active mode in the positive half period. (b) Freewheeling mode in the positive half period. (c) Active mode in the negative half period. (d) Freewheeling mode in the negative half period.

Based on the above analysis, the common-mode voltage V_{CM} of the proposed topology in each operation mode is unchanged, and equals to 0.5U_{PV}. Thus, the requirement for eliminating Leakage current is fulfilled. Furthermore, the leakage current characteristic of this topology only depends on the turn-on speed of the antiparallel diodes of S2, S5, S7 and S8.

IV. SIMULATION MODEL AND RESULTS

A) simulation model

A universal prototype of the NPC simulation topology model has been build up in order to verify the operation principle is shown in the below figure.6.the

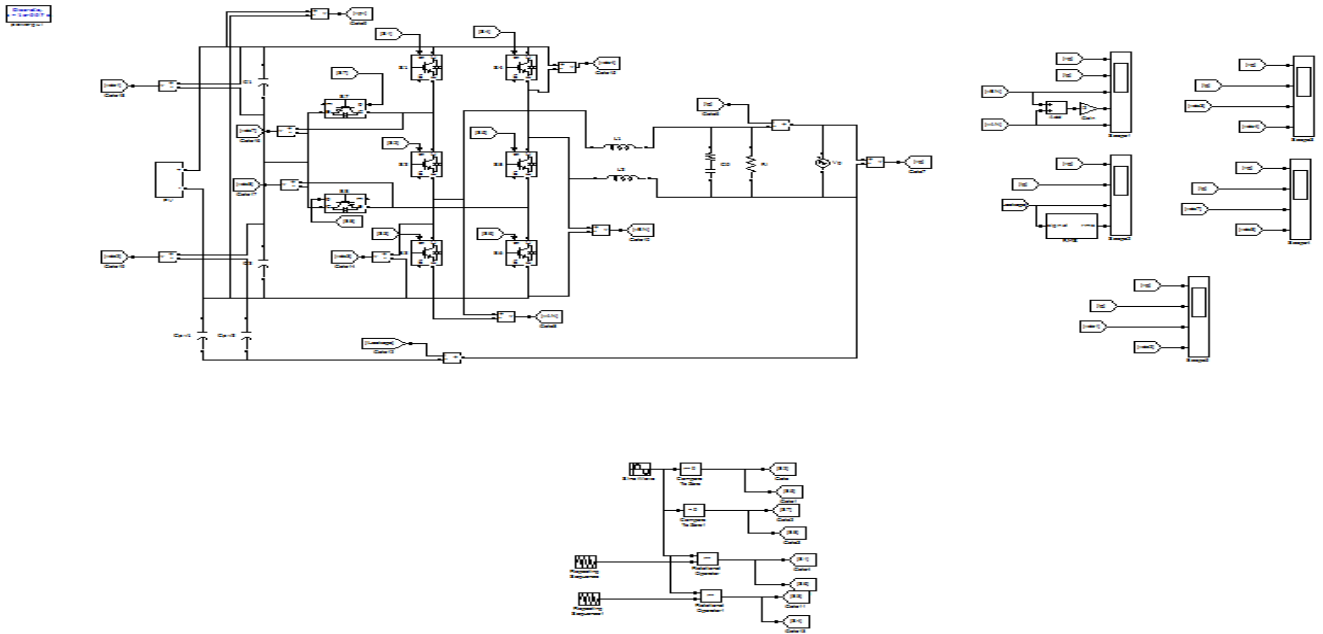


Fig.6.Simulation Model

B) Simulation model with LC filter

A low pass LC filter is required at the output terminal of Full Bridge VSI to reduce harmonics generated by the pulsating modulation waveform. While designing L-C filter, the cut-off frequency is chosen such that most of the low order harmonics is eliminated. To operate as an ideal voltage source, that means no additional voltage distortion even though under the load variation or a nonlinear load, the output impedance of the inverter must be kept zero. Therefore, the capacitance value should be maximized and the inductance value should be minimized at the selected cut-off frequency of the low-pass filter.

Each value of L and C component is determined to minimize the reactive power in these components because the reactive power of L and C will decide the cost of LC filter and it is selected to minimize the cost, then it is common that the filter components are determined at the set of a small capacitance and a large inductance and consequently the output impedance of the inverter is so high. With these design values, the voltage waveform of the inverter output can be sinusoidal under the linear load or steady state condition because the output impedance is zero. But in case of a step change of the load or a nonlinear load, the output voltage waveform will be distorted cause by the slow system response as the output response is non-zero. Figure 7 shows the simulation model of the single phase PWM-VSI with any linear or nonlinear load. The load current flows differently depending on the kind of loads such as linear and nonlinear load.

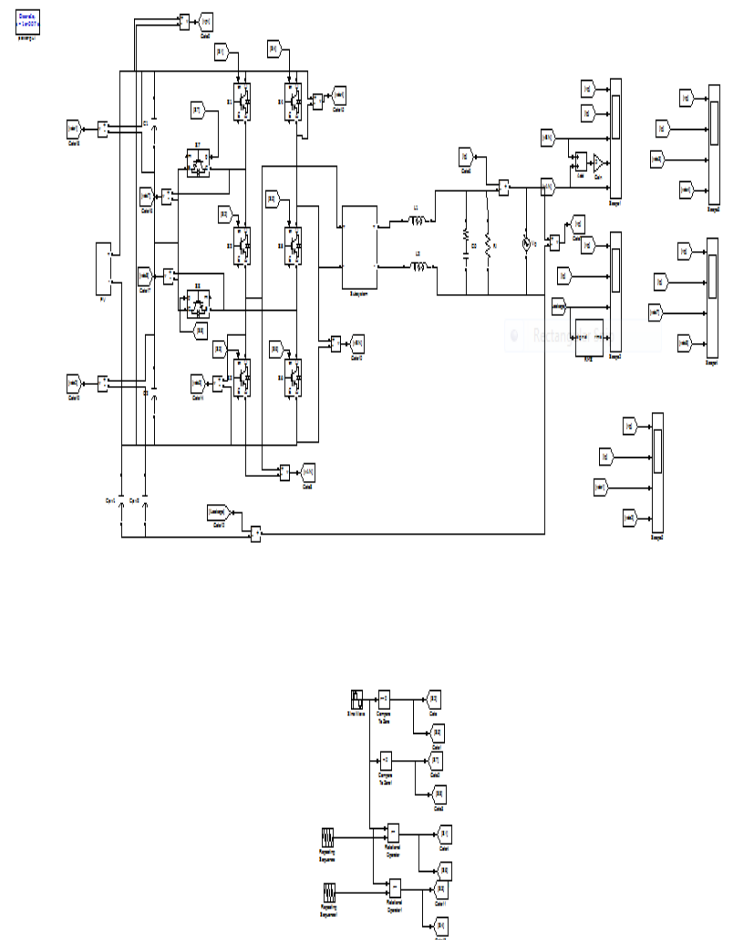


Fig.7.Simulation Model with LC Filter

specifications of the NPC inverter topologies are listed in Table I. control circuit is implemented based on a DSP chip TMS320F280.

TABLE I: PARAMETERS OF THE EXPERIMENTAL PROTOTYPE

| Parameter | Value |
|---|-------------|
| Rate power | 1000 W |
| Input voltage | 380~700 V |
| Switching frequency | 20kHz |
| Filter inductor L_1, L_2 | 3mH |
| Filter Capacitor | 0.47uF |
| Grid voltage/frequency | 230V/50Hz |
| 1200V IGBT | IRG4PH40U |
| 600V IGBT | SGH40N60UFD |
| 1000V Diode | MUR8100T |
| PV parasitic capacitor C_{PV1}, C_{PV2} | 0.1uF |

B. SIMULATION RESULTS

Based on the above analysis, the common-mode voltage V_{CM} of the proposed topology in each operation mode is unchanged, and equals to $0.5UPV$. Thus, the requirement for eliminating Leakage current mentioned is fulfilled. Furthermore, the leakage current characteristic of this topology only depends on the turn-on speed of the antiparallel diodes of $S2, S5, S7$ and $S8$.

It can be seen that the power losses in PN-NPC inverter is much lower than that in existing topology because the voltage rating of some switches in PN-NPC topology are 600 V, half of that in FB-DCBP. The power loss in PN-NPC inverter is similar which with the least number of power devices are required. However, PN-NPC inverter features lower leakage current.

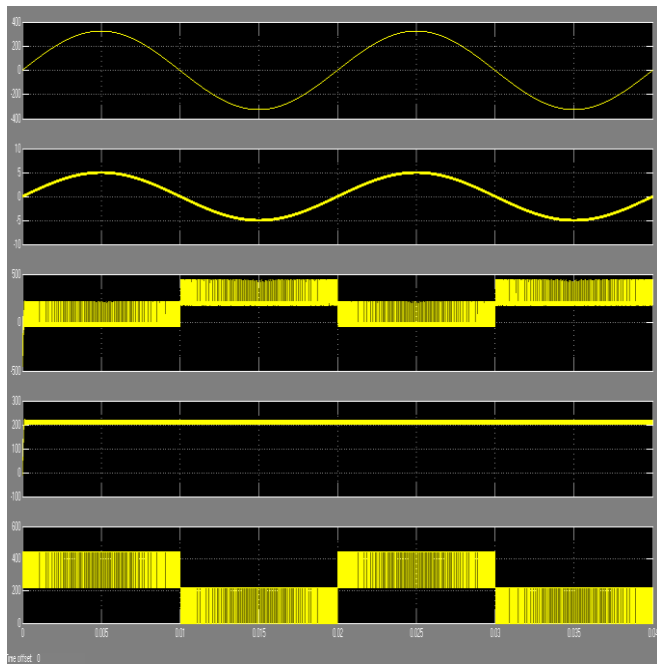


Fig.8.a. Common-mode voltage in PN-NPC topology.

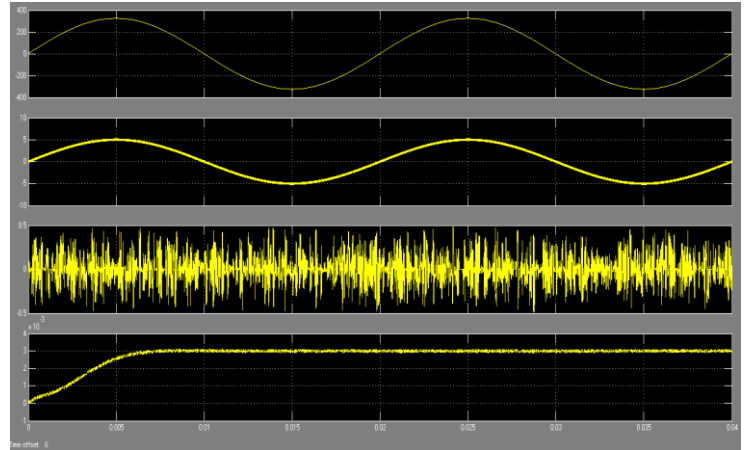


Fig.8.b. leakage current in PN-NPC topology.

A Universal prototype of the NPC topologies has been built up in order to verify the operation principle. The measure point of leakage current is shown in Fig.2.

The common mode voltage and leakage current waveforms of NPC topologies in unified experimental conditions are shown in Fig .8.a and b. and the drain source voltage in PN-NPC topology with voltage stress on the switches $S3, S4, S7$ and $S8$ are shown in Fig.9.a and b. respectively.

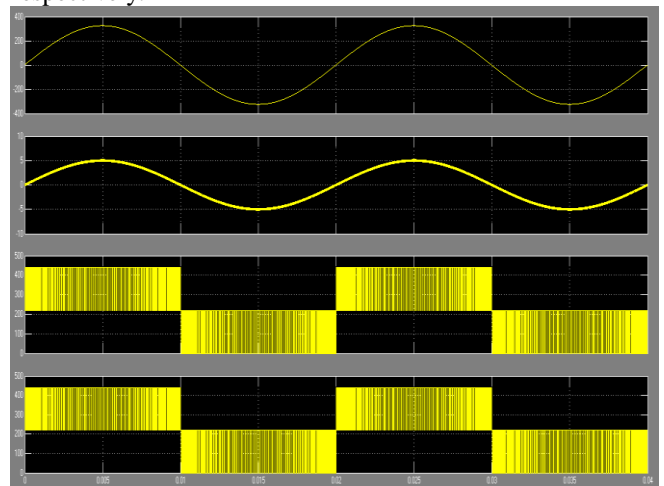


Fig.9.a. Drain-source voltages in PN-NPC topology. (a) Voltage stress on $S3$ and $S4$.

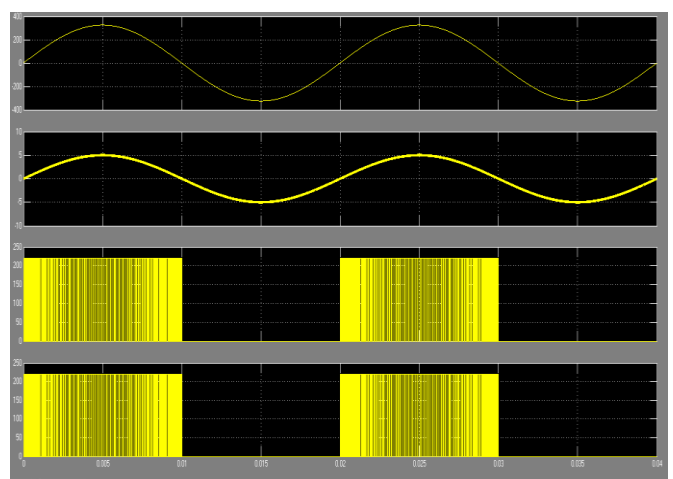


Fig.9.b. Voltage stress on $S7$ and $S8$.

V. CONCLUSION

In this paper, the basic universal structure and operating characteristics of a single phase transformerless full bridge NPC inverter topologies with low leakage current based on the basic switching cells have been described by taking a PN-NPC configuration. The PN-NPC has been illustrating in simulation results by using MATLAB. Suppression of leakage can be obtained by clamping the common mode voltage to a constant level and the excellent differential mode characteristics are achieved. Reactive power injection capability is the major advantage of future PV inverters Applications and extensions.

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FIRST AUTHOR DETAILS:

K .Nauhida Tabassum currently pursuing M.Tech in POWER ELECTRONICS from SRI SAI INSTITUTE OF TECHNOLOGY AND SCIENCE affiliated JNTUA. She has done her B.Tech degree from SRI SAI INSTITUTE OF TECHNOLOGY AND SCIENCE affiliated JNTUA in 2013 and her field of interest includes POWER ELECTRONICS.

SECOND AUTHOR DETAILS:

A. Mahesh Kumar Reddy has completed his B.E electrical and electronics engineering from saphthagiri college of engineering and science affiliated to the university of madras. M.Tech in instrumentation and control system from JNTUK Kakinada in 2008 .,working as assistant professor in sri sai institute of technology and science, Rayachoty, Andhra Pradesh ,India. His areas of interest includes CONTROL SYSTEMS, ADVANCED CONTROL SYSTEMS.

THIRD AUTHOR DETAILS:

V.Vishnu Vardhan has completed his B.Tech ELECTRICAL&ELECTRONICS ENGINEERING in 2010 from audisankara college of engineering and technology affiliated JNTUA, M.Tech in power electronics(2014) in PBR vishvodaya institute of technology and science, kavali, affiliated JNTUA, and ,working as a Assist. Professor of EEE department, SRI SAI INSTITUTE OF TECHNOLOGY AND SCIENCE affiliated JNTUA .Rayachoty, kadapa(dist).Andhra Pradesh, INDIA. His areas of interest includes Power Electronics and Drives.