SIMULATION OF A CASCADED H BRIDGE MULTI LEVEL INVERTER FOR PHOTOVOLTAIC APPLICATION

Sheelu Pandey, Durga Sharma, Dr. Dharmendra Singh

Abstract: In this paper two level, three level, five level and seven level multi level inverter is being simulated to apply on the photo voltaic applications. The photovoltaic source is assumed to have a constant voltage supply and it is being connected to the load via the multi level inverter and power quality is being monitored. The total harmonic distortion of the output voltage and output current of all inverter is being compared and the voltage and current burden of each switch in each inverter is being illustrated. The simulation result shows that as the number of levels in inverter is increased the voltage and current burden on switch decreases and also the power quality of the inverter is improved.

Index terms: Current harmonics, multi level inverter, photovoltaic, voltage harmonics, voltage burden.

Introduction: Due to the energy shortage, the integration of renewable energy sources to the electricity grid becomes interesting research topic nowadays. The number of renewable energy sources and distributed generators is increasing very fast which also brings some threats to the power grid. In order to maintain or even to improve the power supply reliability and quality of the power system with distributed generation, it is necessary to have some new strategies for the operation and management of the electricity grid. SOLAR ENERGY is one of the favorable renewable energy resources, and the multilevel inverter has been proven to be one of the important enabling technologies in photovoltaic (PV) utilization. Multilevel voltage-source inverters offer several advantages compared with their conventional counterparts. By synthesizing the ac output terminal voltage from several levels of voltages, staircase waveforms can be produced, which approach the sinusoidal waveform with low harmonic distortion, thus reducing filter requirements. The need of several sources on the dc side of the converter makes multilevel technology attractive for PV applications [1]. While the multilevel inverter requires more components than conventional two-level inverters, lower voltage-rated devices can be used, and the multilevel inverter offers advantages such as the possibility of lower switching frequency (which leads to higher efficiency) and lower electromagnetic interference (EMI).

Several configurations and new trends of PV power conditioning systems, employing various static converter topologies, can be found in technical literature [2], [3]. Cascaded multilevel inverter with separate dc source is proposed in this paper for supplying the load with the solar PV panel. It is assumed that with a proper maximum power point algorithm the output of the PV array is a constant DC source and simulation is being carried out for 2 level , 3 level, 5 level and 7 level multilevel inverter and the results are being compared. The multilevel inverters requires too many semiconductor switches and thus its cost gets increased and thus the use of multilevel inverters are justified by showing the voltage and current burden on each switch and thus it is showed that in spite of the increased number of switches there will not be much cost difference as the burden on switches gets reduced low rating semiconductor devices can be used to implement the module. Also the control strategy is very much simple there will not be much cost difference. Also it is shown that voltage and current total harmonic distortion gets reduced on increasing the number of levels in a multilevel inverter.

Two level inverter

Figure 1 shows a single phase h bridge inverter having 4 switches . generally an IGBT is used as a switch in an inverter. It is seen that an R-L load is being connected between the two leg of the inverter. A conventional two level inverter uses the two voltage levels at the output of the inverter they are the +V volt and –V volt. For output to be +V volt switch S1 and S2 are closed together and S3 and S4 are kept open. To obtain –V volt at the output S3 and S4 are closed together and S1 and S2 are kept open. The switching table of a Two level inverter is shown in table 1. The output waveform of a two level inverter is shown in figure 2.

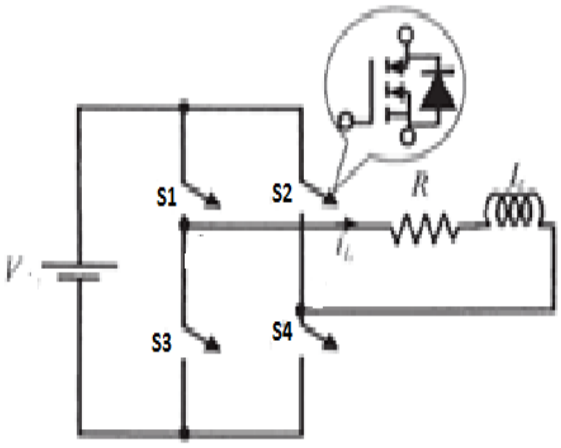

Fig 1 A single phase h bridge inverter

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Voltage level	S1	S2	S3	S4
+V	1	0	0	1
-V	0	1	1	0

Table 1 Switching Table of Two Level H Bridge Inverter

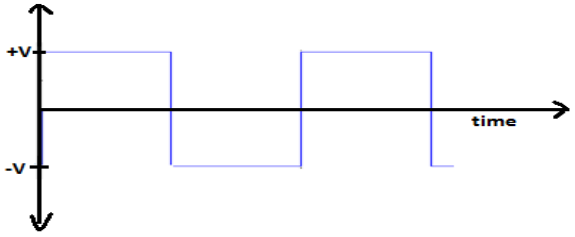

Fig 2 Output Waveform of a Two Level Inverter

Three level inverter

By manipulating the switching signals of the h bridge inverter of figure 1 three level inverter can be obtained. A three level inverter has three level of voltage at the output side namely 0 volt level, +V volt level and –V volt level. The switching table of a three level inverter is shown in table 2. The output voltage waveform of a three level inverter is shown in figure 3.

Voltage level	S1	S2	S3	S4
0	0	0	1	1
+V	1	0	1	0
-V	0	1	1	0

Table 2 Switching Table of a Three Level Inverter

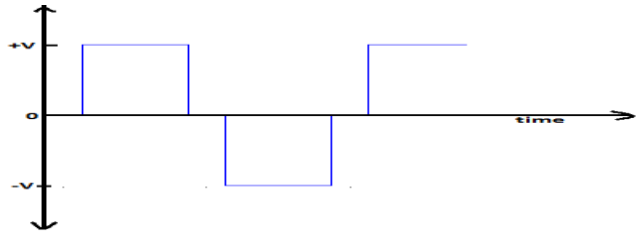

Fig 3 Output Waveform of a Three Level Inverter

Five level inverter

Figure 4 represents the circuit diagram of a five level inverter. It requires two cascaded connecter h level bridge having eight switches. The output voltage levels are 0 volt, +V/2 volt, -V/2 volt, +V volt and –V volts. The switching sequence to obtain 0 , +V/2, -V/2, +V and –V is shown in the table 3. The output waveform of a five level inverter is as shown in the figure 5.

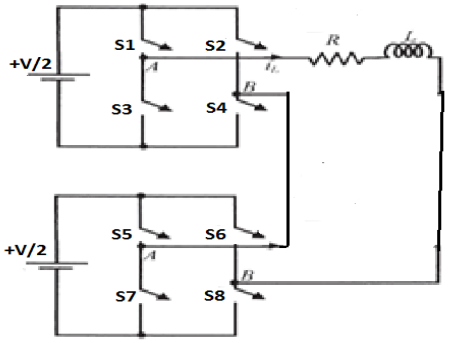

Fig 4 Circuit Diagram of a Five Level Inverter

Voltage	S1	S2	S3	S4	S5	S6	S7	S8
0	0	0	1	1	0	0	1	1
+V/2	1	0	0	1	0	0	1	1
-V/2	0	1	1	0	0	0	1	1
+V	1	0	0	1	1	0	0	1
-V	0	1	1	0	0	1	1	0

Table 3 Switching Table of five Level Inverter

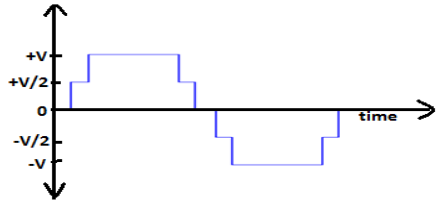

Fig 5 Waveform of a 5 Level Inverter

Seven Level Inverter

Figure 6 represents the cicuit diagram of a 7 level inverter. It requires three dc voltage source and 12 switches. The voltage levels of a 7 level inverter are 0, V/3, 2V/3,V,-V/3,-2V/3 and –V volts. On proper switching these voltage levels at different instant of time is obtained to obtain the nearly sinusoidal signals. The switching sequence to obtain the desired voltage levels is shown in table 4. The output waveform of the 7 level inverter is shown in figure 7.

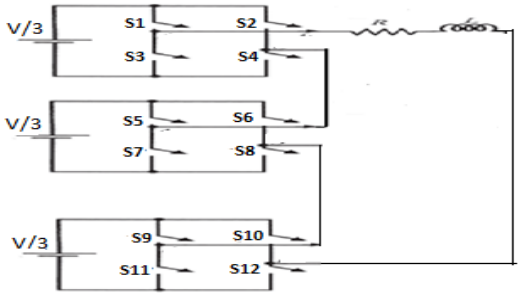

Fig 6 Circuit Diagram of a 7 Level Inverter

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Volt	S 1	S 2	S 3	S 4	S 5	S 6	S 7	S 8	S 9	S1 0	S1 1	S1 2
0	0	0	1	1	0	0	1	1	0	0	1	1
+V/ 3	1	0	0	1	0	0	1	1	0	0	1	1
-V/3	0	1	1	0	0	0	1	1	0	0	1	1
+2V /3	1	0	0	1	1	0	0	1	0	0	1	1
- 2V/ 3	0	1	0	0	0	1	1	0	0	0	1	1
+V	1	0	0	1	1	0	0	1	1	0	0	1
-V	0	1	1	0	0	1	1	0	0	1	1	0

Table 4 Switching Table of a Seven Level Inverter

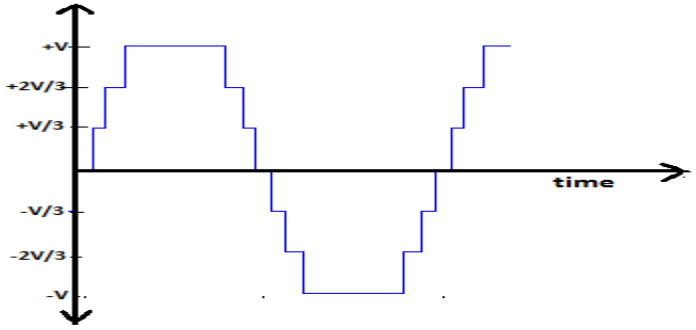

Fig 7 waveform of a 7 level inverter

Control structure

An open loop control structure using Fibonacci series control signal is being implemented in this paper. A sinusoidal signal is compared with a constant value whose value is determined using the Fibonacci series. From the switching tables it is seen that the switch in the lower limb is having gate signal such that it is complement of the upper limb gate signal for example gate signal of S3 which is the lower part of S1 is not of gate signal of S1. Now to obtain the desired signal a sinusoidal signal whose frequency is equal to 50 Hz is being compared to a constant value signal and gate signal is being generated.

Let the sine wale signal which is being compared with a constant value signal be denoted by F.

For a two pulse inverter there is only one constant value signal whose value is 0. If F is greater than 0 then switch S1 is ON.

If F is lesser than 0 then switch S2 is ON. The gate signals given to S3 and S4 are inverter gate signals of S1 and S2 respectively.

For a 3 level inverter the only difference is that S1 is ON when F is greater than 2 and S2 is on when F is lesser than -2.

For a five level inverter there are 4 more switches. The switching of S1 and S2 are similar to that of a three level inverter. Switch S5 is ON when F is greater than 5 and switch S6 is on when F is lesser than -5. Switch S7 and S8 are the inverted signals of S5 and S6 respectively.

For a seven level inverter S9 is On when f is greater than 9 and S10 is ON when F is lesser than -9. Switches S11 and S12 gets the gate signal of inverted values of S9 and S10 respectively.

Thus with the increase of each bridge the sinusoidal signal F is compared with the constant value which is obtained by Fibonacci series starting with 2. Such as 2,5,9,14,……. The amplitude of the sinusoidal signal has to be kept in such a manner that it should be the next number in Fibonacci series after the largest constant value of the constant signal used for controlling. For example the amplitude of F for 2,3,5 and 7 level must be 2,5,9, 14 respectively.

Simulation diagram and result

Simulation of inverter having different voltage levels are being done is a mat lab simulink using sim power system toolbox.

The simulation diagram of a two level inverter with control signals is being shown in figure 8. The magnitude of the dc voltage used is $230\sqrt{2}$ which is the peak value of a sinusoidal signal whose rms vale is 230 Volt.

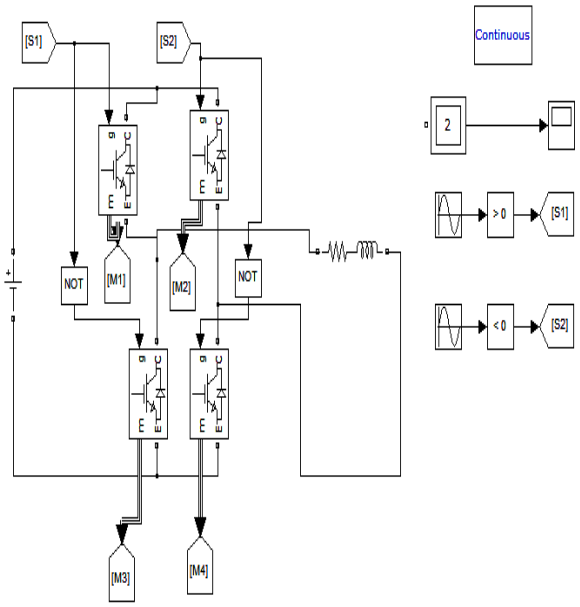

Fig 8 simulation diagram of a two level inverter

A load whose resistance is 10 Ω and inductance of 5 mili Henry is being connected to the output of the inverter to obtain the waveform of output voltage and current. Figure 9 shows the output voltage and waveform of a two level inverter.

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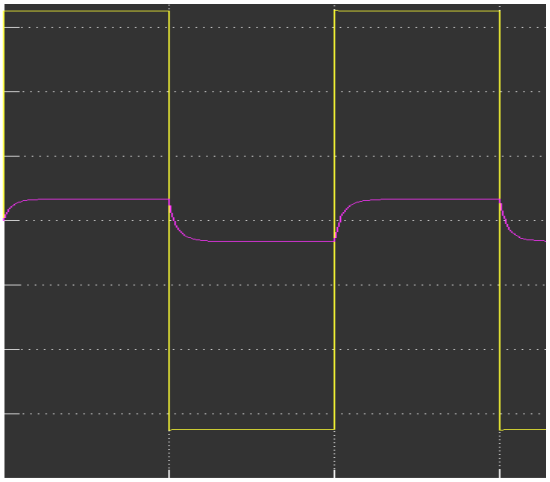

Fig 9 Output voltage and current of a two level inverter.(yellow line is waveform of voltage and the pink line is the waveform of the current)

Simulation diagram of a three level inverter with its control structure is being shown in figure 10. The outpul voltage and current is being shown in figure 11.

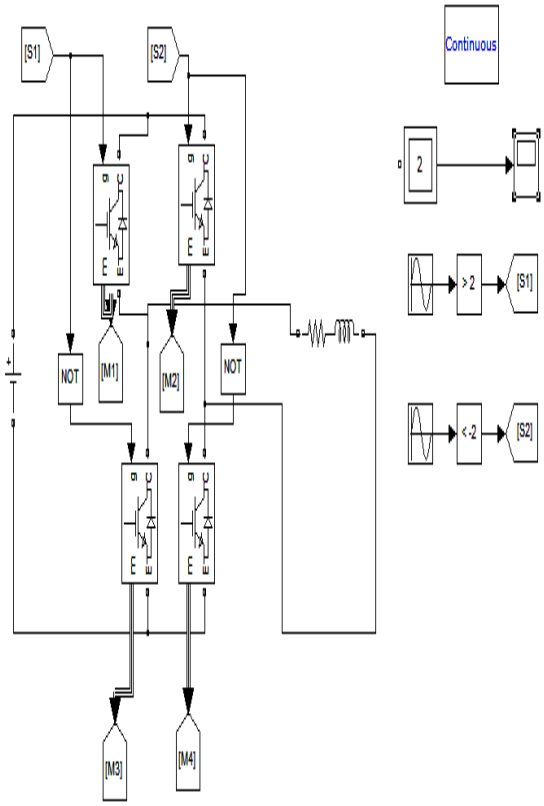

Fig 10 Simulation diagram of a three level inverter

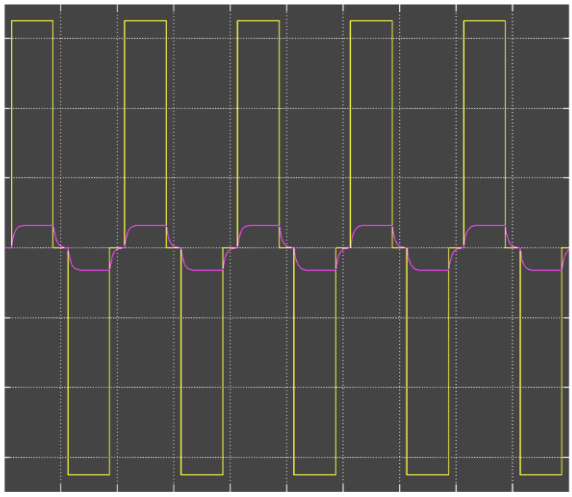

Fig 11 Output voltage and current of a three level inverter.(yellow line is waveform of voltage and the pink line is the waveform of the current)

Simulation diagram of a five level inverter with its control structure is being shown in figure 12. The output voltage and current is being shown in figure 13. Here the voltage source used is $\frac{230\sqrt{2}}{2}$.

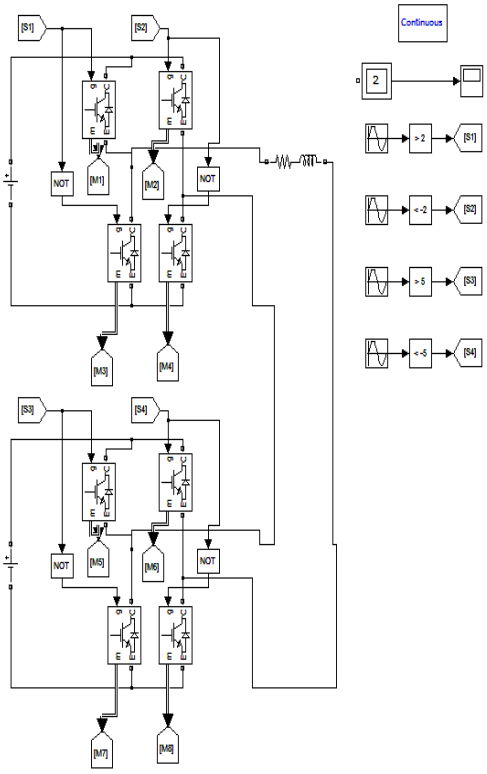

Fig 12 Simulation diagram of a five level inverter

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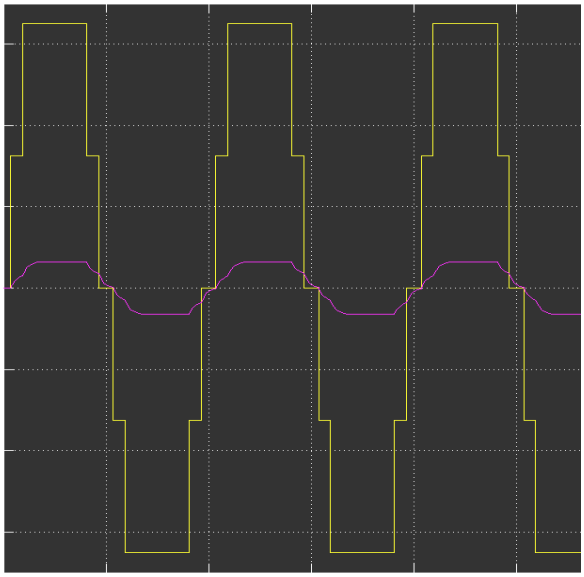

Fig 13 Output voltage and current of a five level inverter.(yellow line is waveform of voltage and the pink line is the waveform of the current)

Simulation diagram of a five level inverter with its control structure is being shown in figure 14. The output voltage and current is being shown in figure 15. Here the voltage source used is $\frac{230\sqrt{2}}{3}$.

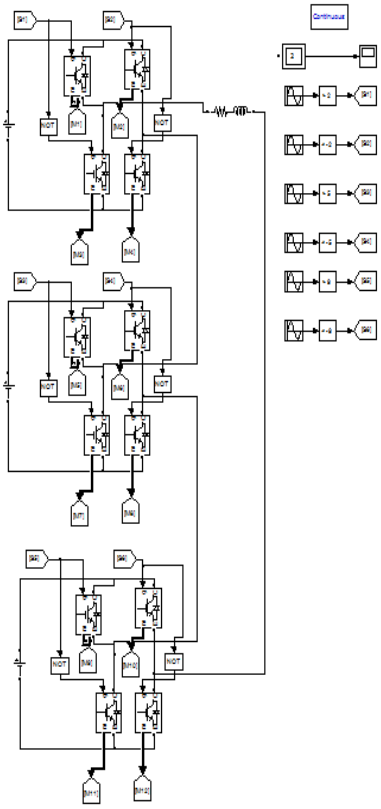

Fig 14 Simulation diagram of a seven level inverter

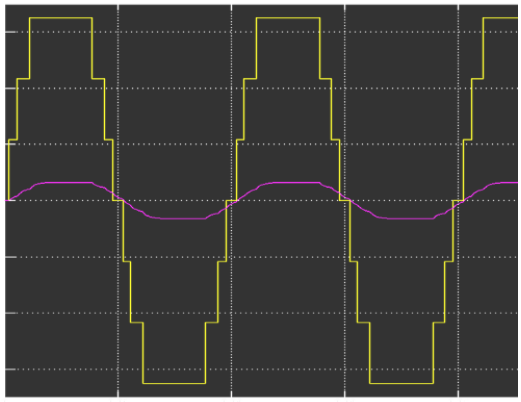

Fig 15 Output voltage and current of a seven level inverter.(yellow line is waveform of voltage and the pink line is the waveform of the current)

From the results obtained from all levels of inverter the voltage burden, current burden of the switches used, voltage harmonics and current harmonics of the output is compared in table 5.

Characteristics	Two level inverter	Three level inverter	Five level inverter	Seven level inverter
Voltage THD	48.23%	28.95 %	18.11%	14.37%
Current THD	36.97%	18.92%	12.12%	10.28%
Voltage burden on switch	325.3 V	325.3 V	162.6	108.4
current burden on switch	32.52 A	32.52 A	32.52 A	32.52 A

Table 5 Various Characteristics Of The Inverters

Conclusion: from the various results obatained from different waveforms of different inverters and comaparing the results obtained as shown in table 5 it is concluded that on increasing the number of voltage levels in an inverter the power quality of the output obtained goes on increasing the total harmonic distortion of voltage as well as the current waveform is reduced and also voltage burden on each switch is being reduced to a large extent. On further increasing the voltage l;evels the output obtained can be made nearly sinusoidal so as to supply the load with a good power quality if it is being supplied by the photo voltaic array which is having DC voltage as the output.

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