FPGA Implementation of Direct Digital Frequency Synthesizer for Communication Applications

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Abstract— Frequency synthesizers are very critical blocks in embedded communications and instrumentation applications. Direct Digital Frequency synthesis [1] is widely used technique, due to its high frequency resolution, fast switching between frequencies and modulation switching capabilities. DDFS is a critical module in Software defined radio. DDFS will be implemented using Very High Speed Integrated Circuit Hardware Description Language (VHDL). In basic mode the DDFS can generate I and Q carrier signals with a chosen frequency value. The DDFS in modulator mode can be used for producing ASK, FSK and PSK signals. In pattern generation mode the DDFS can be used to generate sine, square, triangular and arbitrary waveforms.

The proposed work involves study of Spartan-3E FPGA architecture, implementation of several modules in VHDL and finally synthesis on Spartan-3E FPGA. In this implementation FPGA suitable architectures will be used for coding various arithmetic and sequential blocks. The ModelSim tool from Mentor Graphics will be used, for simulation and functional verification of DDFS.

***Index Terms*—Xilinx, modelsim, DDFS, ASK, FSK, PSK, SPARTAN 3E, control word.**

I. Introduction

The term "frequency synthesis"[2] applies to a technique that accepts some reference input and then generates one or more signals of predefined type as according to a control word or method. The stability, accuracy, and spectral purity are the performance measures of frequency synthesizer.

Three conventional frequency synthesis techniques are popular throughout the industry: phase-lock loop [3] (PLL, or "indirect"), mix/filter/divide (direct-analog), and direct-digital. Each of these methodologies has advantages and disadvantages; hence each application requires selection based upon the most acceptable combination of compromises.

Direct-Digital synthesis (DDS) is the most recently developed frequency synthesis technique, dating from the early 1970s. All three techniques have been available to designers for decades, but it is the direct-digital synthesizer (DDS) that is evolving the most rapidly today. In fact, only a few years ago the DDS was a phenomenon with little utility, but now it is an important design tool that can not be ignored by the architects of any system demanding frequency agility. All other signal generation techniques begin with some sort of oscillator, the output of which is manipulated or controlled by the synthesizer. The DDS is unique because it is digitally deterministic; the signal it generates is synthesized from a digital definition of the desired result.

DDS uses logic and memory to digitally construct the desired output signal, and a data conversion device to convert it from the digital to the analog domain. Therefore, the DDS method of constructing a signal is almost entirely digital, and the precise amplitude, frequency, and phase are known and controlled at all times. Due to its basic principle it also called Direct Digital Frequency Synthesizer (DDFS).

A. DDFS basic principle

Direct Digital Frequency Synthesizer is a technique to produce desired output waveforms with full digital control (hence also called Numerically Controlled Oscillator) [4]. Direct digital synthesis (DDS) is becoming increasingly popular as a technique for frequency synthesis, especially if high frequency resolution and fast switching between frequencies over a large bandwidth are required.

In DDFS, the instantaneous phase of a sinusoidal signal is given by a number stored in a digital accumulator. The accumulator is incremented by adding a constant amount at each clock period, its content will represent a phase value which increases linearly with time. When the accumulator exceeds a value equivalent to 2π radians, it overflows, multiples of 2π are discarded, and the incrementation process continues to the next cycle. The number held in the accumulator is used to address a look-up table held in ROM (read- only memory) which converts phase information to a series of discrete, digitized samples of the amplitude of a sine-wave. A DAC [5] (digital-to-analogue converter), followed by a low-pass filter, convert the digital samples into an analogue signal. Different Look Up Tables (LUT) can be used to produce desired output waveform such as square wave and triangular wave etc.

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II. IMPLEMENTATION

A. Block diagram of Direct Digital Frequency Synthesizer

The basic block diagram of DDFS implemented is shown in the below figure 1. All the blocks are connected with common clock and reset signals. The delta phase value decides the phase increment for each clock pulse. Hence decides the resulting signal frequency. The Frequency modulating instantaneous value is added to the delta phase value which causes instantaneous change in frequency. Due to the digital nature of the modulator only at each clock tick the modulating signal value shall affect the resulting frequency. If the modulating signal is analog then an analog digital converter must be used to digitize the modulating signal which can be used in DDFS.

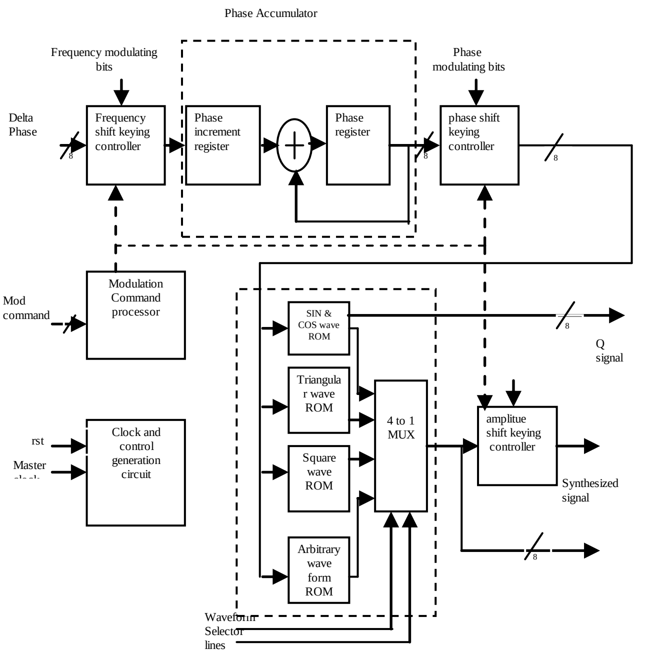

Fig. 1 Direct Digital Frequency Synthesizer

The phase accumulator produces accumulated phase value for each clock pulse. In case if the DDFS is used for phase modulation then instantaneous phase modulating signal value is added to the phase output of phase accumulator. This resulting phase value is given to the four Look Up Tables. Each Look Up Table is configured to produce a specific waveform. The logic used to generate the Look Up Tables is discussed in the further sections.

The outputs of four Look Up Tables are given to the input lines a 4 to 1 Multiplexer. This multiplexer connects one of the inputs to the output depending on the select lines. The output of Multiplexer consists of 8 amplitude bits which is the final output in case required modulation schemes are FM or PM. In case of amplitude modulation, the output of Multiplexer is multiplied with instantaneous modulating signal.

In three modulation schemes if modulating signal is analog in nature then an appropriate Analog to Digital converter is required to convert into 8 bit digital output.

B. PIPO n bit generic register and adder

The Parallel in Parallel Out shift register cells are required in phase accumulator block to hold frequency and phase values. Synchronization is required between the phase increment register and phase register. This is achieved by connecting a common clock signal. Generic is used in VHDL implementation which allows to instantiate the PIPO component any bit size. The N-bit generic adder is implemented in VHDL with simple ripple carry adder logic.

C. Phase Accumulator

The phase accumulator consists of phase increment register, adder and phase register. The figure 2 shows the inner blocks of phase accumulator.

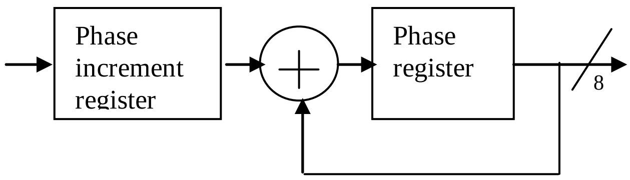

Fig. 2 Phase Accumulator

The phase increment register stores the instantaneous phase increment values resulting from frequency modulation control block. This is fed to a 8 bit adder as one of its input. The other input for adder is phase register output. The phase register holds the instantaneous phase for each clock pulse. The accumulated phase also is represented by 8 bits, which limits the maximum phase by 11111111, and addition by 1 to maximum value causes the phase to become 00000000 This is expected and desired since the Look Up Tables are programmed to consider 255 as highest phase value and phase increment by one results next cycle of waveform. Since 8 bits are used to represent the 0^{O} to 360^{O} the increment in digital phase value by one causes effective increment of 1.40625^{O} (results by dividng 360^{O} with 256 maximum possible combinations of 8 bits) . This also implies that outputs can’t have more that 256 samples for one cycle.

D. Look up tables

Four Look Up Tables are implemented to produce four different output waveforms, namely sine wave, square wave, triangular wave and arbitrary waveform. As a standard practice these LUTs are implemented using VHDL CASE statement.

Since the generation of square wave requires producing only two amplitude levels in one cycle, it can be implemented without Look Up Table. A stair case waveform Look Up Table is implemented for arbitrary waveform. It is possible to implement any arbitrary waveform, by appropriately changing the content of LUT. To fully characterize arbitrary waveform in 8 bit DDFS, we require 256 amplitude values

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corresponding to 256 phase values. The ports of all four look up tables are same.

E. Modulation Command Processor

The Modulation command processor is implemented for carrying out digital versions of frequency modulation, phase modulation and amplitude modulation. For all these three modulations the digital 8 bit modulating signal is expected. In case if the modulating signal is analog that needs to be converted in to 8 bit digital by appropriate Analog to Digital Converter.

The frequency modulation is carried out by frequency modulation controller which is simply an adder adding the phase increment value input for DDFS and instantaneous modulating signal value. Since the phase increment value or delta phase value is proportional to instantaneous frequency of ouput signal of DDFS, controlling that parameter leads to Frequency modulation.

The phase modulation controller adds the output of phase accumulator to the instantaneous value of phase modulating signal. The resulting sum is fed to the LUTs to produce amplitude bits corresponding to the input phase bits.

The amplitude modulator planned in this paper analogous to product modulator. The amplitude bits at the output of multiplexer are multiplied with instantaneous amplitude of modulating signal. To verify the modulation effects from these modulation controllers, these blocks should work in complete DDFS module. Hence the resulting outputs for three types of modulations are presented.

III. SIMULATION RESULTS

A. FSK output

Fig. 3 FSK output

B. PSK output

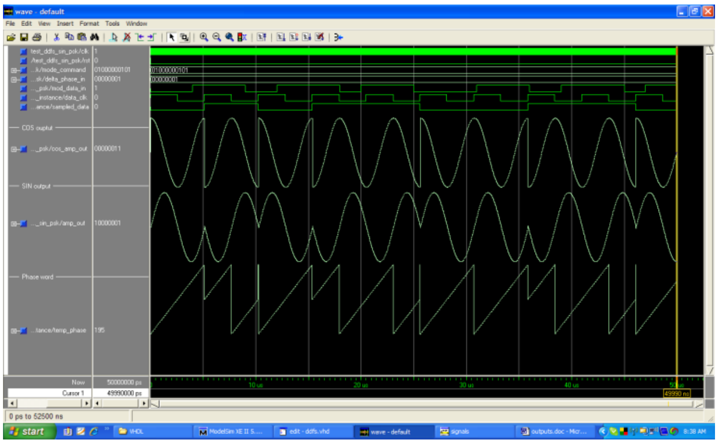

Fig. 4 PSK output

C. ASK output

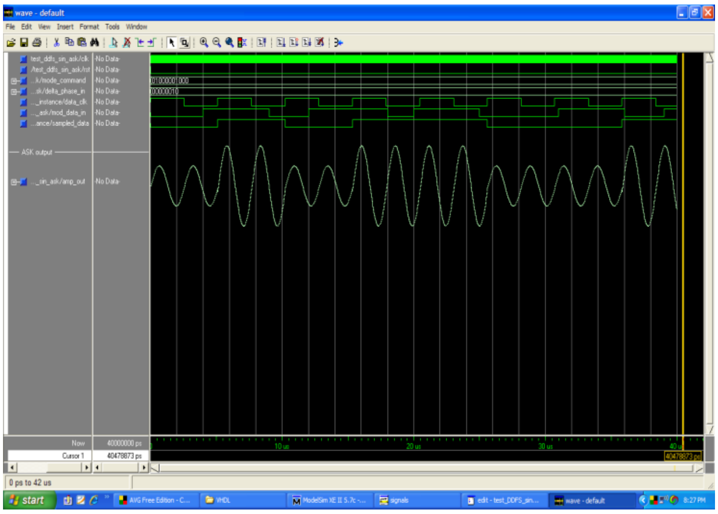

Fig. 5 ASK output

D. Pattern generator mode output

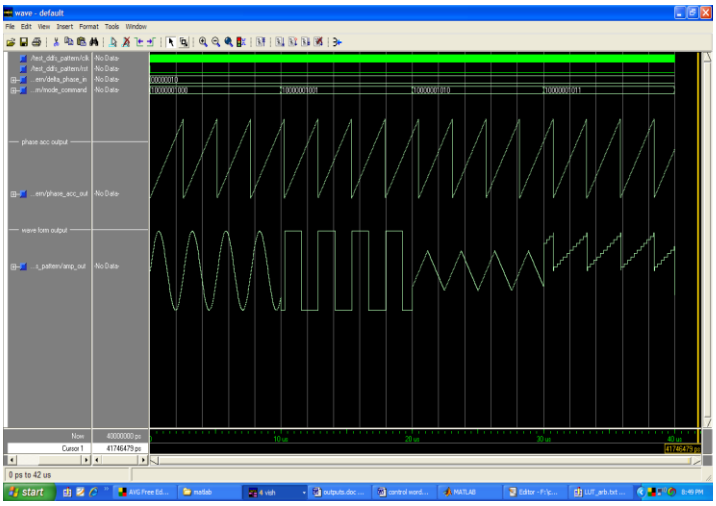

Fig. 6 Pattern generator mode output

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IV. SPARTAN 3E

A. Spartan 3E Board

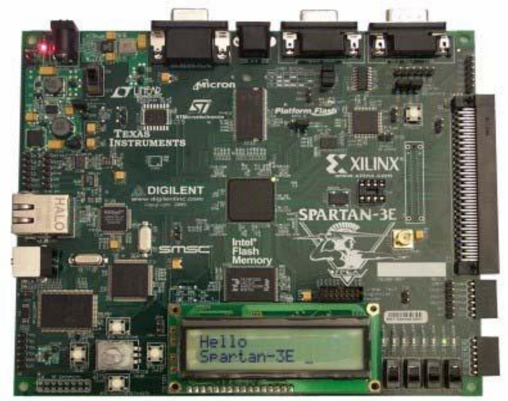

Fig. 7 Spartan 3E board

B. FPGA Structure

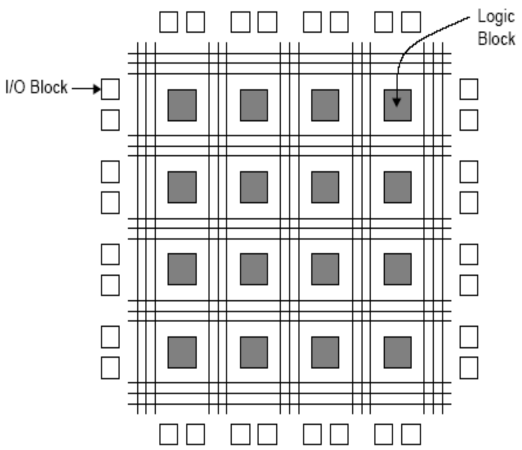

Fig. 8 FPGA structure

V. CHIP SCOPE RESULTS

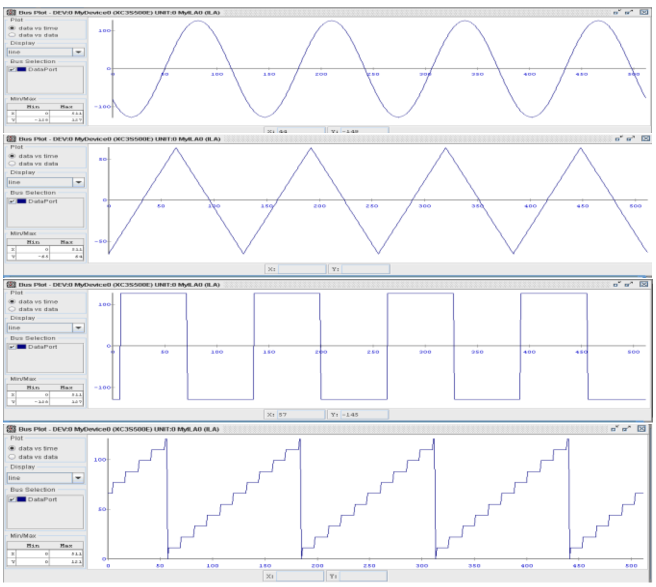

Fig. 9 Chipscope results

VI. CONCLUSION

A major advantage of a direct digital synthesizer (DDS) is that its output frequency, phase and amplitude can be precisely and rapidly manipulated under digital control. It is easy to include different modulation capabilities in the DDS by using digital signal processing methods, because the signal is in digital form. By programming the DDS the flexibility of the DDS makes it ideal for different types of signal generators.

The FPGA based DDFS is highly useful in semi custom VLSI chips, FPGA based VLSI solutions, signal processing cards, Instrumentation and Digital communications. The present work shows basic DDFS implementation proving the design by synthesis on FPGA. If latest/fast FPGAs are used very high bandwidth DDFS can be implemented efficiently.

REFERENCES

[1] Richard J. Kerr and Lindsay A. Weaver, "Pseudorandom Dither for Frequency Synthesis Noise," U.S. Patent 4,901,265, filed December 14, 1987, issued February 13, 1990.

[2] Henry T. Nicholas, III and Henry Samueli, "An Analysis of the Output Spectrum of Direct Digital Frequency Synthesizers in the Presence of Phase-Accumulator Truncation," IEEE 41st Annual Frequency Control Symposium Digest of Papers, 1987, pp. 495-502, IEEE Publication No. CH2427-3/87/0000-495.

[3] Douglas L. Perry ,"VHDL", Second Edition, McGraw-Hill, Inc, 1993

[4] Zainalabedin Navabi, "VHDL Analysis and Modelling of Digital Systems", McGraw – Hill, Second Edition

[5]A Direct Digital Frequency Synthesis System for Low Power Communications by Alistair McEwan, Sunay Shah and Steve Collins, Department of Engineering Science University of Oxford Parks Road Oxford UK

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