Design and Modelling of Hybrid CMOS-SET based Parity Generator Nano IC

Dr. Jayanta Gope, Sanjay Bhadra, Santanu Debnath, Abdullah Alom, Abdul Wakil Lasker

Abstract— **A new designed structure namely hybrid CMOS SET can amalgamate both the merits of Single Electron Transistor (SET) and CMOS transistor. This has raised immense possibilities in future VLSI/ULSI circuits. Present endeavor is an attempt to model Hybrid CMOS SET based parity generator circuit to be incorporated in next generation electronic systems. The circuit operation has been validated using TANNER environment.**

Keywords: SET, Hybrid CMOS-SET, MIB, Parity Generator, Nano IC.

I. INTRODUCTION

The post CMOS era observed the offspring of several new device technologies including single electron transistor (SET) technology. It is considered to be one of the most promising technology bearing the blessings of high speed and simplistic structure. The discrete charge of Single Electron Transistor (SET) arise from the tunneling phenomena that discriminate SET from other conventional technology. Besides, it has potential to transfer 1 bit of information by using single or very few number of electrons. It posses numerous advantages like high speed, robustness, high integration density, simplicity, low power consumption, low heat dissipation and other topologies. This is why Single Electronic Transistor (SET) is envisioned as a dominant emperor for future ultra-dense digital electronics [1-6]. Amid all such merits, SET's alike other existing device topologies do posses few demerits including low voltage gain, random background charge problem and room temperature operations. Study reveals that fabrication of SET requires less than 0° C temperature which is quite tough. Moreover, the advanced e-beam lithography technique needs to be sharpened enough to attained the desire merits of SET.

One the other hand, the rapid progress of present electronic industry depends upon advancement in CMOS technology which not only produces high gain but also the fabrication of CMOS made IC's are less complex; in contrast it suffers from few intrinsic limitations such as high power dissipation, scaling problems and greater power consumption.

Scientist intended to sum up both the positive consequence of CMOS and SET. Thereby the idea of hybridizing CMOS with SET evolved which was later coined by Researchers worldwide. The Hybrid CMOS-SET is primitive brain-child of Prof. Santanu Mahapatra and his team of Co-Researchers. They designed the Co-tunneling of both CMOS and SET popularly known as MIB model [7]. It has been empirically demonstrated that the merits of Hybrid CMOS-SET shadows all limitations of individual CMOS or SET. Hereby the authors being truly motivated by effectual linkage of Hybrid CMOS-SET has attempted this modeling of high speed, low power consuming parity generator nano IC.

The following section attributes the architecture of parity generator nano IC and its modus operandi. Finally the parity generator nano IC is compared with its conventional counterpart.

II. FUTURE PARITY GENERATOR NANO IC

In communication engineering error detection is the epicenter of a multimillion research initiated by governments worldwide. In real life communication it is evident that digital signal when transmitted, produces a simple noise impulse that can change bit logic level of a data bit. Parity bits are added to the signal to detect such errors introduced in the data bit. Conventionally there are existing to ways of adding parity bit and data bit. Parity bits when are added in a manner to add an even number of ones (1), then it is even parity bit whereas incase of odd parity bit- odd number of ones (1) are considered.

During modeling of the circuit three consequently Hybrid CMOS-SET based XOR gates have been connected in situ such as the output of the first XOR is the input of the second XOR and output of the second XOR gate is the input of the successive XOR gates. Before deliberating the construction of proposed model the authors in very brief attributes the simple but most efficient few hybrid CMOS-SET logic gates for easy understanding and simplicity [8-12].

The uniqueness of such logic synthesis is that the load of the hybrid CMOS-SET circuit is produced by SET. That is why the PUN comprises of SET whereas the PDN are made of CMOS and is always grounded. Such sophistication intensifies the electron transport phenomenon and the speed of the devices thereby increases manifold.

The subsequent section attributes a simple parity generator nano IC in Fig. 5, having 56 number of tunnel junctions, 73 number of capacitors and the working voltage is 0.18-0.2 Volts.

The circuit when simulated using TANNER tools shows better trade off in obtaining the output of the proposed IC. The substantial input voltage is quite low compared to simple CMOS made parity generator IC. Also the generation of output requires few nano second which is quite speedy.

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Following the space limitations the Authors here have limited them-selves detailing the inherent operations of the proposed nano IC.

III. Comparative Study of the IC

The comparative study led to few decisive factors including inherent high speed, high integration density, low power consumption, simplicity and robustness. Following table represents the same in a subtle but in a state forward presentation.

TABLE: ***Study of power dissipation and power consumption of different device in the proposed Hybrid CMOS-SET based parity generator nano IC***

Gate	Power Consumption	No. of CMOS	No. of SET
AND	0.01V	3	3
OR	0.01V	3	3
NOT	0.01V	1	1

As tabled in the above section it is apparent that the proposed model is 200 times faster and takes nearly 0.01V power. These portray the approximation only, exact numerical are at present not being attributed because further investigation in this matter is still continuing. The apparent results truly advocate for the incorporation of Hybrid CMOS-SET in designing future ultra-dense VLSI/ULSI circuits.

IV. Conclusion

Designing Hybrid CMOS-SET parity generator has been enumerated in this short communication; the authors would like to add that the task is highly painstaking as well as time consuming and certainly it posses all the goodness of nano technology. The comparative study is included in order to explore the novel merits of future Nano electronic devices and to be incorporated in next generation consumable electronics. The augmentation of such research has undoubtedly geared up and it now requires potential contribution from all fields of electronic research. Last but not least the significance of such research is to be studied more conveniently.

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VI. References

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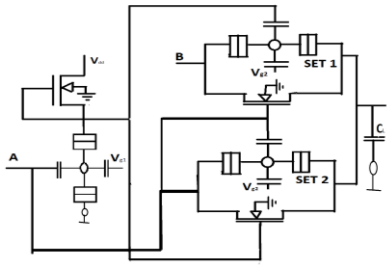

Fig1. Hybrid CMOS-SET based AND realization

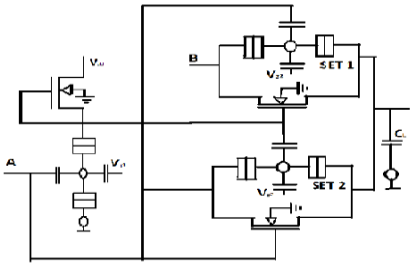

Fig2. . Hybrid CMOS-SET based OR realization

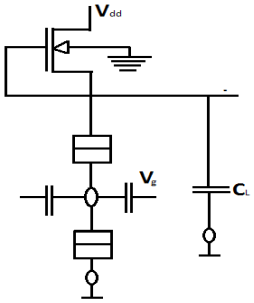

Fig 3. Hybrid CMOS-SET based NOT realization

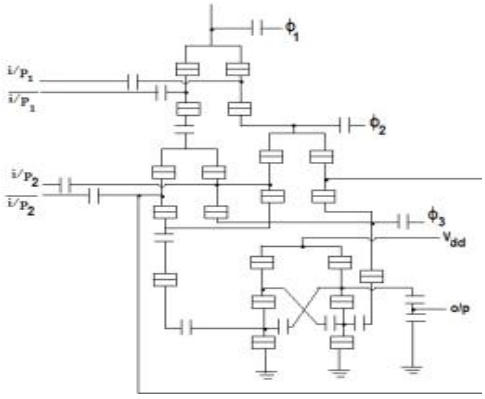

Fig 4. Hybrid CMOS-SET based XOR realization

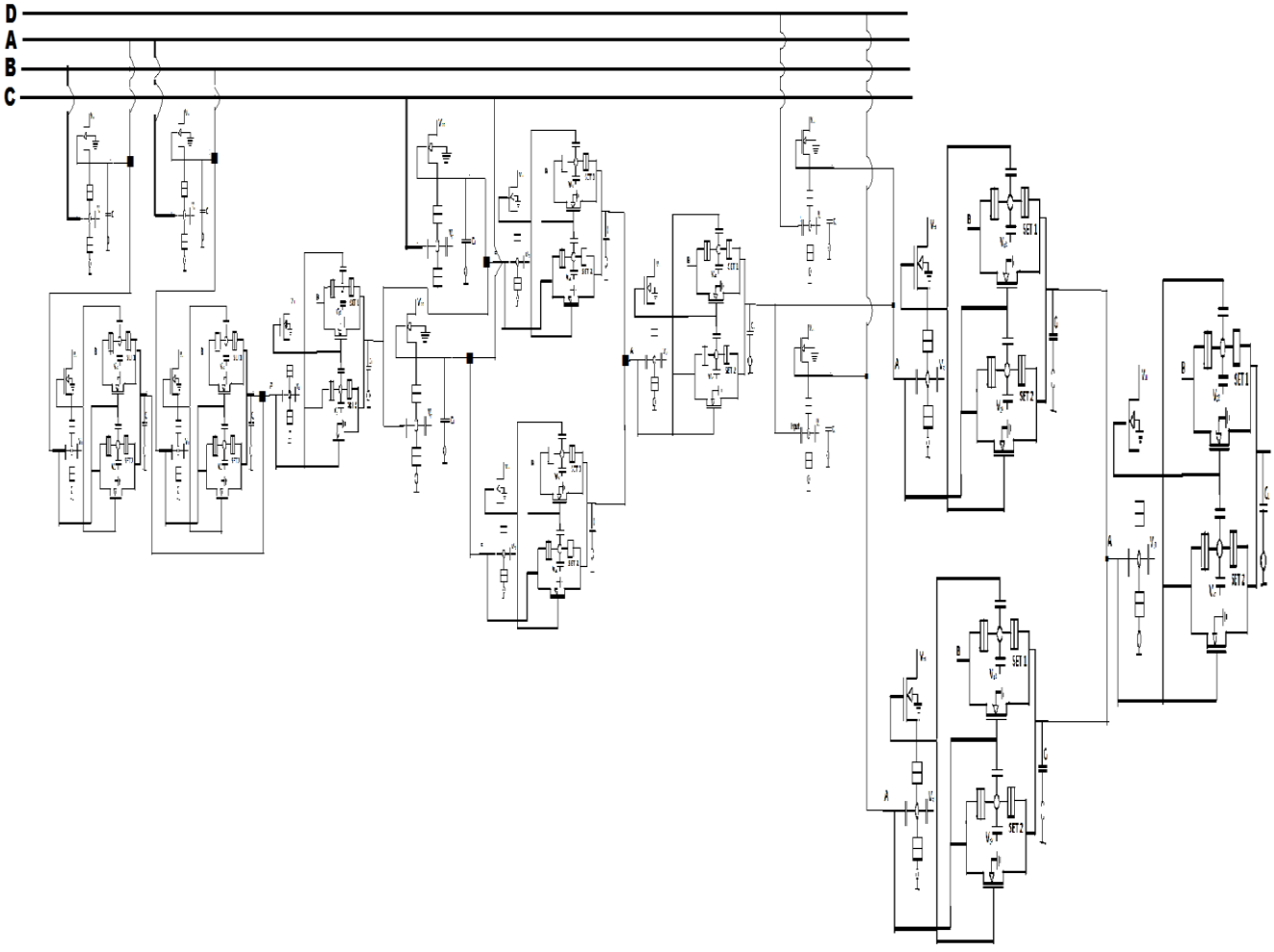

Fig.5. Hybrid CMOS-SET based Parity Generator realization

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