Implementation of Optimized Cascaded Integrator Comb Filters for Digital Up, Down Conversions

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Abstract— **Digital conversion is a fundamental part of many digital radio systems, which include up-conversion of the discrete baseband signal stream into a high-resolution radio signal at the transmitter, and down-conversion of a high-resolution radio signal back into a baseband signal at the receiver. Digital down conversion (DDC) and Digital Up Conversion(DUC)[1] are the core technologies in wireless communication systems, as well as important components of digital intermediate frequency receiver system.**

When a signal is to be rate converted to a different clock frequency then special filter architectures running at high clock rates are required. Normal FIR architectures and its variants fail to work at such high frequencies. Cascaded Integrator comb (CIC) filters are useful to reduce as well as to increase the data sampling rate.

In this project a full fledged digital up conversion and down conversion systems will be developed in VHDL for FPGA based Software Defined Radio applications. The CIC based architecture will be implemented in VHDL and will be tested on Xilinx FPGAs.

***Index Terms*—DDC, DUC, CIC, comb, Xilinx, VHDL.**

I. INTRODUCTION

Digital conversion is a fundamental part of many digital radio systems, which include up-conversion of the discrete baseband signal stream into a high-resolution radio signal at the transmitter, and down-conversion of a high-resolution radio signal back into a baseband signal at the receiver. Digital Up Converters (DUC) and Digital Down Converters (DDC) are widely used in communication systems for converting the sample rate of signals. Digital up conversion is required when a signal is translated from baseband to intermediate frequency (IF) band. Digital down conversion happens when a signal is converted from intermediate frequency band to baseband. DUCs and DDCs typically include frequency shifting using mixers, in addition to sampling rate conversion.

A. Digital down conversion

A digital down-converter (DDC) converts a digitized real signal centered at an intermediate frequency (IF) to a baseband complex signal centered at zero frequency. A DDC consists of three basic components they are direct digital synthesizer (DDS), a low pass filter (LPF) and a down sampler. Digital Down-Converter (DDC) is a major component of digital radios. Numeric Controlled Oscillator (NCO) and a mixer are used to down convert the input signal to baseband. In decimation process CIC filters are anti aliasing filters before down sampling. The DDC uses the lower resource utilization, low power consumption, high speed and low circuit complexity in wireless communication systems to reduce the cost of main design.

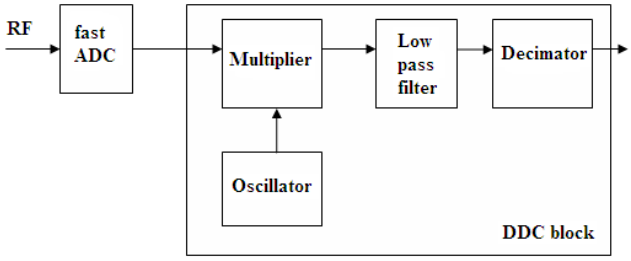

Fig.1 Theoretical DDC Block Diagram

Any suitable low-pass filter can be used including FIR, IIR and CIC filters. The most common choice is a FIR filter for low amounts of decimation (less than ten) or a CIC filter followed by a FIR filter for larger down sampling ratios. DDC's are most commonly implemented in logic in field-programmable gate arrays or application-specific integrated circuits.

B. Digital up conversion

Digital up converter (DUC) translates the base band signal to a higher frequency band. This is done by first up-sampling the base band signal to the required sampling frequency and then mixing it with a high frequency carrier. The DUC can be extensively used in wireless and wire line communication systems. A DUC system consists of a Cascaded Integrator Comb (CIC) interpolation filter, CIC compensation filter, multiplier and a direct digital synthesizer. The input signal is first given to CIC filter for upsampling, then fed to CIC compensation filter for filtering input signal and finally it is multiplied with the carrier signal generated by DDS. Compensation filter is also type of finite impulse response (FIR) filter used to compensate for loses in cascaded integrator comb (CIC) filter. A CIC compensation filter is used to provide ideal pass band and narrow transition region for the input signal and upsample the input signal by factor two.

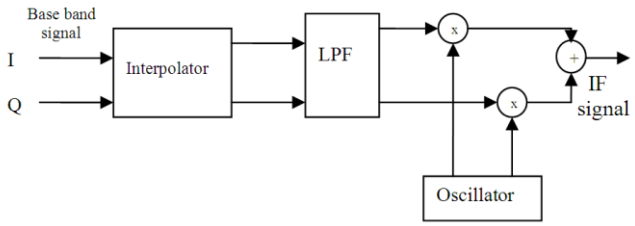

Fig.2 Theoretical DUC Block Diagram

II. CASCADED INTEGRATOR COMB FILTERS[2]

As data converters become faster and faster, the application of narrow-band extraction from wideband sources, and narrow-band construction of wideband signals is becoming more important. These functions require two basic signal processing procedures: decimation and interpolation. And while digital hardware is becoming faster, there is still the need for efficient solutions. Techniques found in very well in practice, but large rate changes require very narrow band filters. Large rate changes require fast multipliers and very long filters. This can end up being the largest bottleneck in a DSP system.

An efficient way of performing decimation and interpolation was introduced by Hogenauer, who devised a flexible, multiplier-free filter suitable for hardware implementation that can also handle arbitrary and large rate changes. These are known as cascaded integrator-comb filters, or CIC filters for short. In digital signal processing[3], a cascaded integrator-comb (CIC) is an optimized class of finite impulse response filter combined with an interpolator or decimator.

A CIC filter consists of one or more integrator and comb filter pairs. In the case of a decimating CIC, the input signal is fed through one or more cascaded integrators, then a down-sampler, followed by one or more comb sections (equal in number to the number of integrators). An interpolating CIC is simply the reverse of this architecture, with the down-sampler replaced with a zero-stuffer (up-sampler). The CIC filter finds applications in interpolation and decimation. Unlike most FIR filters, it has a decimator or interpolator built into the architecture. The two basic building blocks of a CIC filter are an integrator and a comb.

A. *Basic integrator*

An integrator is simply a single-pole IIR filter with a unity feedback coefficient:

$$y[n] = y[n-1] + x[n] \tag{1}$$

This system is also known as an accumulator. The transfer function for an integrator on the z- plane is

$$H_I(z) = \frac{1}{1 - z^{-1}} \tag{2}$$

The power response is basically a low-pass filter with a 20 dB per decade (- 6 dB per octave) roll off, but with infinite gain at DC. This is due to the single pole at z = 1; the output can grow without bound for a bounded input. In other words, a single integrator by itself is unstable.

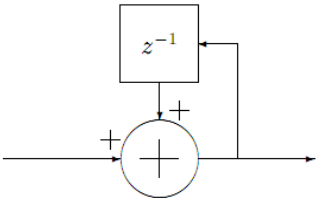

Fig.3 Basic Integrator

B. *Basic comb*

A comb filter running at the low sampling rate, f_s / R, for a rate change of R is an odd- symmetric FIR filter described by

$$y[n] = x[n] - x[n - RM] \tag{3}$$

In this equation, M is a design parameter and is called the differential delay. M can be any positive integer, but it is usually limited to 1 or 2. The corresponding transfer at f_s / R

$$H_C(z) = 1 - z^{-RM} \tag{4}$$

When R = 1 and M = 1, the power response is a high-pass function with 20 dB per decade (6 dB per octave) gain (after all, it is the inverse of an integrator). When RM 6= 1, then the power response takes on the familiar raised cosine form with RM cycles from 0 to 2π .When we build a CIC filter, we cascade, or chain output to input, N integrator sections together with N comb sections. This filter would be fine, but we can simplify it by combining it with the rate changer.

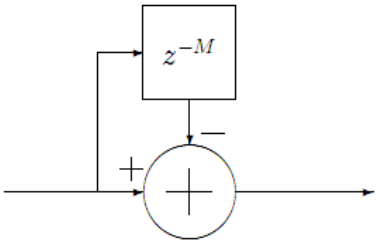

Fig.4 Basic Comb

To Summarize a CIC decimator and CIC interpolator would have N cascaded integrators stages at running at clock frequency f_s, followed by a rate change by a factor R, followed by N cascaded comb stages running at f_s / R and vice versa.

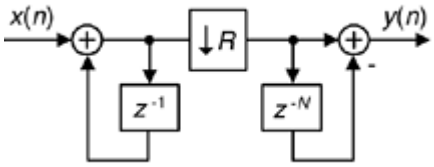

Fig.5 CIC decimation Filter

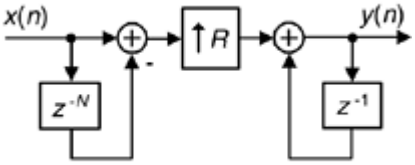

Fig.6 CIC interpolation Filter

III. CIC BASED IMPLEMENTATION

A. Decimation filter

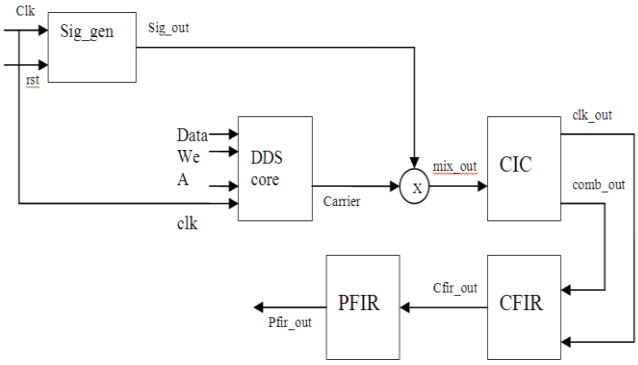

Fig. 7 DDC block diagram using CIC Filters

In the DDC based CIC filters The Test signal is generated by mixing the two signals with frequencies of 300 kHz and 2 MHz. These two signals are generated by using two DDS cores as shown in the below figure 8.

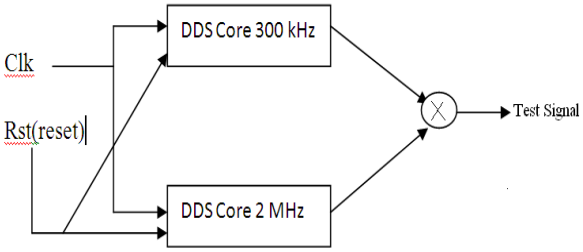

Fig.8 Test signal generator using two DDS cores

These two signals are mixed and given as the input to the CIC Filter In Phase and Quad Phase sections separately. The output of the CIC Filter is followed by the CFIR[4] (Compensating FIR Filter) and PFIR (Programmable FIR Filter).

The CFIR Filter is used to compensate the output of the CIC Filter and PFIR Filter is used to solve the bandwidth issues in both the sections. The CIC filter frequency response does not have a wide, flat pass band. To overcome the magnitude droop, a FIR filter that has a magnitude response that is the inverse of the CIC filter can be applied to achieve frequency response correction. Such filters are called compensation filters. The cic filter response shown below figure 9. The CIC filters exhibits the pass band droop.

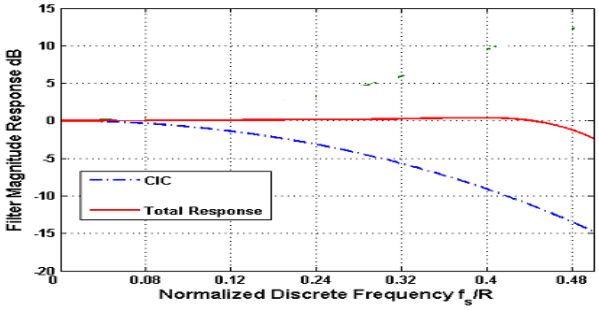

Fig.9 CIC filter Response

CFIR filter is used compensate this pass band droop. Compensating FIR filter is required to compensation the magnitude response non-linearity in pass band. Compensation filter response shown in below figure 10.

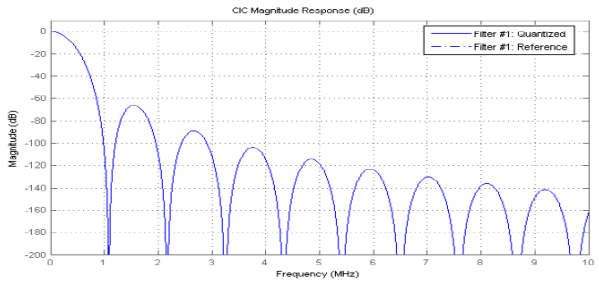

Fig.10 compensation filters response

Equation shows the magnitude response of an N-stage CIC filter at high frequency (f_S):

$$|H(f)| = \left| \frac{\sin(\pi M f)}{\sin\left(\frac{\pi f}{R}\right)} \right|^N \quad (5)$$

An example of a CIC filter magnitude response To achieve a flat pass band, the compensation FIR filter should have a magnitude response that is the inverse of above Equation, as shown in below Equation

The response after using the CFIR Filter is as shown in the below figure 11.

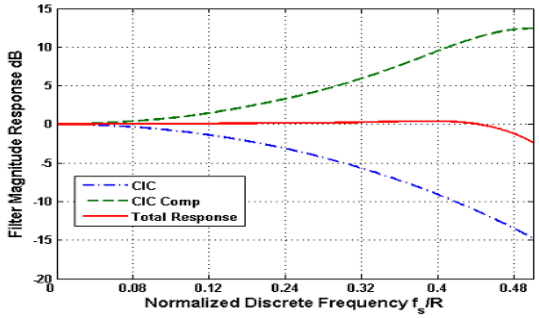

Fig.11 Response after using the CFIR Filter

B. Interpolation filter

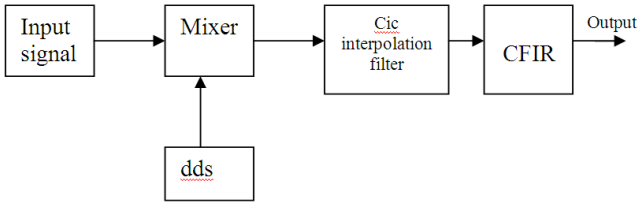

Fig. 12 DUC block diagram using CIC Filters

The block diagram of digital up converter (DUC) is shown in the figure 12. A DUC system consists of a Cascaded Integrator Comb (CIC) interpolation filter, CIC compensation filter, multiplier and a direct digital synthesizer. Direct digital synthesizer (DDS) is used to generate a carrier signal in order to modulate with the input base band signal. The modulated signal is fed to the CIC interpolation filter and the output is followed by CFIR filter.

The interpolating CIC filter is used for upsampling[5] the input signal Unlike FIR filters, the decimator or interpolator can be built into the CIC filter architecture. Cascaded Integrator Comb (CIC) interpolating filter can be widely used for up-sampling the input signal in digital up converter. In the case of interpolating CIC filter, cascaded comb sections comes first, then an up-sampler and followed by integrator sections. In this work, the CIC filter upsamples the filtered signal at the rate of two. Compensation filter is just a FIR filter which is used to in order compensate the losses of CIC filter. A CIC compensation filter provides ideal pass band and narrow transition region for the input signal. These properties are not provided by the CIC filters.

IV. Simulation Results

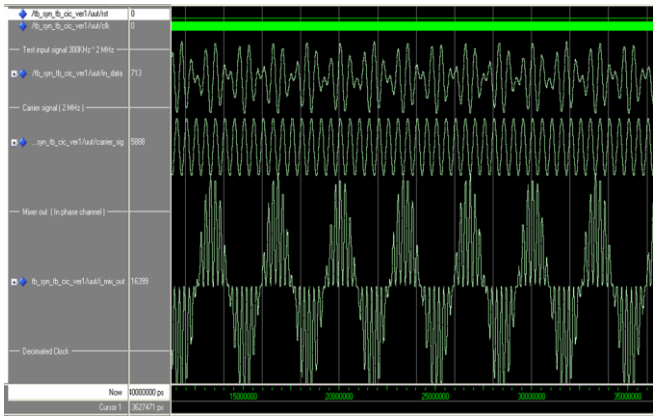

Fig.13 DDS outputs

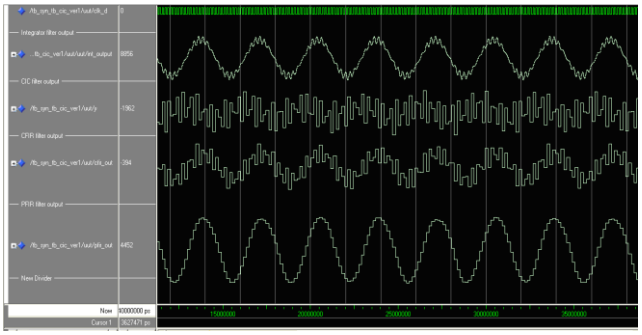

Fig.14 output of CIC decimator filter, CFIR Filter and PFIR filter.

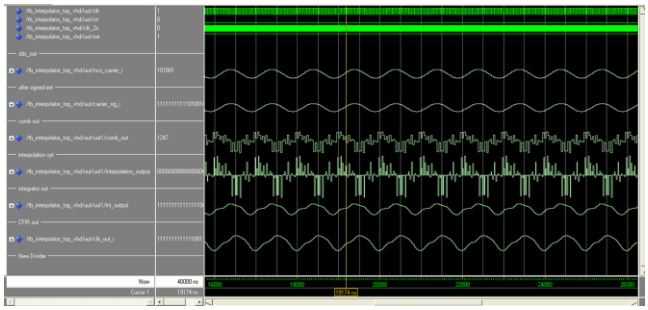

Fig.15 output of CIC interpolation filter.

V. Chipscope Results

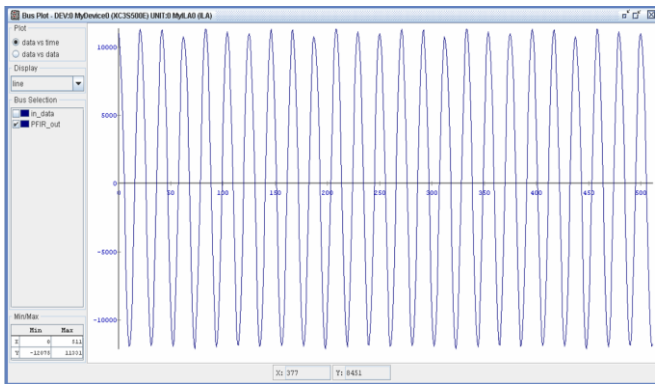

Fig.16 PFIR output of DDC.

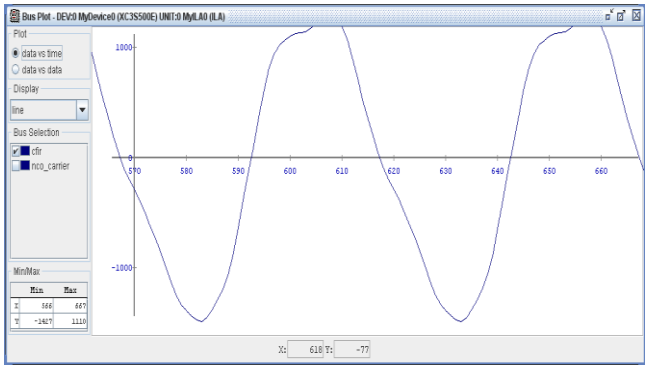

Fig.17 CFIR output of DUC.

VI. Conclusion

The CIC filter based digital up, down conversions are designed and implemented on FPGA SPARTAN 3E board. VHDL generic coding style is followed to make the blocks highly configurable so that the same design with generic map can be configured for different data rates. The outputs of each block is simulated and synthesized in Modelsim and Xilinx ISE. Chipscope results are also verified for DDC and DUC.

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