Design and Implementation of QAM Architecture on FPGA for Wimax Applications

SUBRAT KUMAR SAHOO, M. A. ASIMA BEGUM, G. KALYAN

Abstract— Wimax is an emerging and promising technology to provide high speed broadband connectivity to the mobile phone using latest modulation and multiplexing techniques. Wimax mainly uses QAM modulation technique due to its spectrum efficiency and several other added advantages. In such Wimax communication systems, synchronization which consists of both carrier and symbol level is the most challenging task. There have been several researchers paying attention to solve synchronization problem in particular, hence build a whole communication system.

The FPGA technology has been playing a considerable role in portable and mobile communication. This is due to the features of flexibility, accuracy and configurability in designing and implementation. This paper presents a complete design for a 16-QAM transmitter and receiver based on VHDL. The implemented system can be used in typical Wimax system and any other QAM based communication systems. The carrier synchronization and timing synchronization both issues are covered in the implementation. The transmitter of QAM consists of symbol mapper, NCO and modulator blocks. The NCO is used for carrier generation. The receiver of QAM consists of NCO, carrier synchronization block, time synchronization block, symbol demapper and clock managing unit. All blocks will be realized in VHDL and will be aimed to implement with generic feature so that the designs are scalable for different bit sizes.

***Index Terms*—Xilinx, Modelsim, 16-QAM, DDS, WIMAX**

I. INTRODUCTION

Quadrature Amplitude Modulation or QAM is a form of modulation which is widely used for modulating data signals onto a carrier used for radio communications. It is widely used because it offers advantages over other forms of data modulation such as PSK, although many forms of data modulation operate along side each other.

Quadrature Amplitude Modulation[1], QAM is a signal in which two carriers shifted in phase by 90 degrees are modulated and the resultant output consists of both amplitude and phase variations. In view of the fact that both amplitude and phase variations are present it may also be considered as a mixture of amplitude and phase modulation.

Quadrate amplitude modulation (QAM) may exist in what may be termed either analogue or digital formats. The analogue versions of QAM are typically used to allow multiple analogue signals to be carried on a single carrier. For example it is used in PAL and NTSC television systems, where the different channels provided by QAM enable it to carry the components of chroma or colour information. In radio applications a system known as C-QUAM [2] is used for AM stereo radio. Here the different channels enable the two channels required for stereo to be carried on the single carrier.

Digital formats of QAM are often referred to as "Quantized QAM"[3] and they are being increasingly used for data communications often within radio communications systems. Radio communication systems ranging from cellular technology through wireless systems including WiMAX, and Wi-Fi 802.11 use a variety of forms of QAM, and the use of QAM will only increase within the field of radio communications.

QAM, Quadrature amplitude modulation is widely used in many digital data radio communications and data communications applications. A variety of forms of QAM are available and some of the more common forms include 16 QAM, 32 QAM, 64 QAM, 128 QAM, and 256 QAM[4]. Here the figures refer to the number of points on the constellation, i.e. the number of distinct states that can exist.

The various flavors of QAM may be used when data-rates beyond those offered by 8-PSK [5] are required by a radio communication systems. This is because QAM achieves a greater distance between adjacent points in the I-Q plane by distributing the points more evenly. And in this way the points on the constellation are more distinct and data errors are reduced. While it is possible to transmit more bits per symbol, if the energy of the constellation is to remain the same, the points on the constellation must be closer together and the transmission becomes more susceptible to noise. This results in a higher bit error rate than for the lower order QAM variants. In this way there is a balance between obtaining the higher data rates and maintaining an acceptable bit error rate for any radio communications system

II. IMPLEMENTATION OF BLOCK DIAGRAM

A. QAM modulation and demodulation

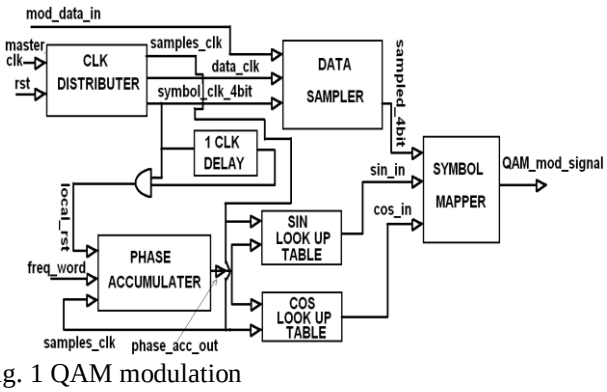

Fig. 1 QAM modulation

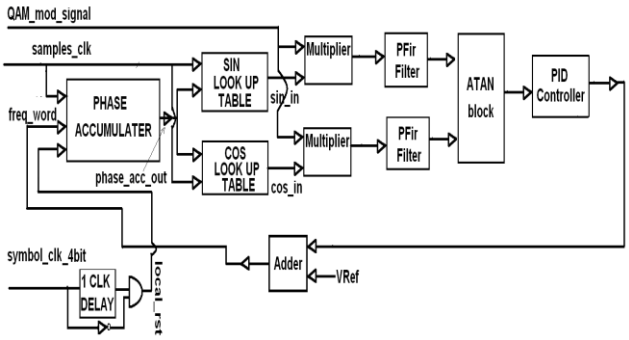

Fig. 2 QAM demodulation

The QAM modulator consists of clk distributor, Data sampler, phase accumulator, sin lookup table, and sin lookup table, qam IQ modulator.

The QAM demodulator consists of clk distributor, Data sampler, phase accumulator, sin lookup table, and pfir lpf,pid controller, dpll for carrier recovery.

B. CLK Distributor

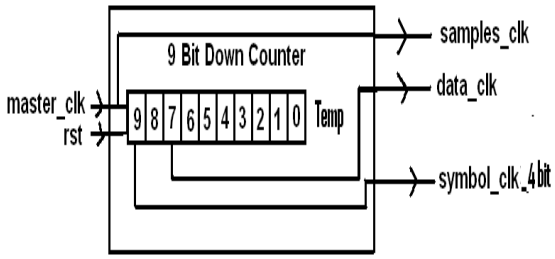

Fig. 3 block diagram of clock distributor

In Clk_distributor the inputs for the clock generation module is reset and master clock of 50Mhz and the outputs are sample_clk, data_clk and symbol_clk. The sample_clk is same as the master_clk. The clock generation module consists of 9 bit counter. In the counter 7^{th} bit value gives the output of data_clk and the 9^{th} gives the output of symbol_clk . The data_clock will be at active low for 128 clk pluses and for other 128 clk pluses will be in active high to complete one cycle. Symbol_clk will be at active low for 512 clk pluses and for other 512 clk pluses will be in active high to complete one cycle.

C. Data sampler

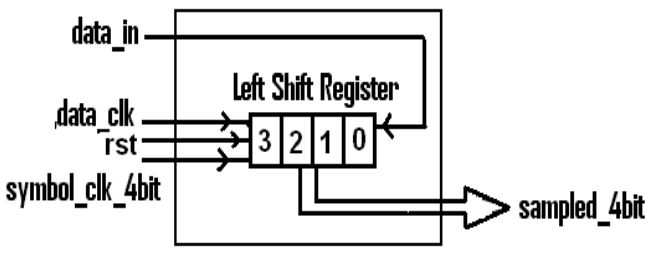

Fig. 4 block diagram of data sampler

Rst is used to clear or reset module, data_clk will be four times faster then symbol_clk_4bit When rst is active high then left shift register will be cleared, if rst is active low with raising edge of data_clk then data_in will be forced on to the LSB bit of left shift register. Left shift register will be shifter one bit. Raising edge of symbol_clk_4bit then left shift register will be reflected on the output sampled_4bit.

D. Sample mapper

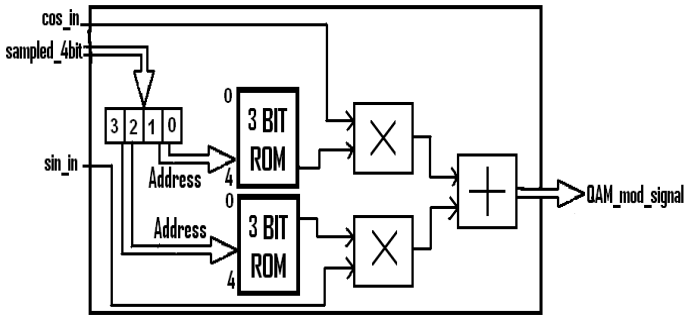

Fig. 5 block diagram of sample mapper

Sampled_4bit data is loaded into a tempary register there 0^{th} bit and 1^{st} bit are assumed as I bits and 2^{nd} and 3^{rd} bit are asumed as Q bits, these I bits and Qbits are assumed as address to 3 bit Rom block's in this according to Rom address data in that address will be given to the next block called as multipler's. I bits are multipled with cos_in bits and Q bits are multipled with sin_in bits than resultant output's of the multipler section will be added which generates the final output as QAM_mod_signal.

E. Symbol demapper

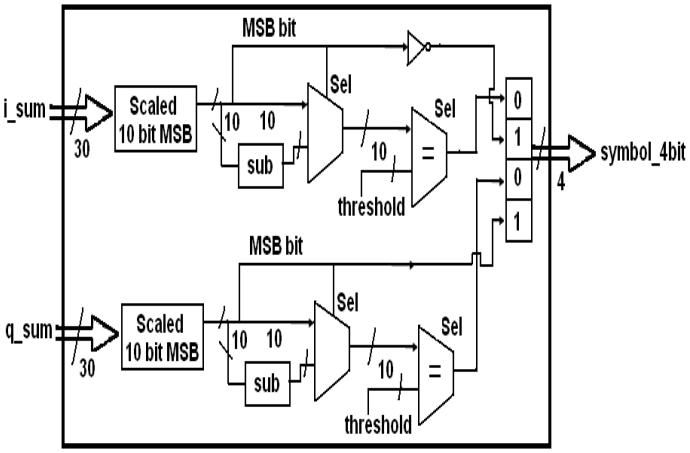

Fig. 6 block diagram of symbol demapper

The input's are I_sum and Q_sum these are trunketed to 10 bits, the MSB of trunckted is used as a select if bit is '1' then output will be same if bit is '0' then output will be negative ot the input. The generated signal is compared with threshold resultant is less then threshold then active high signal is stored in 1^{st} bit of register and 0^{th} bit will be the sel signal value. Same process will be done for I_bits and resultant will be stored in 3^{rd} and 4^{th} bits. the register of 4 bit's will be reflected as symbol_4bit

F. PID controller

PID controller is an important ingredient of a distributed control system. The controllers are also embedded in many special purpose control systems. PID control is often combined with logic, sequential functions, selectors, and simple function blocks to build the complicated automation systems used for energy production, transportation, and manufacturing.

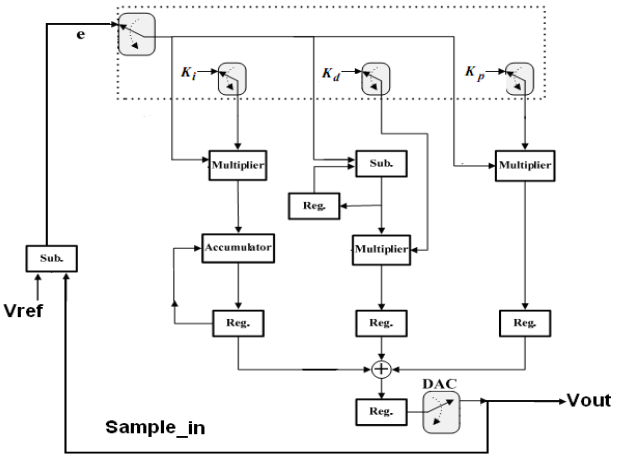

Fig. 7 Block diagram of PID controller

The output of the system is taken as input (i.e sample_in) of PID controller as that is compared with vref to generate error signal. PID controller has three sections that is integration section, differentiation section and proportional section. In Proportional section gain K_p is multiplied by error and produces K_p_prod signal but in integration section accumulation (i.e past error with present error) of the error is multiplied by gain K_i to produce K_i _prod and the subtraction of the past error from present error generated result is multiplied by K_d_prod. Addition of K_i_prod, K_d _prod and K_p_prod generates vout which is given to the system to control by the PID controller.

III. SIMULATION RESULTS

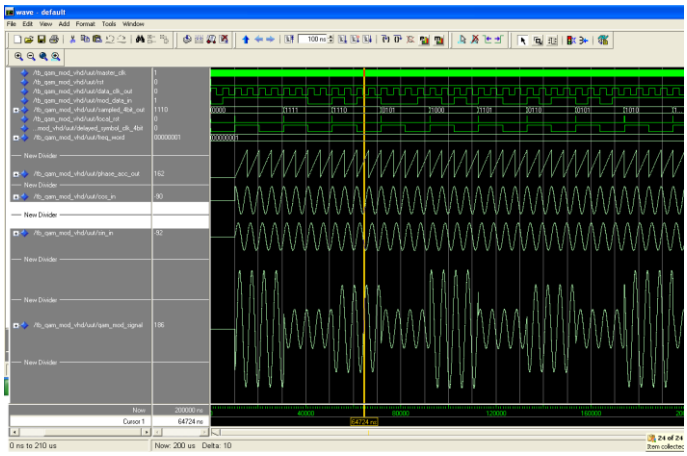

Fig. 8 QAM modulation simulation results

Master_clock is 50MHz clock that is board clock, rst is used to reset QAM modulation module. Data_clk_out is used to collect data from mod_data_in after completing of 4 clk pluses of Data_clk_out resultant will be forced on sampled_4bit_out, delayed_sym_clk_out_4bit is used to generate local_rst this is used to reset phase_acc_out is added with freq_word and updated in phase_acc_out that will be given to cos and sin lut that generates cos_in and sin_in. processing(i.e. multiplication and addition) of combination of cos_in, sin_in and sampled_4bit_out will generate QAM_mod_signal

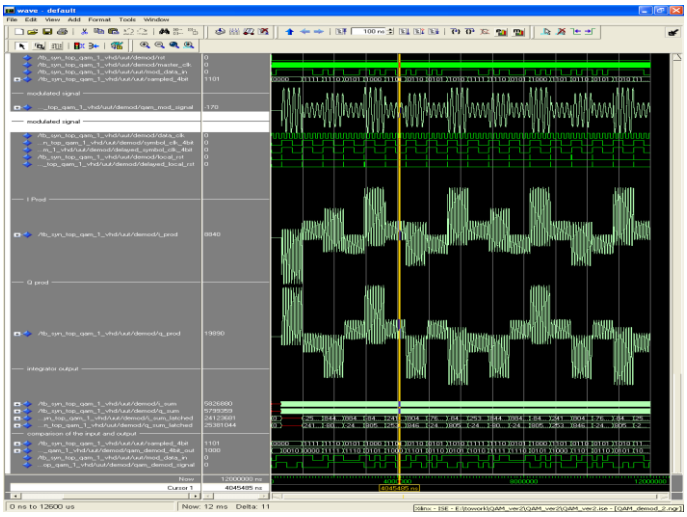

Fig. 9 QAM demodulation simulation results

Here we are showing the QAM modulation and demodulation signals by implementing in vhdl.

IV. SPARTAN 3E

A. Spartan 3E Board

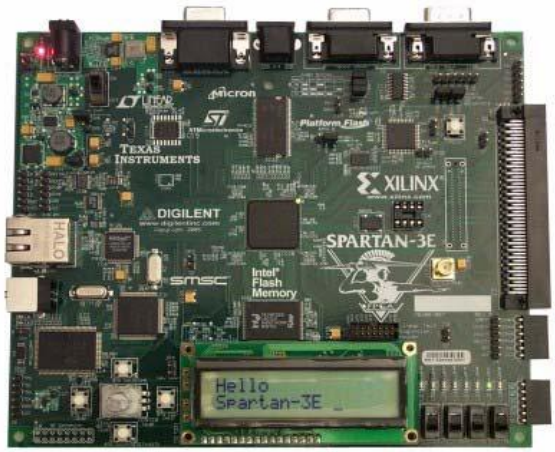

Fig. 10 Spartan 3E board

B. FPGA Structure

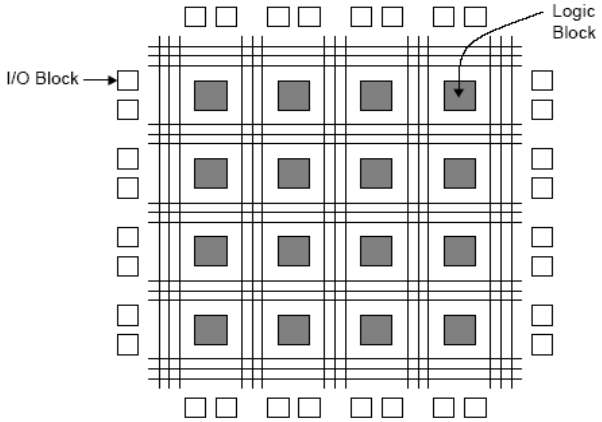

Fig. 11 FPGA structure

V. CHIP SCOPE RESULTS

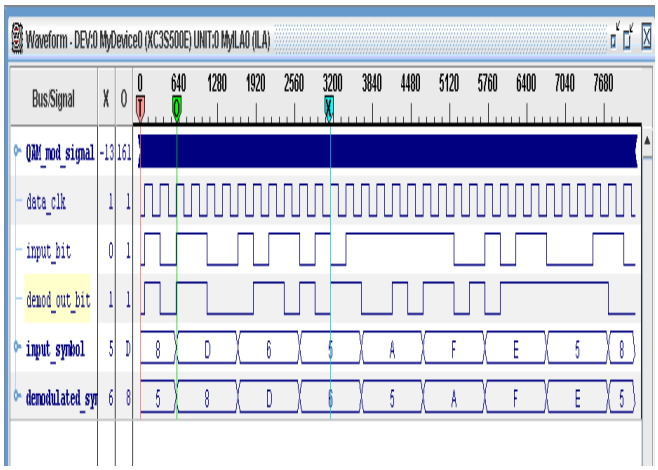

Fig. 12 Chipscope results

VI. TABLE-1

Device Utilization

Logic utilization	used	available	Utilization
Number of slice flipflops	51	9,312	19%
Number of 4 input LUT's	210	9,312	9%
Number of occupied slices	134	4,656	24%
Number of bonded IOB's	19	232	9%
Number of GCLK'S	1	24	4%

VII. CONCLUSION

In this paper we implemented 16-QAM modulator and demodulator on SPARTAN 3E FPGA XC3S500E. The present design is prototyped to Spartan series FPGA. We can scale up the modules for better performance and implement on Virtex series FPGA.

The present technique is designed for co-operative communication type. In future the techniques can be implemented for non-cooperative communication scheme (military applications). This can be extended for implementing 64 QAM, to support later versions of WiMAX.

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