Design and Implementation of Multiband Clock for SOC System

K.Mouna, Dr.B.K.Madhavi

***Abstract*— Generally clock consumes the largest part of total chip power. The different IP blocks on the chip may require multiple-frequency clocks for which multiple clock generators are to be used which increases the area and power consumption of the chip. This paper concentrates on some issues of clock power consumption in system-on-a-chip (SOC) designs. In this paper we developed a single clock multiband network which can supply for multi-clock domain network. A single-phase multi-band clock is developed which can generate multiple clock frequencies using a single clock frequency. The proposed 2/3 prescaler is verified in the design of the proposed multiband clock network. A UART is designed which uses the BIST technique. The UART and the master slave flip-flop are designed to verify the multiband clock network.**

Index Terms*— Clock power consumption, single clock multiband network, system-on-a-chip (SOC).

I. INTRODUCTION

As the IP blocks on a chip increases, their clock frequencies and requirements also becomes more heterogeneous. In some instances different blocks may operate at different clock frequencies. For this reason a multiband clock network is designed to provide multiple clock frequencies through a single clock. This project is highly useful for the communication devices like Bluetooth and Zigbee.

The multiband clock network can divide the input frequency either by 32/33/47/48 based on the control signals 'sel' and 'mod'. In order to verify the multiband network a Universal Asynchronous Transmitter Receiver (UART) and a Master Slave Flip-Flop are designed. The output frequency of multiband network is provided to both the UART and the Master Slave Flip-Flop which acts as its input clock. As the multiband network provides different clock frequencies only one at-a-time, a demux with 'sel' as its selection line is used to provide the clocks to the uart and the master slave flip-flop. The multiband clock network operates at a frequency range of GHz whereas the uart and the master slave flip-flop operate at a frequency range of MHz.

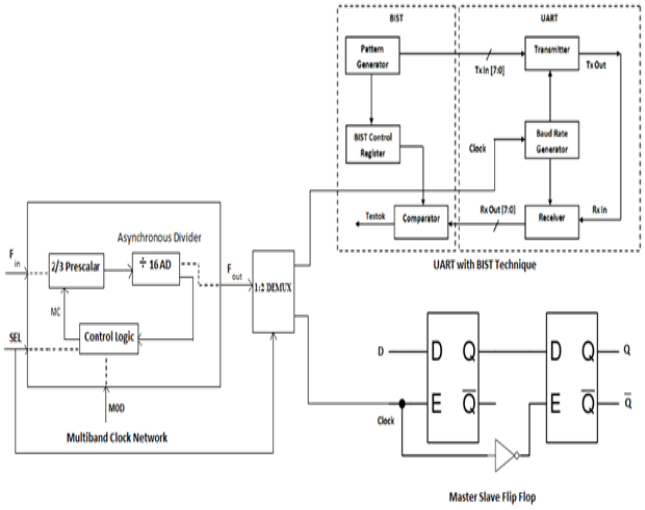

Fig.1 Proposed Multiband Clock for SOC System

Fig 1 represents the proposed multiband clock for SOC system. The proposed single clock multiband network reduces clock jitter. The clock has the highest switching activity when compared to the other input signal to most of the blocks. Due to this activity, it is said to be one of the most power consuming inputs as it consumes almost 70% of the entire power consumed by the IC. Hence when multiple clock generators are replaced by a single clock multiband network, it reduces large amount of power consumption by multiple clock generators.

II. MULTIBAND CLOCK NETWORK

A. 2/3 Prescalar

The conventional TSPC 2/3 prescaler consumes large power and has low operating frequency due to its large load capacitance. An improved speed and low power 2/3 prescaler is proposed in this work which is implemented in TSPC [1] logic. The Fig 2 shows the proposed 2/3 presclar which consists of two D flip-flops and two NOR gates embedded into the flip-flops. The first NOR gate of the proposed 2/3 prescaler is embedded into the third stage of DFF1 and the second NOR gate is embedded into the first stage of DFF2.This reduces the load capacitance and switching power consumption of the proposed 2/3 prescaler.

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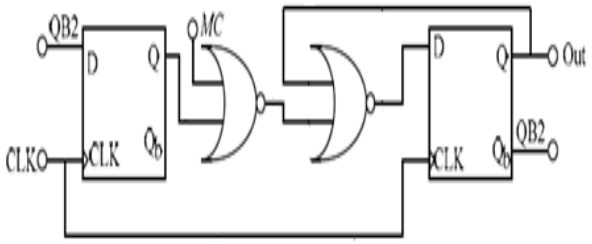

Fig.2 Proposed 2/3 Prescalar

B. *Single Clock Multiband Network*

The multiband clock network shown in Fig 3 consists of a 2/3 prescalar, four asynchronous frequency dividers each divided by 2 (÷16 AD) and some combinational logic circuits (control logic) to achieve multiple division ratios. The circuit has two control signals 'sel' and 'mod'. The 'mod' controls the N/N+1 division and the 'sel' control the switching between 32/33 [2]-[3] and 47/48 modes.

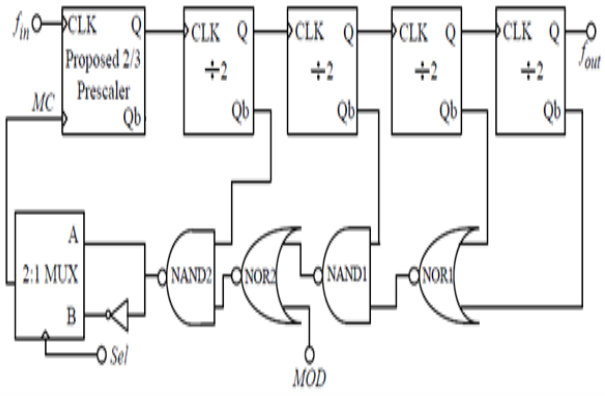

Fig. 3 Multiband Clock Network

Case-I: Sel='0'

When *Sel*='0', the output of the second NAND gate is directly transferred by the 2:1 MUX to the input of 2/3 prescaler as MC. The multiband clock network operates in divided by 32/33 mode, where the logic signal *MOD* controls the division ratio.

If *MOD*='1', the multiband clock network acts as ÷32. If we denote the 2/3 prescaler as *M/M+1* and the four asynchronous dividers whose division ratio equal to 16 by '*AD*', the division ratio in this mode (*MOD*='1', *Sel*='0') is given by

$$F_{32} = [(AD - \overline{MOD}) \times M] + [\overline{MOD} \times (M+1)] = [(16-0) \times 2] + [0 \times (2+1)] = 32$$

If *MOD*='0', the multiband clock network acts as ÷33 .The division ratio in this mode (*MOD*='0', *Sel*='0') is given by

$$F_{33} = [(AD - \overline{MOD}) \times M] + [\overline{MOD} \times (M+1)] = [(16-1) \times 2] + [1 \times (2+1)] = 33$$

Case-II: Sel='1'

When *Sel*='1', the inverted output from the second NAND gate is transferred by the 2:1 MUX to the input of 2/3 prescaler as MC. The multiband clock network operates in divided by 47/48 mode, where the logic signal *MOD* controls the division ratio. Here, when *MC*='0', the wide-band 2/3 prescaler operates in the ÷2 mode and when *MC*='1', the 2/3 prescaler operates in the ÷3 mode.

If *MOD*='1', the prescaler acts as ÷48. If we denote the wide-band 2/3 prescaler as *M/M+1* and the four synchronous dividers whose division ratio equal to 16 by '*AD*', the division ratio in this mode (*MOD*='1', *Sel*='1') is given by

$$F_{48} = [(AD - \overline{MOD}) \times (M+1)] + [\overline{MOD} \times M] = [(16-0) \times (2+1)] + [0 \times 2] = 48$$

If *MOD*='0', the prescaler acts as ÷47.The division ratio in this mode (*MOD*='0', *Sel*='1') is given by

$$F_{47} = [(AD - \overline{MOD}) \times (M+1)] + [\overline{MOD} \times M] = [(16-1) \times (2+1)] + [1 \times 2] = 47$$

Table 2: Proposed Multiband Network Division Ratios

SEL	MOD	Fout
0	0	Fin/33
0	1	Fin/32
1	0	Fin/47
1	1	Fin/48

III. UART WITH BIST TECHNIQUE

The Universal Asynchronous Receiver Transmitter (UART) transmits or receives data from one device to another. The division of frequencies is mainly required in communication purposes. Hence a uart which is communication device is chosen for verifying the multiband network. The uart can act either as a transmitter or a receiver. In order for the data to be transmitted, the clock frequencies of both the transmitter and the receiver have to match.

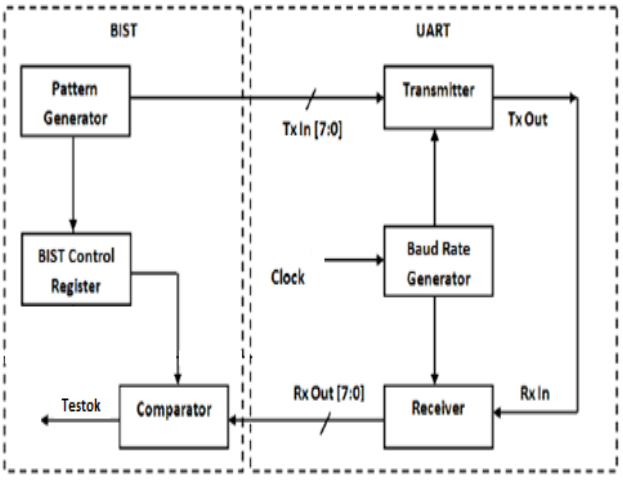

Fig. 4 UART with BIST Technique

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Table 1: Data Framing

Bit No.	1	2	3	4	5	6	7	8	9	10	11
	Start Bit	8 data bits								Stop Bits	
	Start	D 0	D 1	D 2	D 3	D 4	D 5	D 6	D 7	Stop	

Generally 8 bit data is transmitted through the uart [4]-[5]. A start and a stop bit are added along with the data transmitted. The baud rate generator indicates the number of bits transmitted per second which is set to 9600bps. The start bit indicates that a new character is coming. The data is sent next to the start bit. If a parity bit is used, it would be placed after all of the data bits. The last bit is always marked as logic high which is the stop bit. It signals the receiver that the character is completed. Since the start bit is logic low (0) and the stop bit is logic high (1) there are always at least two guaranteed signal changes between characters.

The Fig 4 shows the uart with the bist architecture. The UART operates at a frequency range of MHz. The Built-in-self-test (BIST) allows efficient test coverage [6]. A properly designed BIST is able to offset the cost of added test hardware while at the same time ensuring the reliability, testability and reduces maintenance cost. The Pattern generator generates different data patterns which are sent to the transmitter. The transmitter transmits the data to the receiver when the transmit signal is high. The comparator compares the received data to the data stored in the register. The testok low indicates mismatch of data at transmitter and receiver. The testok high indicates the transmitted and the received data are the same.

IV. Master Slave Flip-Flop

The Master-slave flip flop is designed using two separate D flip flops out of which, one acts as the master and the other as a slave. The master-slave flip-flop eliminates all the timing problems by using two flip-flops connected together in a series configuration. The first flip-flop is the “Master” circuit and it triggers on the falling edge of the clock pulse. The other fkip flop is the “Slave” circuit and it triggers on the leading edge of the clock pulse. This results in the two sections, the master section and the slave section. The two sections are enabled during opposite half-cycles of the clock signal.

The Master Slave D Flip-Flop shown in Fig 5 operates at a frequency range of MHz. In the master slave flip flop, two gated flip-flops are connected in series and the master has an inverted clock pulse [7]. The output Q from the output of the “Master” flip flop is connected to the input of the “Slave” flip flop. The Q output of the slave flip flop is considered to be the output of the master slave flip flop and will be same as the D input with respect to the pos-edge clock.

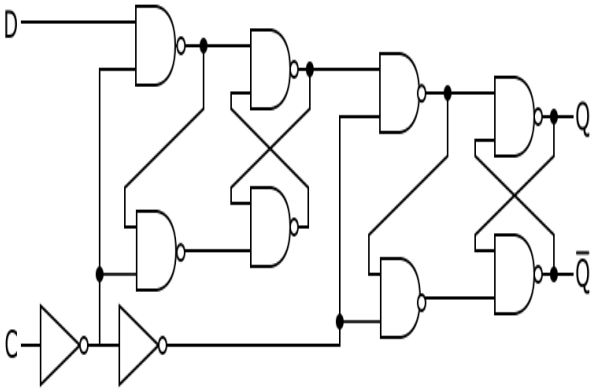

Fig. 5 Master Slave D Flip-Flop

For a positive-edge triggered master–slave D flip-flop, when the clock signal is low (logical 0) the "enable" seen by the first or "master" D latch (the inverted clock signal) is high (logical 1). This allows the "master" latch to store the input value when the clock signal transitions from low to high. As the clock signal goes high (0 to 1) the inverted "enable" of the first latch goes low (1 to 0) and the value seen at the input to the master latch is "locked". Nearly simultaneously, the twice inverted "enable" of the second or "slave" D latch [8] transitions from low to high (0 to 1) with the clock signal. This allows the signal captured at the rising edge of the clock by the now "locked" master latch to pass through the "slave" latch. When the clock signal returns to low (1 to 0), the output of the "slave" latch is "locked", and the value seen at the last rising edge of the clock is held while the "master" latch begins to accept new values in preparation for the next rising clock edge.

V. Results

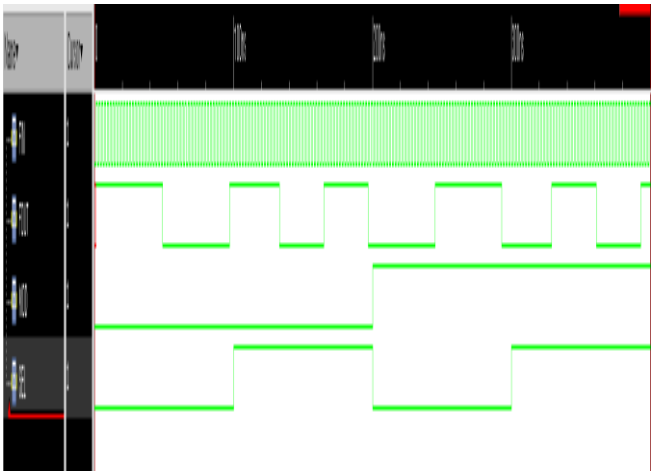

Fig. 6 Simulated Output of the Proposed Multiband Clock Network

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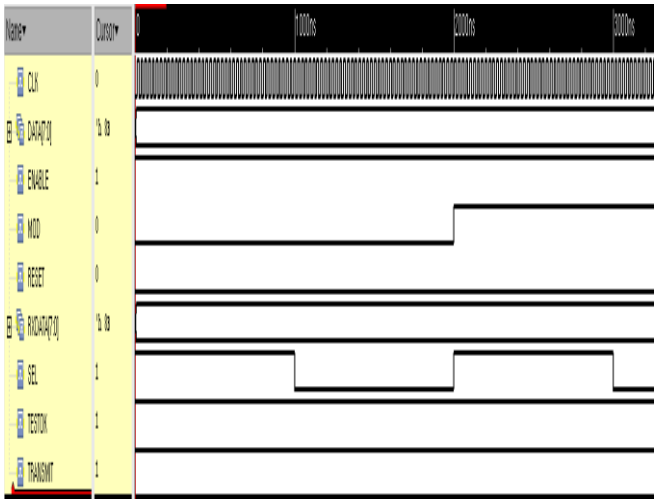

Fig. 7 Simulated Output of Multiband Clock Connected to UART with BIST Technique

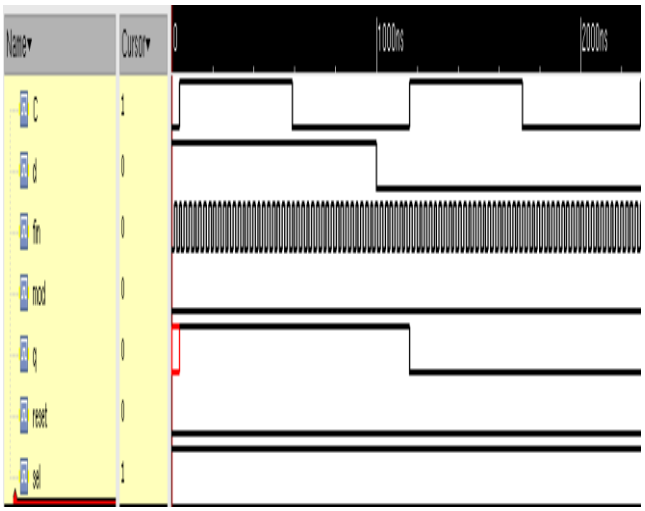

Fig. 8 Simulated Output of Multiband Clock Connected to Master Slave D Flip Flop

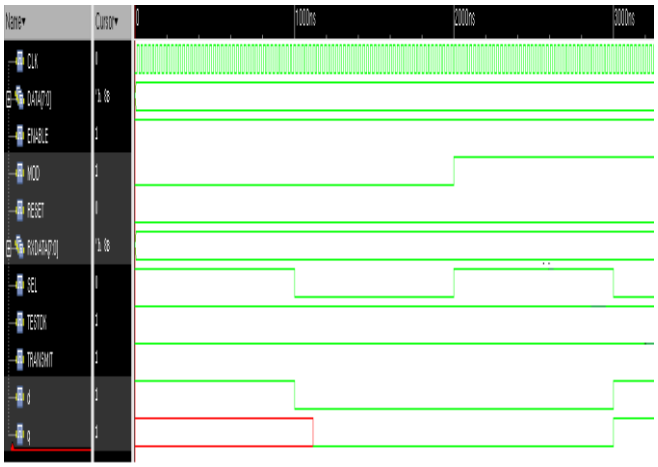

Fig. 9 Simulated Output of Multiband Clock Connected to both UART and Master Slave Flip-Flop

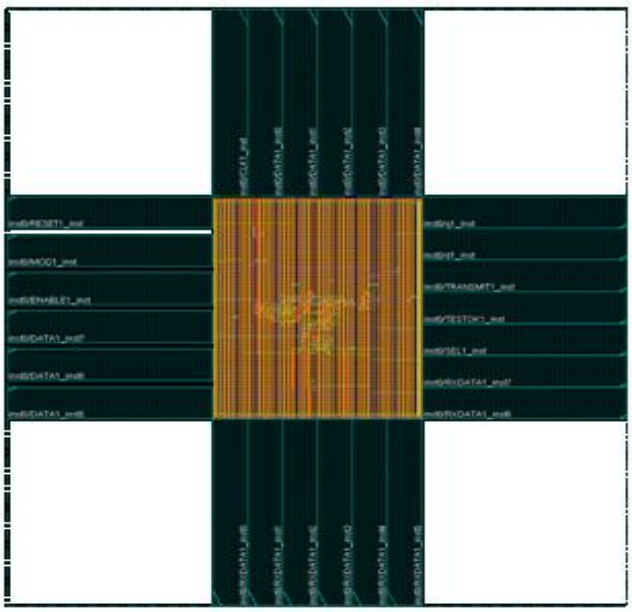

Fig. 10: SOC Output

Table 3: Power Report of the Multiband Clock for SOC System

Leakage Power (µW)	**Dynamic Power (µW)**	**Total Power (µW)**
4.286	5772.624	5776.910

VI. CONCLUSION

The multiband clock network for SOC system is designed and implemented in Cadence SOC Encounter. The proposed multi-band clock network reduces clock jitter. The developed clock is supplied to the uart and the master slave flip-flop and the output of each block is simulated and synthesized. The results are verified and the power analysis is performed using RTL.

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