Implementation of Maximum Likelihood Based Alamouti Space Time Block Coded (STBC) MIMO System for Reliable Communication

Nuzhath Farhana, Ramadurgam Basavaraju

Abstract— Realization of multi input and multi output (MIMO) [1] systems is highly essential for Wimax networks. Space–time block coding is a technique used in wireless communications to transmit multiple copies of a data stream across a number of antennas and to exploit the various received versions of the data to improve the reliability of data-transfer. In wireless communications the transmitted signal must traverse a potentially difficult environment with scattering, reflection, refraction and so on and may then be further corrupted by thermal noise. In the receiver STBC [2] redundancy results in a higher chance of being able to use one or more of the received copies to correctly decode the received signal. The space–time coding combines all the copies of the received signal in an optimal way to extract as much information from each of them as possible.

In this project a computationally efficient algorithm for space time block decoding will be implemented for FPGA based applications. The VHDL will be used for realization of the decoding algorithm and other communication blocks. The decoding algorithm will be computationally efficient extension of the maximum likelihood algorithm. The new algorithm results in more than 50% reduction in the computational complexity.

The algorithm will be realized for BPSK modulation scheme. The STBC encoder will also be realized which generates the required appropriate codes for decoder. The work involves implementation of STBC encoder, modulators, demodulators and STBC decoders. Various sub blocks such as SIN/COS generators, multipliers, adders, encoding look up tables, complex arithmetic units etc. These blocks will be realized in generic style to ensure scalability and reconfigurability of the STBC decoder design.

Modelsim xilinx edition (MXE) tool will be used for simulation and functional verification. Xilinx Synthesis technology (XST) will be used for FPGA synthesis. Timing analysis will be carried out to predict the maximum achievable clock speeds for chosen Xilinx Spartan 3E FPGA device.

***Index Terms*—STBC, MIMO, Modelsim, Xilinx, FPGA, VHDL.**

I. INTRODUCTION

A. Multi- input Multi output (MIMO)[3]:

In radio, multiple-input and multiple-output, or MIMO is the use of multiple antennas at both the transmitter and receiver to improve communication performance. It is one of several forms of smart antenna technology. Note that the terms input and output refer to the radio channel carrying the signal, not to the devices having antennas.

MIMO technology has attracted attention in wireless communications, because it offers significant increases in data throughput and link range without additional bandwidth or transmit power. It achieves this by higher spectral efficiency (more bits per second per hertz of bandwidth) and link reliability or diversity (reduced fading). Because of these properties, MIMO is an important part of modern wireless communication standards such as IEEE 802.11n (Wifi), 4G, 3GPP Long Term Evolution, WiMAX and HSPA+.

B. Space time block coding (STBC)[4]:

It is a technique used in wireless communications to transmit multiple copies of a data stream across a number of antennas and to exploit the various received versions of the data to improve the reliability of data-transfer. The fact that transmitted data must traverse a potentially difficult environment with scattering, reflection, refraction and so on and, as well as, be corrupted by thermal noise in the receiver means that some of the received copies of the data will be "better" than others. This redundancy results in a higher chance of being able to use one or more of the received copies of the data to correctly decode the received signal. In fact, STBC combines all the copies of the received signals in an optimal way to extract as much information from each of them as possible.

II. IMPLEMENTATION OF BLOCK DIAGRAM

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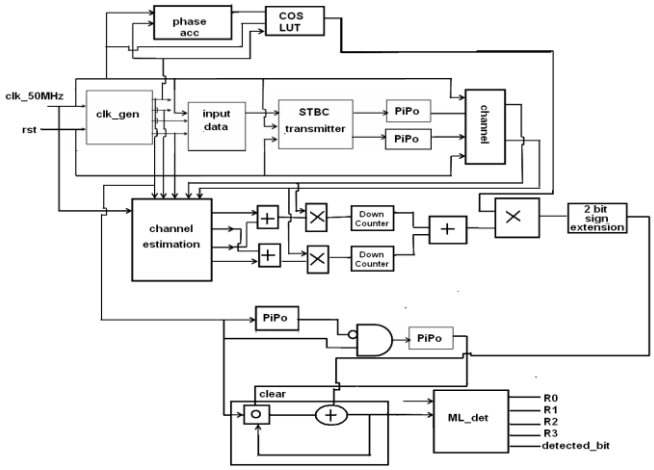

Fig. 1 block diagram

A. Clock generator module

The inputs for the clock generation module is reset and master clock of 50Mhz and the outputs are sample clock, data bit clock, frame clock and symbol clock. The sample clock is same as the master clock. The clock generation module consists of 12 bit counter. In the counter 6^{th} bit value gives the output of data bit clock and symbol clock and the 12^{th} gives the output of frame clock. The data bit clock and the symbol clock takes 128 pulses to complete one cycle and the frame clock requires 4096 pulses to have one complete cycle. The symbol clock, frame clock and sample clock are given as inputs to channel estimator, the symbol clock and frame clock are given as inputs to the input data generation module, the symbol clock to the ML detector.

B. Input data generator

The inputs to the input data generation module is reset, symbol clock and frame clock and the output is data bits. This module consists of 5-bit up counter, ROM. The 5-bit up counter increments by one bit when the frame sync is 0 and the symbol clock is 1 and this incremented value will be given to the ROM to read as address and the ROM gives the data bits as output. This data bits are given as input the transmitter.

C. ML detector section

The reset, symbol clock and channel sum latched are the inputs and the r0out, r1out, s0_out, s1_out, detected bit are the outputs. The channel sum latched is the 16 bit register. The r1_temp is the 17 bit register and these bits are taken from channel sum latched which contains 16 bits and the 17^{th} bit is the signed extension of the channel sum latched 16th bit. The r1_1 contains four bits and these bits are r1_temp MSB four bits. The r1out is cleared when r1_1 contains 1111 else r1out is same as r1_1 and the r0_out is same as r1_out. The r0_out and r1_out are summed to give s0_est and r0_out the r1_out are subtracted to give s1_est. The s0_bit is 1 when the msb bit of s0_est is 0 otherwise s0_bit is 0 and similarly s1_bit can also be found. When the STBC receiver state is 0 then the s0_bit will be sent as detected bit and STBC receiver state is 1 then s1_bit will be sent as the detected bit.

D. Channel estimation

The inputs are reset, symbol clock, sample clock, frame clock, receiver 1_in, recevier2_in and the outputs are h01, h02, h11, h22. To get the delayed frame clocks by one clock cycle delay we are using pipo registers. The frame clock is delayed by one clock cycle to get temp, temp is delayed by one clock cycle to get frame clock delayed, frame clock delayed is delayed by one clock cycle to get frame clock delayed2, frame clock delayed2 is delayed by one clock cycle to get frame clock delayed3, these are done by using pipo registers. The frame clock and not of frame clock delayed2 are added to get the output signal frame sync_ant1 and similarly the frame clock delayed2 and not of frame clock delayed3 are added to get the output signal frame sync_ant0. The signal acc_reset1 is achieved by using frame sync_ant1 and not of delayed frame sync_ant1, delayed frame sync_ant1 is calculated by using pipo register and similarly the signal acc_reset0 is achieved by using frame sync_ant0 and not of delayed frame sync_ant0, delayed frame sync_ant0 is calculated by using one more pipo register.

To estimate the channel estimation parameters first we have to extend the receiver1_in as receiver1_in_ext which is extended to 16 bits by using signed extension msb bit and similarly for receiver2_in is extended to receiver2_in_ext. The abs_receiver1_icn is calculated by using receiver1_in_ext, when receiver1_in_ext msb bit is 0, abs_receiver1_in is same as receiver1_in_ext else abs_receiver1_in is signed negative value of receiver1_in_ext, as it follows for the receiver2_in_ext. By calculating the receiver1_ext, we can find the values of abs_receiver01_in_sum and scaled_abs_receiver01_in_sum. The absolute sum of cosine can be calculated from matlab i.e., 1262. By using divider core we will calculate h01. In the same way we are going to find h02, h11, h12.

E. Channel module

The predefined random noise is multiplied to antenna signal (i.e. ant0_in and ant1_in) to make signal more practical as it passed to channel, ant0_in is multiplied by rand1 and rand2 and resultant signals are mul01 and mul02 respectively and ant1_in is multiplied by rand3 and rand4 and resultant signals are mul11 and mul12 respectively. Mul11and mul01 are added to get the output signal rec1 and Mul02 and mul12 are added to get the output signal rec2.

F. STBC [5] Transmitter

The inputs are reset, master clock, data bit and outputs are ant0_out and ant1_out. The data bit is given to symbol mapper that will convert data bit to i_sym and q_sym these output's will be shifted to pipo block so that with the same clock the data is processed to next state, STBC state is used as a select pin to S block it works as a multiplexer according to

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select bit the operation will be selected and generates the signals selected i_sym_ant0. Using the phase increment word the phase accumulator section generates address to the LUT_cos and lut_sin generates the amplitude according to address amplitude signals will be supplied to the multiplier blocks for further process. Frame clock is used to generate the enable signals to the multiplier section this is shown in above figure

When the enable signal is given by frame sync_ant0 then multiplier will perform the multiply operation on inputs and result of both multiply section will be given to adder section that will generate output signal's ant0_out and with the same process but the enable signal is given from frame sync_ant1 will be used for other section to generate the output ant1_out.

III. Simulation Results

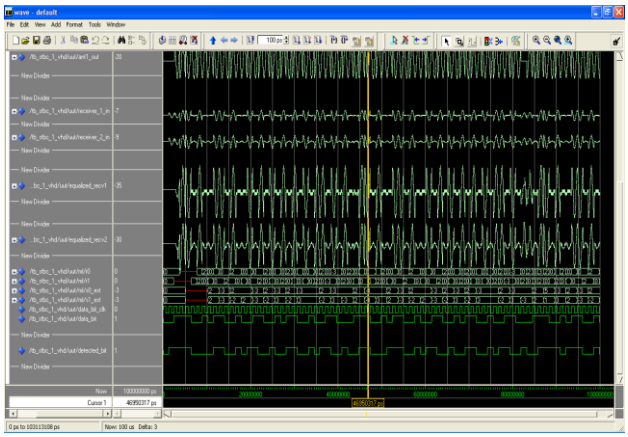

Fig. 2 simulation results

IV. SPARTAN 3E

A. *Spartan 3E Board*

Fig. 3 Spartan 3E board

B. *FPGA Structure*

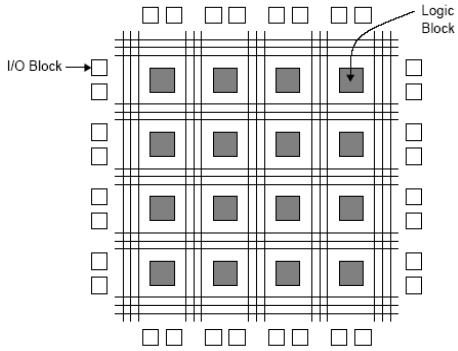

Fig. 3 FPGA structure

V. Chip Scope Results

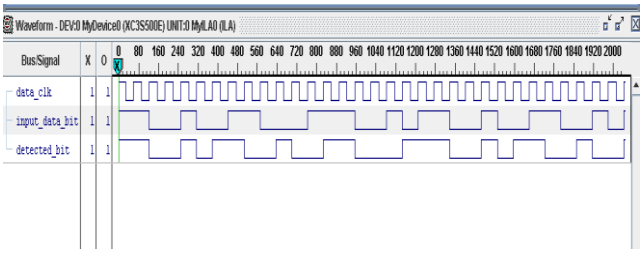

Fig. 3 chipscope results

VI. Table

A. *Device Utilization*

Logic utilization	used	available	utilization
Number of slice flipflops	1,861	9,312	19%
Number of 4 input LUT's	919	9,312	9%
Number of occupied slices	1,144	4,656	24%
Number of bonded IOB's	23	232	9%
Number of block RAM's	4	20	20%

VII. Conclusion

In this project Alamouti STBC transmission is shown to be in upper bound for transmitting data through communication channel with respect to combating fading and transmission loss. The STBC encoding allows us to get Space wise (by multi transmitting antennas) and Time wise (corresponding to different transmitting times) encoding of blocks of data to be transmitted, by which reliability of data transmission is provided, the fundamental need of communication system.

In MIMO[6] with STBC when selecting the number of transmit/receive antennas, several practical considerations must be taken into account as under strict delay constraints, achieving high diversity gains (i.e. high reliability) becomes critical in order to minimize the need for retransmissions.

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Since transmit/receive diversity gains experience diminishing returns as their numbers increase, complexity considerations dictate the use of small antenna arrays (typically no more than 4 antennas at each end).

By providing mechanisms in reducing the setup costs and power consumption by multiple antennas in MIMO system and by combating above stated problems with latest technologies in communication system, we can effectively provide the reliable communication with less increased complexity.

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Nuzhath Farhana is presently pursuing final semester M. Tech in VLSI System Design at Aurora's Technological and Research Institute.

Ramadurgam Basavaraju is presently working as Assistant Professor at Aurora's Technological and Research Institute.

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