FPGA Realization of Gaussian Pulse Shaped QPSK Modulator

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***Abstract*— In past few years, a major transition from analog to digital modulation techniques has occurred and it can be seen in all areas of satellite communications systems, cellular and wireless. Modulation is essential in transmitting as two or more signals are sent at a time and modulation avoids interference between the signals and also ensure that errors are avoided during transmission. In order to transmit them over long distances, different modulation scheme have been used. For digital modulation, instead of varying the amplitude or the frequency of the carrier signal, it is preferred to vary the phase because it offers better protection in transmitting signals.**

QPSK (Quadrature Phase Shift Keying) modulation which is a simple but very robust form of digital modulation. The QPSK modulation conveys 2 bits per symbol and it is very popular in satellite communication. The modulating signal is generated internally by a LFSR and is divided into two sequences: the odd-sequence for the I-channel and the even-sequence for the Q-channel. The sine and cosine waveform are generated outside the FPGA. The QPSK modulated signal is obtained by adding two modulated signals. The same principle is applied in implementing the modulator on the board, with the difference that the sine and cosine signals were generated inside the board.

***Index Terms* — QPSK, VHDL, FPGA, MATLAB.**

I. INTRODUCTION

Modulation is the process of sending data signal over carrier signal to minimize the noise or fading effect. They are mainly divided into two categories i.e., analog and digital. In analog modulation carrier signal is modulated with the help of analog data signal and in digital it modulates with digital signal. Digital modulation is called shift keying because in this, the carrier signal is shifted in amplitude, frequency or phase by digital input signal. Different PSKs can be obtained by M-ary PSK, where M is the number of states or number of phase shifts which depend upon the number of signals that are combined for modulation.

In QPSK two signals are combined for modulation. BER of QPSK is better than higher order PSK signals such as 8-PSK, 16-QAM, 32-QAM etc. which are easily affected by noise. At higher order PSK, larger bandwidth is require for higher data transfer rate and consume more power, whereas QPSK is more bandwidth as well as power efficient. There are many applications where QPSK modulator is used, out of which few are of battery operated devices such as Bluetooth, TDMA cellular communication, Medical Implant Communication Services (MICS) etc. Therefore it is necessary to minimize the power consumption of these devices so that the battery will last for longer time. It can be reduced by reducing size of circuit or reducing the speed of operation. Digital devices are becoming smaller in size, hence considering this issue the lower size modulator is designed, which provides same output as conventional modulator.

II. CONVENTIONAL MODULATOR

A. The model of QPSK

The QPSK modulator can modulate two signals in same frequency band as shown in fig. 1. Each signal is to be converted from analog to digital, then modulate one signal with sine and another with cosine which gives four different
Phase shifts with two signals, by adding these two phase shifted signals we get QPSK output signal [1].
The QPSK signal can be given as

$$S_{QPSK} = \sqrt{\frac{2Es}{Ts}} \cos\left(2\pi f_c t + (i-1)\frac{\pi}{2} \right) \quad \text{for} \quad i = 1, 2, 3, 4 \tag{1}$$

Where, $\sqrt{\frac{2Es}{Ts}}$ = Constant amplitude with Es energy and Ts time period of the signal

fc= Frequency of carrier signal

i = phase no. of signal as per the symbols of the data signal from the trigonometric equation given below,

$$\text{Cos}\,(A+B) = \cos(A)\cos(B) - \sin(A)\sin(B) \tag{2}$$

Fig. 1. Shows that separate sine and cosine waves are generated which require two ROM's to store these signals [2]. This is then modulated by the input binary data signal. These two signals are then added to generate the QPSK signal. All these process is discuss in [5] with design flow diagram.

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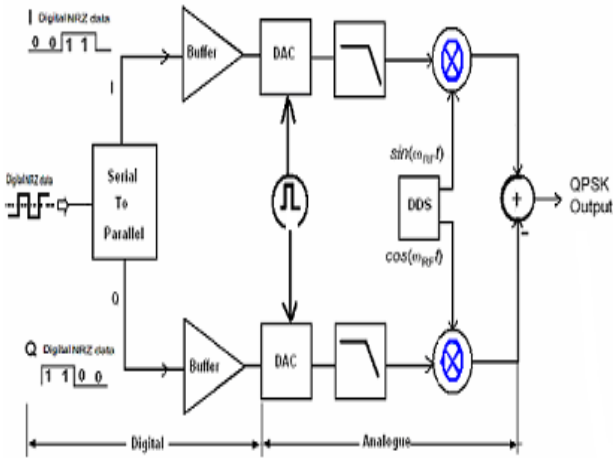

Fig. 1 Conventional QPSK Modulator

From eq. (2) we can write

$$S_{QPSK} = \sqrt{\frac{2Es}{Ts}}\cos(2\pi f_c t)\cos[(i-1)\frac{\pi}{2}] - \sqrt{\frac{2Es}{Ts}}\sin(2\pi f_c t)\sin[(i-1)\frac{\pi}{2}]$$

B. *Mathematical equation of QPSK Modulator*

The QPSK signal can be given as

$$S_{QPSK} = \sqrt{\frac{2Es}{Ts}}\cos(2\pi f_c t + (2i-1)\pi/4) \quad \text{for i = 1, 2, 3, 4}$$

Where, , $\sqrt{\frac{2Es}{Ts}}$ = Constant amplitude with Es energy and Ts time period of the signal

fc= Frequency of carrier signal

i = phase no. of signal as per the symbols of the data signal from the trigonometric equation given below,

cos(A+B) = cos(A)cos(B) - sin(A)sin(B)

$$S_{QPSK} = \sqrt{\frac{2Es}{Ts}}\cos(2\pi f_c t)\cos[(i-1)\frac{\pi}{2}] - \sqrt{\frac{2Es}{Ts}}\sin(2\pi f_c t)\sin[(i-1)\frac{\pi}{2}] \quad (3)$$

There are two signals in QPSK signal i.e. in phase I(t) and Quadrature phase Q(t). This is given in eq. (3) Can be Written as

$$S_{QPSK} = \sqrt{\frac{2}{Ts}}\cos(2\pi f_c t)\, I(t) - \sqrt{\frac{2}{Ts}}\sin(2\pi f_c t)\, Q(t)$$

where,

$$I(t) = \sqrt{Es}\cos[(i-1)\frac{\pi}{2}] \quad \text{and} \quad Q(t) = \sqrt{Es}\sin[(i-1)\frac{\pi}{2}]$$

Output QPSK waveform with four different phase shifts is as shown in fig. 2. In this, we can see that for each symbol phase angle of original signal is different.

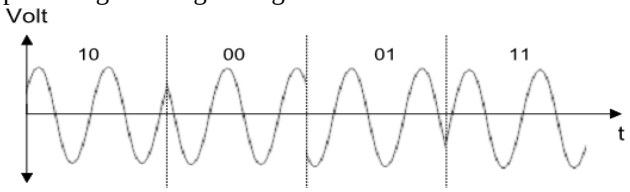

Fig. 2 Output waveform of QPSK modulator i.e., SQPSK

III PROPOSED DESIGN

A. *Implementation*

The proposed architecture focuses on the hardware multiplexing technique, where the hardware can be efficiently shared and utilized between different operations. This in turn leads to reduced area and power consumption at a reasonable data rate. By integrating several of modulation schemes in one common structure, and reusing the hardware for different standards one can minimize the amount of program memory in the processor, can save valuable development time, and reduce the development costs. However in a reprogrammable multi-standard baseband processor, hardware multiplexing can often achieve comparable power consumption and lower silicon area than a fixed function circuit [1].

The architecture of the proposed programmable multi-standard baseband processor using hardware multiplexing technique is as depicted in Figure 3

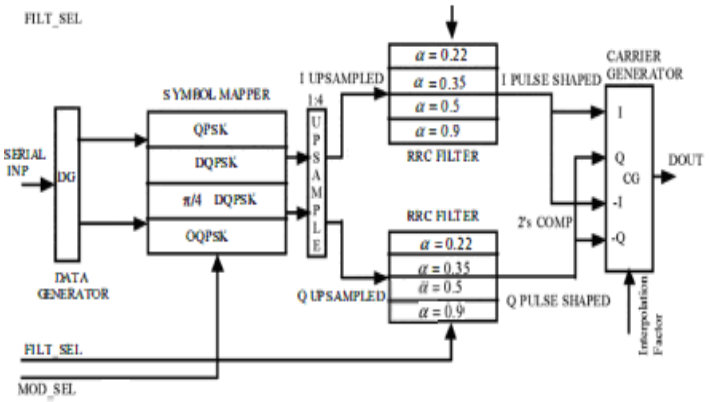

Fig. 3 Proposed Block diagram

The key component of the multi-standard baseband processor, as shown in Figure 3 includes the (A) serial to parallel converter (shown as DG), (B) symbol mapper, (C) Up sampler, (D) root raised cosine filter as a pulse shaping filter, and (E) Carrier Generator (shown as CG) block.

A data generator (DG):

A dummy data acquisition module accepts the digitized data from the Analog to Digital Converter (ADC) and then passes through a serial to parallel converter for dividing the incoming message bit stream into the even and odd bit stream. To accommodate the OQPSK scheme a delay of one bit period has been placed in the quadrature data stream path.

A. *Symbol Mapper*

Symbol Mapper block contains the four different IQ mapper blocks for four different modulation schemes for generating the carrier signal. It takes the even and the odd bit stream from the data generator block and generates a stream of mapped I and Q bit streams each of 3-bit length. The symbol

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mapper block consists of four blocks described below which can be chosen by the MOD _ SEL parameter.

B. Up sampler

Up sampler block takes the mapped data stream input from the previous block and will generate the up sampled I and Q data by a factor of 4. This up sampler block consists of ,a chain of registers connected serially which acts as a shift register. The seven prior symbols are loaded into the shift register and generate the addresses for the RRC filter.

C .Filter

The FIR filter is standard linear convolution, which described the output as convolution of input and impulse response of the filter.

$$y[n] = x[n]*c[n] = \sum_{k} x[k]c[n-k] = \sum_{k} c[k]x[n-k].$$

Where c[n] values represent filter coefficients, and x[n] represents the input samples. The following figure shows the direct form FIR structure.

D.Carrier Generation

The basic block diagram of DDFS implemented is shown in the below Figure. All the blocks are connected with common clock and reset signals. The delta phase value decides the phase increment for each clock pulse. Hence decides the resulting signal frequency. The Frequency modulating instantaneous value is added to the delta phase value which causes instantaneous change in frequency. Due to the digital nature of the modulator only at each clock tick the modulating signal value shall affect the resulting frequency. If the modulating signal is analog then an Analog Digital converter must be used to digitize the modulating signal which can be used in DDFS.

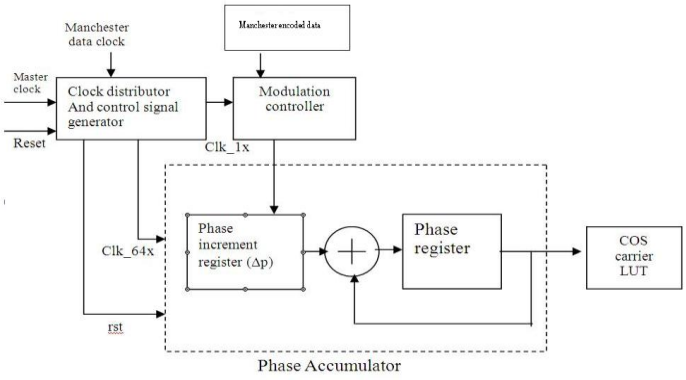

Fig 4. Direct digital synthesizer for Carrier generation

The phase accumulator produces accumulated phase value for each clock pulse. In case if the DDFS is used for phase modulation then instantaneous phase modulating signal value is added to the phase output of phase accumulator. This resulting phase value is given to the four look up tables. Each look up table is configured to produce a specific waveform. The logic used to generate the look up tables is discussed in the further sections.

In three modulation schemes if modulating signal is analog in nature then an appropriate analog to digital converter is required to convert into 8 bit digital output.

The Parallel in Parallel Out shift register cells are required in phase accumulator block to hold frequency and phase values. Synchronization is required between the phase increment register and phase register. This is achieved by connecting a common clock signal. Generic is used in VHDL implementation which allows to instantiate the PIPO component any bit size

IV FPGA BASED IMPLEMENTATION

The proposed architecture shows the Gaussian pulse shaped QPSK modulator which mapping of pulse shaped QPSK. Mainly based on constellation diagram we can map to corresponding phase nothing but QPSK modulating signal.

This block accepts the even and odd bit stream and generates a phase of the current bit sequence according to the TABLE I which causes the carrier to shift by 90° or 180°. The shift in the carrier generates the symbols belonging to the set {-I, 0, I} for both I and Q data streams. The block diagram of the QPSK mapper shows

TABLE I

Input di bit 0?t?T	Phase of QPSK signal (radians)	Coordinates of message points S_i1 S_i2	
10	π/4	+√E/2	-√E/2
00	3π/4	-√E/2	-√E/2
01	5π/4	-√E/2	+√E/2
11	7π/4	+√E/2	+√E/2

This block accepts the even and odd bit stream and generates a phase of the current bit sequence according to the TABLE I which causes the carrier to shift by 90° or 180°. The shift in the carrier generates the symbols belonging to the set {-I, 0, I} for both I and Q data streams. The block diagram of the QPSK mapper block is as shown in Figure. By this way we can generate Pulse shaped QPSK.

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TABLE II

Information bits		Phase shift(radians)
I	Q	
0	0	0
0	1	Π/2
1	0	Π
1	1	3Π/2

V. RESULTS

A.VHDL programming code simulation

The QPSK Modulator implemented on the Spartan 3E Starter Kit board [5] has, as a model, to implement in System Generator. The only difference is that the sine and cosine signals are generated internal, in a ROM. The experimental setup consists of a computer, a Spartan 3E board and an oscilloscope. The ISE Web Pack [6] runs on the computer and it programs the Spartan 3E board.

The simulation of Pulse Shaped QPSK which consists of Pulse shaped Qpsk with RRC filtered output.

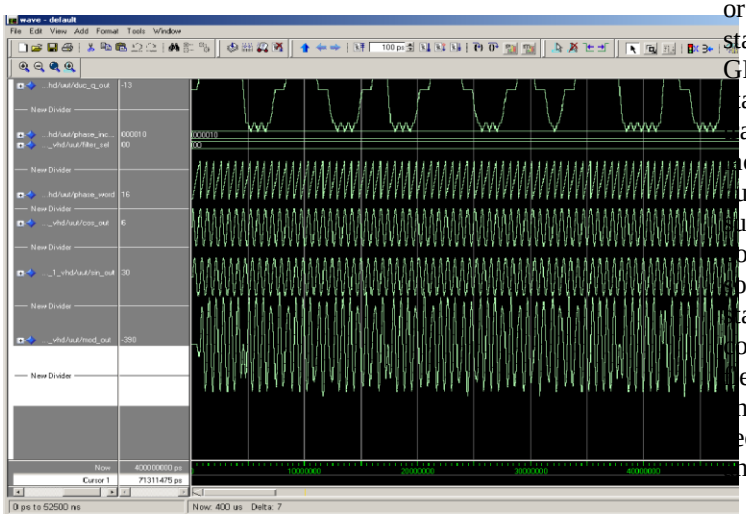

Fig 5. Simulation results of model

The proposed modulator was built by the Xilinx Spartan3E development kit board [8], programmed with the VHDL language for modeling, design and analysis of the proposed QPSK modulator. The simulated result of this modulator is presented in Fig 5. This demonstrates the output signals waveforms indicating the transitions (180°, 270°) of the carrier signal influence by input data signal. The carrier frequency 12.5 MHz was generated from the local clock signal on the board, which operates at 50 MHz. The data signal was reduced to 1.36 MHz by a frequency divider. (behavioral described).The modulator was implemented and comparing two different designs structural and behavior descriptions; for efficient performance. The generated VHDL "Behavioral" block diagram of the QPSK modulator.

TABLE III

LOGIC UNIT	USED	AVAILABLE
Number of slices	3408	4656
Number of Slice Flip Flops's	1193	9312
Number of 4 input LUTs	5909	9312
Number of bonded IOB'S	20	232

VI APPLICATIONS OF QPSK

In today's scenario there are several mobile handsets or wireless communication systems to support various existing standards like digital wireless communication standards (GSM, GPRS, HSPDA, WCDMA, UMTS, etc.), digital broadcasting standards (DAB-T, DVB-T, DVB-C, etc.) And / or digital data transfer services (WLAN, Wi-Fi etc.). Due to the limitation or lack of flexibility in the analog technology counterpart this current wireless communication systems are manufactured to support single standard. This repels the wireless communication field to provide a flexible single terminal solution where various existing standards along with the future standards will also be accommodated very easily. In this context the concept of software defined radio evolves to design a flexible single terminal device which can support multi-standard and multi-carrier protocols. Flexibility is defined by dynamic reconfiguration which results in a very short time to market and reduced development cost.

This emerging technology has evolved towards the concept of SDR. The SDR concept first appeared in the military area , and was later implemented in the civil communication area . Several concepts have been applied to make an ideal SDR solution according to the need. The ASIC implementation or multi-chip solution of the SDR system gives a good performance by higher expenses. Higher integration overhead requirements in the IF processing part of the digital front end, like multi-channel digital up converter (DUC) (Analog Devices AD 6623 or Texas Instruments GC5316) and crest factor reduction (CFR) (PMC-Sierra PM 7819 or Texas Instrument GCl115) increases the carrier per cost. Due to this limitation pure software based (GPP based solution- Vanu's Radio)

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implementation of SDR system has been developed. But this technique has been limited by the poor performance when compared with hardware implementations.

There are two different approaches in the programmable flexible hardware solution (1) DSP based (2) FPGA based. DSP based solution (by Texas Instrument, Sanbridges, etc.) to implement the SDR facilitate the flexibility with the low-power consumption, low-cost and reprogrammable feature. The next generation wireless communication standards which requires very high data rate limits the performance of the DSP based solution. FPGA solution provides a flexible, highly integrated and low-cost feature. In FPGA, dynamic reconfiguration of the hardware to generate multiple standards at different times can be easily done by modifying the algorithm to architecture mapping. Along with this low-power consumption, high data rate support (require for 3G and 4G) and reduced cost per carrier metric feature make the FPGA an ideal platform to develop an SDR system.

VII CONCLUSIONS

In this paper the design is proposed on XILINX Spartan-3E having device as XC3S500E-4FG320 FPGA Hardware kit and observed that with change in no. of blocks and logical coding, actual size i.e. number of logic elements of the circuit changes. In this paper, we get the smaller size Gaussian pulse shaped QPSK modulator which gives same output as the conventional modulator by making some changes in number of blocks and logical coding.

The new design is developed by replacing some blocks by only one ROM block containing different ROM values for a wave, the phase shifting is achieved by taking Q and I as input and starting the wave from particular value for particular symbol. We implemented a new simple direct QPSK digital modulator.

It has been successfully designed with VHDL programming code by XILINX development kit. The modulator generate pulse shaped QPSK modulator signal directly from binary digital data. For test purpose it was generated with VHDL code inside the CPLD/FPGA, mapped For I / Q to control the carrier signal using VHDL multiplexer Code. The output producing modulated digital signal, filtered to transmit through designed filters (LPF/BPF). Experimentally measurements were presented at carrier. The comparison of performance between conventional and proposed design can be done on FPGA kit i.e. speed, device utilization, power consumption etc.

REFERENCES

[1] S.O. Popescu, A.S.Gontean and D.Ianchis, "QPSK Modulator on FPGA," IEEIntelligent Systems and Informatics, September 8-10, 2011, Subotica, Serbia
[2] F.Xiong, "Digital Modulation Techniques", Artech House, UK, 2000.
[3] Wenmiao Song, Qiongqiong Yao, "Design and Implement of QPSK Modem Based on FPGA" North China Electric Power University, Baoding, China.
[4] Douglas.L.Perry"VHDL Programming byExample"Mc.Grawh. USA:Academic 2002, pp. 842- 868
[5] Spartan 3E FPGA Starter Kit board. User guide. Xilinx. 2011.
[6] ISE 9.1 Quick Start Tutorial, Xilinx, 2008.
[7] Roger.Lipsett,Carl.Schaefer, Cary.Ussery "VHDL Hardware Description and design" pp842-868
[8]M.Kovac,J.kolouch "BPSK,QPSK MODULATOR SIMULATION MODUEL"2004

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