

# Low Power High Speed Hybrid CMOS Full Adder Design Using 130 nm Technology

R. Shara, T. K. Kalaiarasan

**Abstract**—One of the most required feature for the electronic system is energy. Adders are the frequently used devices for the portable electronic systems such as for the DSP operations and processor based applications.

In this paper we are implementing the full Adder design using hybrid-CMOS logic style by dividing it in modules so that it can be optimized at various levels.

The adder circuit which we are implementing is hybrid CMOS logic based 16T full adder. Proposed full adder will be designed by combining three modules. Here we will not represent those three modules as a schematic. Module1 will be for xor and xnor operations and module2 and module 3 for the sum and carry operations. By combining these three modules will have the 16T proposed full adder. The proposed full adder area wise reduced and with reduced power consumption. We compared with conventional full adder of 28 transistor technology and 16T full adder of proposed design of 180 nm technology.

This paper presents the proposed circuit as 1-bit 16T CMOS full-adder and the application as 4-bit carry select adder with 130 nm technology of both schematics and layouts.

The proposed design and the application will be implemented by using Electric for the both schematic and layout level diagrams of our project. The LT-SPICE Tool will be used for simulation of the Spice code which tests the functionality of our generated layout and schematic blocks with application.

**Index Terms**—Hybrid CMOS, Full adder, Electric, LT-SPICE, Simulation.

## I. INTRODUCTION

As we know the major concern in vlsi is about area, speed and power. But actually there is no much importance given to the power when compared to the the speed and area in vlsi circuits. But as per the current growing technology, power has become placing a major role to reduce the power consumption of the electronic circuits.

In these applications, average power consumption is a critical design concern. In the absence of low-power design techniques then, current and future portable devices will suffer from either very short battery life or very heavy battery

pack. To reduces this power consumption and for good battery life we are proposing a Hybrid-CMOS<sup>[1]</sup> logic design of the Full adder.

Full adder is a basic block for various arithmetic circuits such as multipliers, compressors, comparators etc. The power consumption, requirement and output delay of arithmetic circuits is surely depending upon the power requirement and delay of the full adder circuits. So for designing the high performance arithmetic circuits, minimization of the delay and power of the full adder circuit is required.

Several logic styles for designing the Full adder have been proposed. In conventional design of full adder normally single CMOS structure is used for the complete design, Such as the standard static CMOS full adder is based on regular CMOS structure with conventional pull -up and pull-down transistors providing full swing output and good driving capabilities but the main drawback of this circuit is less speed due to more number of PMOS and large capacitance. Now here we are proposing a One bit Full Adder (FA) cell with Hybrid-CMOS logic, and it is the building block for most implementations of addition operations with less area and less power consumption. Full adder circuit which is functional building block and most critical component of complex arithmetic circuits like microprocessors, digital signal processors or any ALU's.

## II. CONVENTIONAL FULL ADDER

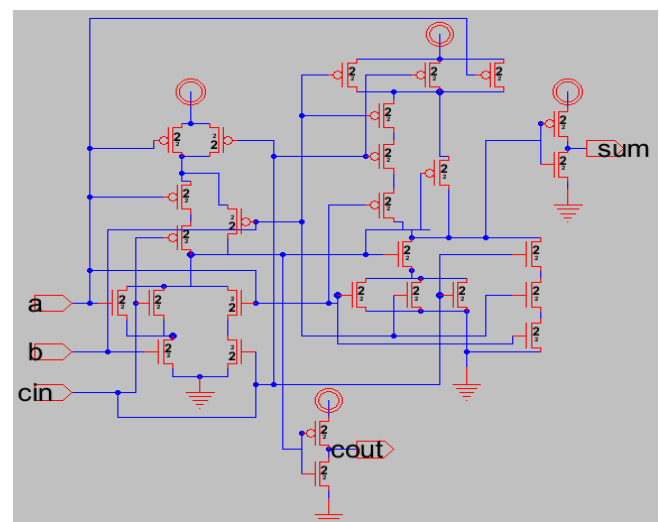


Fig.1 Schematic of Conventional 28T Full adder.

The conventional CMOS 28 transistor Full adder, as shown in above Figure 1, is considered as one of the Base case throughout this paper. The circuit is having inputs are a, b, cin and the sum, cout are the outputs of the one bit conventional 28 transistor full adder of 180 nm technology.

### III. PROPOSED FULL ADDER

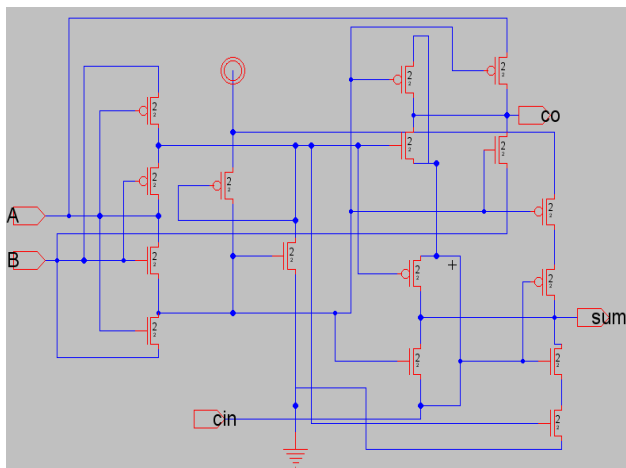


Fig. 2 Schematic of Proposed Full Adder.

The above figure 2 represents the proposed one bit full adder with 130 nm technology. In hybrid-CMOS<sup>[2]</sup> architecture, we get XOR and XNOR operations as module I. Module I circuit is an XOR -XNOR circuit. Many XOR-XNOR circuits are proposed by many authors. Circuit uses only 6 transistors and provides full output swing. This circuit is widely used in hybrid CMOS logic style. Module II and Module III are for the both sum and carry generation as individually. Here we have combined the three modules and designed the one bit full adder of 16 transistors for the 130 nm technology.

The below figure 3 shows the proposed 1-bit full adder layout.

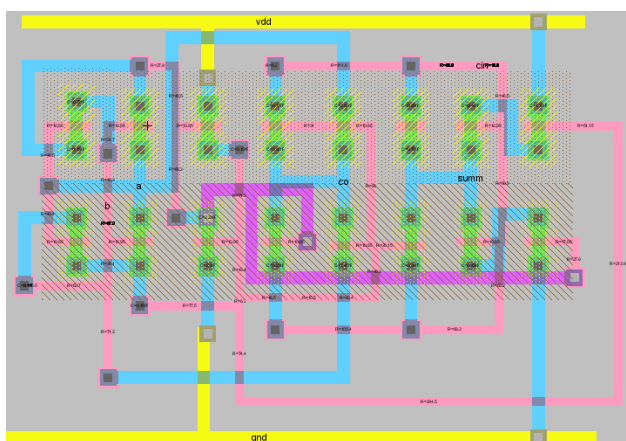


Fig. 3 Layout of the proposed 1-bit full adder.

### IV. CARRY SELECT ADDER APPLICATION

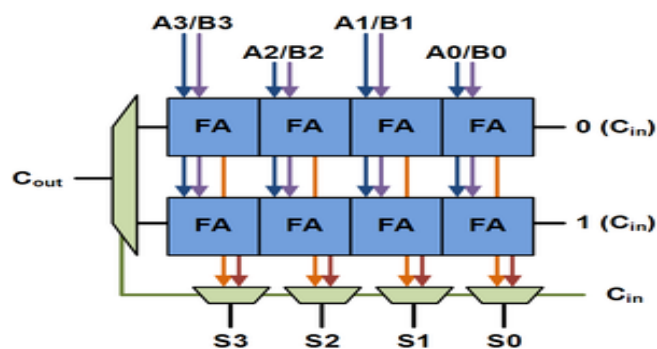


Fig. 4 Block diagram of 4-bit carry select adder.

The carry-select adder generally consists of two ripple carry adders and a multiplexer. In order to perform the calculation twice, one time with the assumption of the carry being logic zero and the other assuming logic one.

The above carry-select adder block size is 4. Two 4-bit ripple carry adders are multiplexed together, where the resulting carry and sum bits are selected by the carry-in. Since one ripple carry adder assumes a carry-in of 0, and the other assumes a carry-in of 1, selecting which adder had the correct assumption via the actual carry-in yields the desired result.

The above application can be used anywhere at communication systems and portable electronic devices.

The below figure 5 shows the 4-bit carry select adder layout for 130 nm technology.

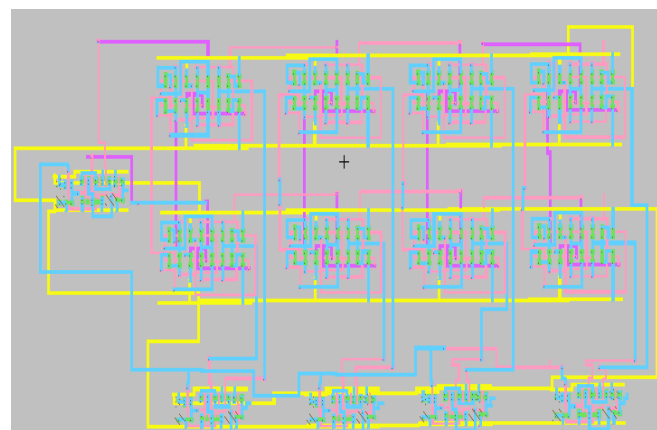


Fig. 5 Layout of 4-bit carry select adder for 130nm.

#### A. Operation of the circuit

From the above block diagram and the layout of the 4-bit carry select adder circuits, the operation of the 4 bit carry select adder will be as follows. The 4-bit carry select adder is having the inputs are a0, a1, a2, a3, b0, b1, b2, b3, cin, c0, c1. And the outputs are s0, s1, s2, s3, and cout.

Those outputs will be coming from the two ripple carry

adders depends on the selection lines of the mux's which are [presented at our block diagram. Here c0, c1 are the two inputs for carry as logic '0' and carry as logic '1'. So for carry as logic '0' the outputs of the 4-bit carry select adder will be coming from the first ripple carry adder for sum's of s0, s1, s2, s3. For carry as logic '1' the outputs of the 4-bit carry select adder will be coming from the second ripple carry adder for sum's of s0, s1, s2, s3.

### V. SIMULATION RESULTS

The below simulation results are showed for the conventional one bit full adder layout of 180 nm technology, proposed full adder<sup>[3]</sup> of both schematic and layouts, 4-bit carry select adder of both schematic and layouts of 130 nm technology.

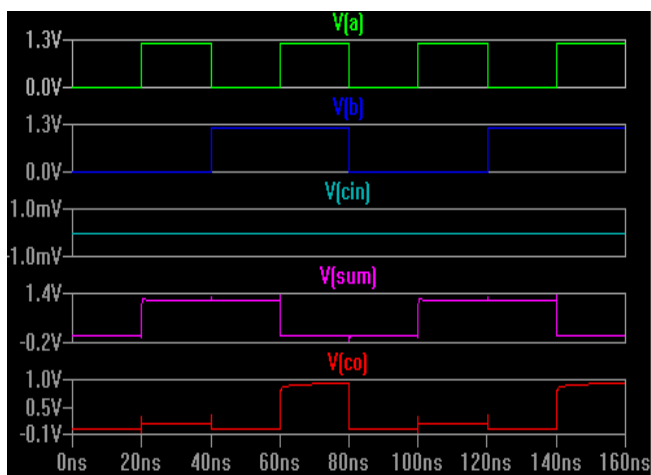


Fig. 6 Simulation Results for schematic of Conventional Full Adder.

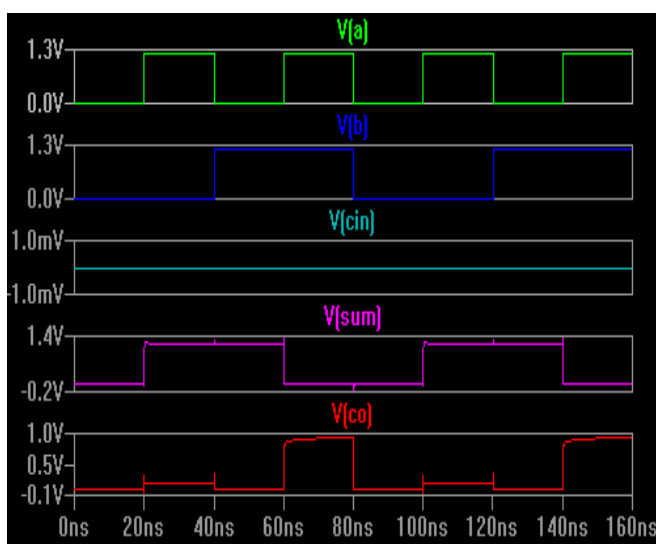


Fig. 7 Simulation Results for schematic of Proposed Full Adder.

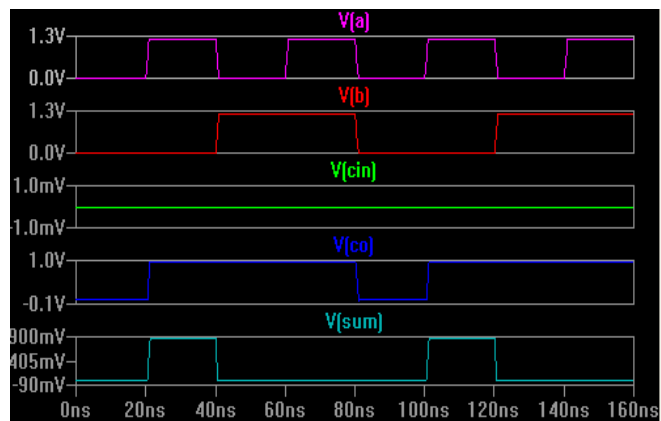


Fig. 8 Simulation Results for Layout of Proposed Full Adder.

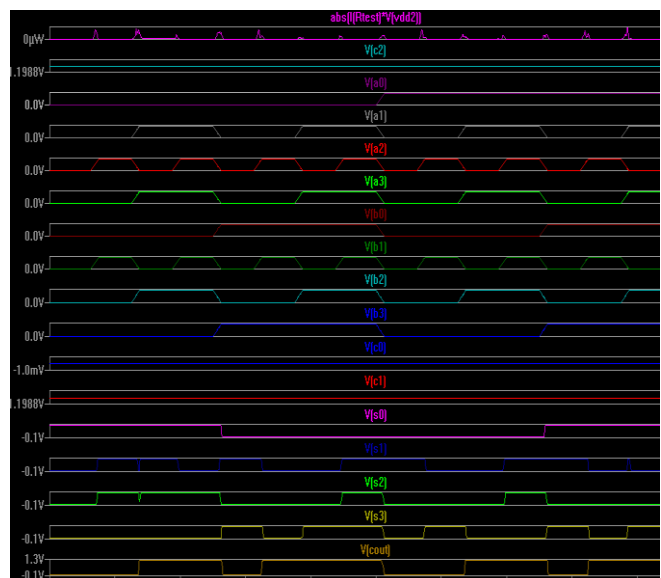


Fig. 9 Simulation Results of 4-bit carry select adder schematic for 130nm.

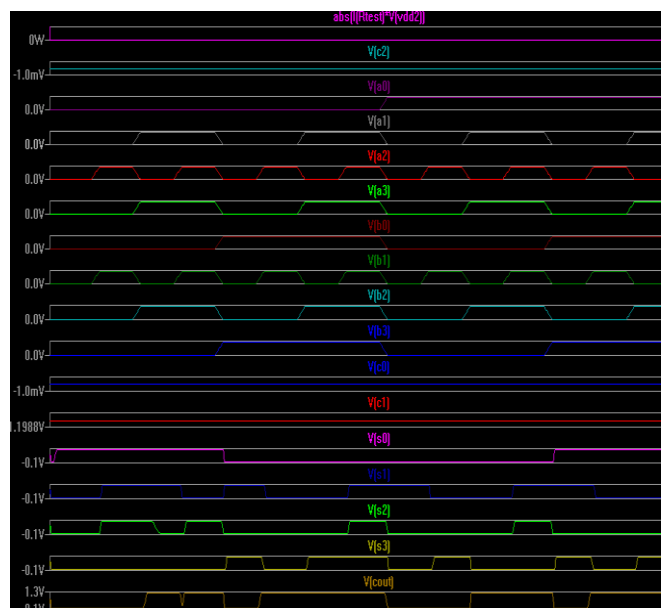


Fig. 10 Simulation Results of 4-bit carry select adder layout for 130nm.

## VI. TABLE

The below table shows the technology difference and power consumption of the each circuit which we have designed.

layouts	technology	Number of transistors	Average power
Conventional full adder	180nm	28	12.974uw
Proposed full adder	130nm	16	685.57nw
Carry select adder	130nm	188	522.19 $\mu$ w
Mux	180nm	12	7.8035uw
Mux	130nm	12	5.9475uw
Proposed full adder	180nm	16	5.530uw
Carry select adder	180nm	188	1.037mw



R. Shara is presently pursuing final semester M. Tech in VLSI at Swetha Institute of technology and science, C. Ramapuram, Tirupati, Andhra Pradesh, India.



T. K. Kalaiarasan, M.tech, working as Head of Department & Associate Professor in the department of Electronics and Communication Engineering in Swetha Institute of technology and science, C. Ramapuram, Tirupati, Andhra Pradesh, India.

## VII. CONCLUSION

The proposed Hybrid-CMOS design style is implemented in module wise, so for any particular application the each module can be used separately for logic dependency. In this paper we have designed the conventional one bit full adder as well as the proposed one bit full adder and compared the results in terms of the power and area.

The application presented in this paper is 4-bit carry select adder with two 4-bit ripple carry implementations. The comparison has been showed in the above table of both for 130nm and 180nm technology and simulation results are also verified.

## REFERENCES

- [1] N. Weste, and K. Eshraghian, "Principles of CMOS VLSI Design: A System Perspective," Reading MA: Wesley, 1993.
- [2] Sung-Mo Kang, and Y. Leblebici, "CMOS Digital Integrated Circuits: Analysis and Design," Tata McGraw Hill, 2003.
- [3] S. Goel, Ashok Kumar and M. A. Bayoumi, "Design of robust, energy-Efficient full adders for deep-submicrometer design using Hybrid-CMOS logic style", IEEE Trans. Very Large Scale Intsgr. (VLSI) Syst., vol. 14, no. 12, Dec. 2006.