Design, Simulation and Parameter extraction of a TG-FinFET Device

Sachin kumar*, Shilpa goyal*

***Abstract*— Planer MOSFET is reaching to its physical limit with the advancement of technology. The factors, which affects the performance of planer MOSFET in sub-half micron regime are drain induced barrier lowering (DIBL), poor subthreshold swing, gate leakage current, band-to-band tunneling across the junction, gate-induced drain leakage (GIDL) and random doping variations. All these constraints is also known as short channel effects (SCE). hence to overcome the difficulties of the planar MOSFET technology or to get better gate control over the channel. FinFET technology based on multiple gate devices is better technology option for further shrinking the size of the planar MOSFET. In this paper work we have designed and simulated a TG-FinFET device using ATLAS command language and 3D device simulators of SILVACO TCAD tool. And then extracted some important parameters related to the process and device simulation like Vth, gate leakage, subthreshold voltage.**

***Index Terms*— Design, Parameter Extraction, Planer MOSFET, Simulation, SCEs, SILVACO, TG-FinFET.**

I. INTRODUCTION

When we shrink further the size of the planar MOSFET technology several short channel effects are produced. So instead of planar MOSFET technology DG-MOSFET/TG-MOSFET technology based on multiple gate devices have better control over the SCEs[4]. Particularly the FinFET technology provides superior scalability of the TG-MOSFETs compare to the planar MOSFET. It provides better performance compare to the bulk Si-CMOS technology. Because of its compatibility with the recent CMOS technology, FinFETs are seen to be strong candidate for replacing the bulk or planar Si-CMOS technology from 22nm node onwards[3].

With scaling of planar bulk MOSFETs, the channel doping will need to be increased to undesirably high levels in order to reduce short-channel effects and to set the threshold voltage according to requirement. As a result of the high channel doping, the mobility of electrons and holes will be reduced and the junction leakage due to band-to-band tunneling and gate-induced drain leakage will increase[8]. Furthermore, due to the small total number of dopants in the channel of extremely small MOSFETs, the percentage of stochastic variation in the number and location of the dopants will increase sharply, and this will sharply increase the statistical variability of the threshold voltage[10].

Another challenge for highly scaled MOSFETs is to reduce the parasitic series source/drain resistance (Rsd) to tolerable values with very shallow source and drain junction depth. Due to the challenges with the scaling of planar bulk MOSFETs, advanced devices such as ultra-thin body fully depleted SOI MOSFETs and multiple-gate, particularly double-gate (DG), Triple-gate (TG) MOSFETs (e.g., FinFETs) are under investigation[8]. Since such devices will typically have lightly doped channels and the threshold voltage will be controlled by the metal gate electrode work function, the challenges associated with high channel doping and stochastic dopants variation in planar bulk MOSFETs can be avoided by using multigate architecture.

This paper work investigates the effects of geometrical parameters variation on the performance of Triple Gate (TG) FinFET structures designed by ATLAS 3D simulator. After designing the device successfully their V-I characteristics has been drawn. It has been found that controlling of threshold voltage by metal gate with proper work function could be more effective approach for ultra large scaled devices. In this work, various parameters related to FinFET devices have been extracted to investigate or analyse the Short Channel Effects (SCEs) on FinFET devices.

II. DESIGN OF FINFET

There are two methods to design a 3-D device by using SILVACO TCAD Tool 1) Atlas command language 2) DevEDIT3D, So here we have used first one i.e. Atlas command language.

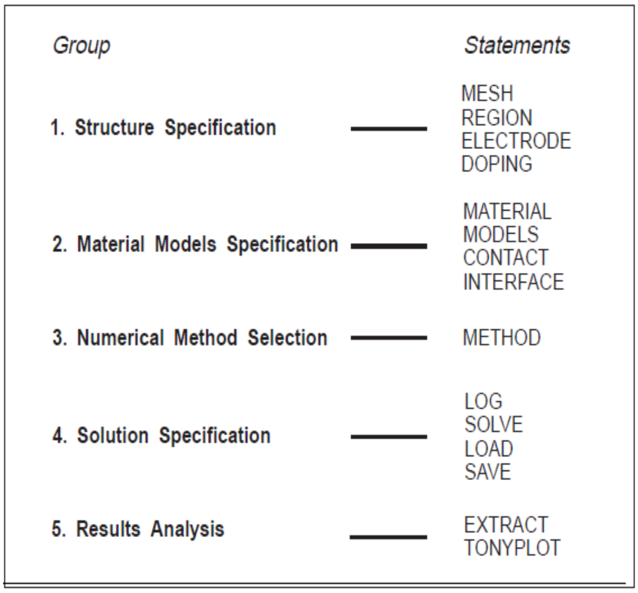

Fig.1- Atlas Command Groups with the Primary Statements in each Group[16]

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To define a device through the Atlas command language, you must first define a mesh. This mesh or grid covers the physical simulation domain. The mesh is defined by a series of horizontal and vertical lines and the spacing between them. Then, regions within this mesh are allocated to different materials as required to construct the device. For example, the specification of a MOS device requires the specification of silicon and silicon dioxide regions. After the regions are defined, the location of electrodes is specified. The final step is to specify the doping in each region.

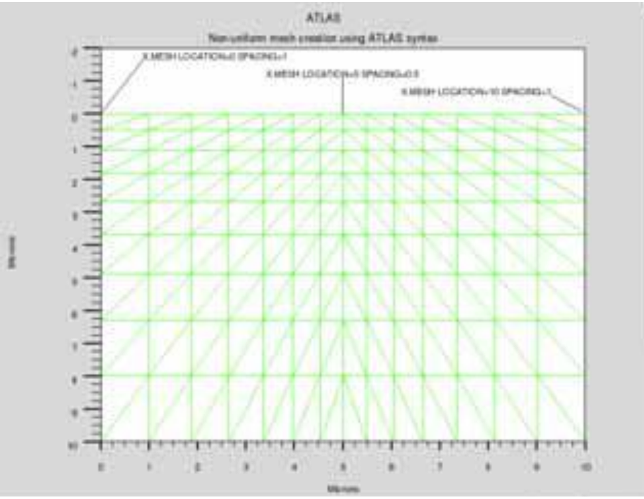

Fig.2- Non-uniform Mesh Creation using Atlas Syntax

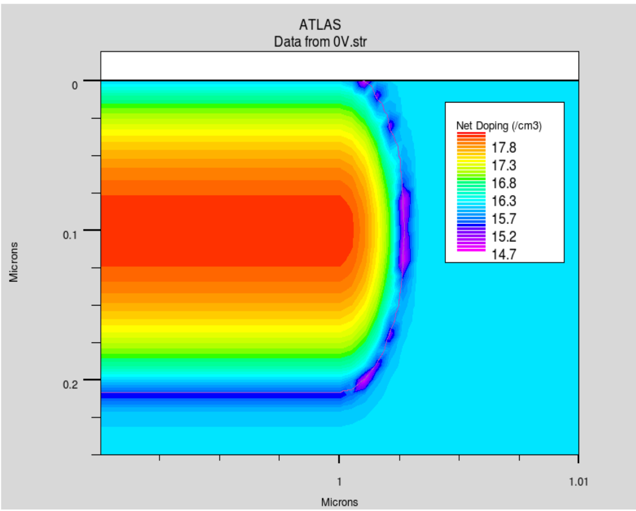

Fig.3- Analytical specification of a 2D Profile[16]

Automatic meshing provides a simpler method for defining device structures and meshes than the standard method described in this Section "Using The Command Language To Define A Structure". Auto-meshing is particularly suited for epitaxial structures, especially device structures with many layers (for example, a VCSEL device)[16]. Auto-meshing unburdens you from the delicate bookkeeping involved in ensuring that the locations of mesh lines in the Y direction are consistently aligned with the edges of regions. This is done by specifying the locations of Y mesh lines in the REGION statements. This concept of automatic-meshing has been implemented here while designing the proposed TG-FinFET device structure.

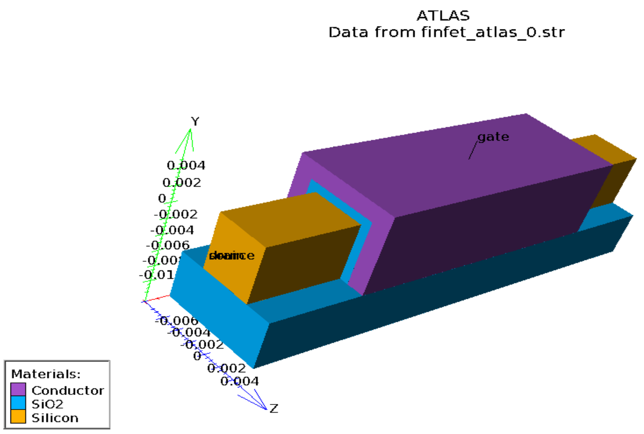

Fig.4- A 30-nm TG-FinFET 3-D structure designed by ATLAS

The basic characteristics of the designed TG-FinFET is Tox=1nm length=30nm width=6nm and Fin height=7nm, gate workfunction=4.16. Note that we have defined a parametrized structure for subsequent use in our automation tool which make much more easier any kind of variation (length, width..) to perform large scale simulation. The main physical effects (mobility, carrier statistics, recombination) were expressed by a set of models universally used for simulating the MOS technology: mobility dependence of the electric field and doping level, Boltzmann statistics and Schokley-Read-Hall generation recombination mechanisms.

III. FINFET SIMULATION

The 3-D SILVACO simulation suite including Device3D, Atlas3D, DevEDIT3D and TonyPlot3D, allows device engineers to study deep sub-micron devices which are 3-D by nature like the FinFET presented above. Furthermore, 3-D simulations give access to data impossible to measure like charge distribution, potential, electric field and current lines. After designing the FinFET now start the ATLAS device simulator by the following command:

go atlas in the **DeckBUILD** command window.

Then the Atlas will be the current simulator in DeckBUILD. And we can use the different numerical solution techniques, physical models, and save the structure and Log files. After that plot the results in the form of V-I characteristics.

A. Choosing Numerical Methods

Numerical Solution Techniques- Several different numerical methods can be used for calculating the solutions to semiconductor device problems. Numerical methods are given in the METHOD statements of the input file. Some guidelines for these methods will be given here. Different combinations of models will require Atlas to solve up to six equations. For each of the model types, there are basically three types of solution techniques: (a) decoupled (GUMMEL), (b) fully coupled (NEWTON) and (c) BLOCK. The GUMMEL method will solve for each unknown in turn keeping the other variables constant, repeating the process until a stable solution is achieved. The NEWTON method solve the total system of unknowns together[16]. The BLOCK methods will solve some equations fully coupled while others are de-coupled. Generally, the GUMMEL method is useful where the system of equations is weakly coupled but has only

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linear convergence[11]. The NEWTON method is useful when the system of equations is strongly coupled and has quadratic convergence. The NEWTON method may, however, spend extra time solving for quantities, which are essentially constant or weakly coupled. NEWTON also requires a more accurate initial guess to the problem to obtain convergence. Thus, a BLOCK method can provide for faster simulations times in these cases over NEWTON. GUMMEL can often provide better initial guesses to problems[9]. It can be useful to start a solution with a few GUMMEL iterations to generate a better guess. Then, switch to NEWTON to complete the solution. Specification of the solution method is carried out as follows:

B. Method GUMMEL BLOCK NEWTON

The exact meaning of the statement depends on the particular models it applied to. This will be discussed in the following sections.

Basic Drift Diffusion Calculations- The isothermal drift diffusion model requires the solution of three equations for potential, electron concentration, and hole concentration. Specifying GUMMEL or NEWTON alone will produce simple Gummel or Newton solutions as detailed above. For almost all cases, the NEWTON method is preferred and it is the default Specifying:

C. Method GUMMEL NEWTON

It will cause the solver to start with GUMMEL iterations. Then, switch to NEWTON if convergence is not achieved. This is a robust but a more time consuming way of obtaining solutions for any device. This method, however, is highly recommended for all simulations with floating regions such as SOI transistors[1]. A floating region is defined as an area of doping, which is separated from all electrodes by a pn junction. BLOCK is equivalent to NEWTON for all isothermal drift-diffusion simulations.

D. Obtaining Solutions

Atlas can calculate DC, AC small signal, and transient solutions. Obtaining solutions is similar to setting up parametric test equipment for device tests. You usually define the voltages on each of the electrodes in the device. Atlas then calculates the current through each electrode. Atlas also calculates internal quantities, such as carrier concentrations and electric fields throughout the device. This is information that is difficult or impossible to measure.

In all simulations, the device starts with zero bias on all electrodes. Solutions are obtained by stepping the biases on electrodes from this initial equilibrium condition. As will be discussed, due to the initial guess strategy, voltage step sizes are limited. This section concentrates on defining solution procedures. To save results, use the LOG or SAVE statements.

E. DC Solutions

In DC solutions, the voltage on each electrode is specified using the SOLVE statement. For example, the statements:

SOLVE VGATE=1.0
SOLVE VGATE=2.0

solves a single bias point with 1.0V and then 2.0V on the gate electrode. One important rule in Atlas is that when the voltage on any electrode is not specified in a given SOLVE statement, the value from the last SOLVE statement is assumed. In the following case, the second solution is for a drain voltage of 1.0V and a gate voltage of 2.0V.

SOLVE VGATE=2.0
SOLVE VDRAIN=1.0

When the voltage on a particular electrode is never defined on any SOLVE statement and voltage is zero, you don't need to explicitly state the voltage on all electrodes on all SOLVE statements. For example, in a MOSFET, if Vsub is not specified, then Vbs defaults to zero.

F. Sweeping The Bias

For most applications, a sweep of one or more electrodes is usually required. The basic DC stepping is inconvenient and a ramped bias should be used. To ramp the base voltage from 0.0V to 1.0V with 0.05V steps with a fixed collector voltage of 2.0V, use the following syntax:

SOLVE VDRAIN=2.0
SOLVE VBASE=0.0 VSTEP=0.05 VFINAL=1.0 NAME=base

The NAME parameter is required and the electrode name is case-sensitive. Make sure the initial voltage, VSTEP and VFINAL, are consistent. A badly specified ramp from zero to 1.5V in 0.2V steps will finish at 1.4V or 1.6V.

G. Generating Families of Curves-

Many applications such as MOSFET Id/Vds and bipolar Ic/Vce simulations require that a family of curves is produced. This is done by obtaining solutions at each of the stepped bias points first, and then solving over the swept bias variable at each stepped point. For example in MOSFET Id/Vds curves, solutions for each Vgs value are obtained with Vds=0.0V. The output from these solutions are saved in Atlas solution files. For each gate bias, the solution file is loaded and the ramp of drain voltage performed.

The family of curves for three 1V gate steps and a 3.3V drain sweep would be implemented in Atlas as follows:

SOLVE VGATE=1.0 OUTF=solve_vgate1
SOLVE VGATE=2.0 OUTF=solve_vgate2
SOLVE VGATE=3.0 OUTF=solve_vgate3
LOAD INFILE=solve_vgate1
LOG OUTFILE=mos_drain_sweep1
SOLVE NAME=drain VDRAIN=0 VFINAL=3.3 VSTEP=0.3
LOAD INFILE=solve_vgate2
LOG OUTFILE=mos_drain_sweep2
SOLVE NAME=drain VDRAIN=0 VFINAL=3.3 VSTEP=0.3
LOAD INFILE=solve_vgate3
LOG OUTFILE=mos_drain_sweep3
SOLVE NAME=drain VDRAIN=0 VFINAL=3.3 VSTEP=0.3

The LOG statements are used to save the Id/Vds curve from each gate voltage to separate files.

We recommend that you save the data in this manner rather than to a single LOG file.

H. Interpreting the Results

Atlas produces three different types of output files. These files are also described in the following sections.

a) Run-Time Output- Run-time output is provided at the bottom of the DeckBuild Window. If it's run as a batch job, the run-time output can be stored to a file. Errors occurring in the run-time output will be displayed in this window. Note

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that not all errors will be fatal (as DeckBuild tries to interpret the file and continue). This may cause a statement to be ignored, leading to unexpected results. We recommend that you check the run-time output of any newly created input file the first time it runs to intercept any errors. If you specify the PRINT option within the MODELS statement, the details of material parameters and constants and mobility models will be specified at the start of the run-time output. This is a useful way of checking what parameters values and models are being applied in the simulation. We recommend that you always specify MODELS PRINT in input files. During SOLVE statements.

b) Log Files- Log files store the terminal characteristics calculated by Atlas. These are current and voltages for each electrode in DC simulations. In transient simulations, the time is stored. In AC simulations, the small signal frequency and the conductances and capacitances are saved. For example, the statement: LOG OUTF=<FILENAME>

is used to open a log file. Terminal characteristics from all SOLVE statements after the LOG statement are then saved to this file along with any results from the PROBE statement. To not save the terminal characteristics to this file, use another LOG statement with either a different log filename or the OFF parameter. Typically, a separate log file should be used for each bias sweep. For example, separate log files are used for each gate bias in a MOS Id/Vds simulation or each base current in a bipolar Ic/Vce simulation. These files are then overlaid in TonyPlot. Log files contain only the terminal characteristics. They are typically viewed in TonyPlot. Parameter extraction of data in log files can be done in DeckBuild. Log files cannot be loaded into Atlas to re-initialize the simulation.

IV. PARAMETER EXTRACTION

The EXTRACT command is provided within the DeckBuild environment. It allows you to extract device parameters. The command has a flexible syntax that allows you to construct specific EXTRACT routines. EXTRACT operates on the previous solved curve or structure file. By default, EXTRACT uses the currently open log file. To override this default, supply the name of a file to be used by EXTRACT before the extraction routine[16]. For example:

EXTRACT INIT INF="<filename>"

A typical example of using EXTRACT is the extraction of the threshold voltage of an MOS transistor. In the following example, the threshold voltage is extracted by calculating the maximum slope of the Id / Vg curve, finding the intercept with the X axis and then subtracting half of the applied drain bias.

EXTRACT NAME="nvt"
XINTERCEPT(MAXSLOPE(CURVE(V."GATE",(I."DRAIN"))) \-(AVE(V."DRAIN"))/2.0)

The results of the extraction will be displayed in the run-time output and will be by default stored in the file results.final. To store the results in a different file at the end of EXTRACT command, use the following option:

EXTRACT....DATAFILE="<filename>"

V. DEVICE SIMULATION RESULTS

We have drawn two V-I characteristics in the form of Id/Ig Vs Vgs. And Id Vs Vds for different gate voltages as shown in Fig.6, and we have extracted some important parameters related to the device simulation of designed TG-FinFET device.

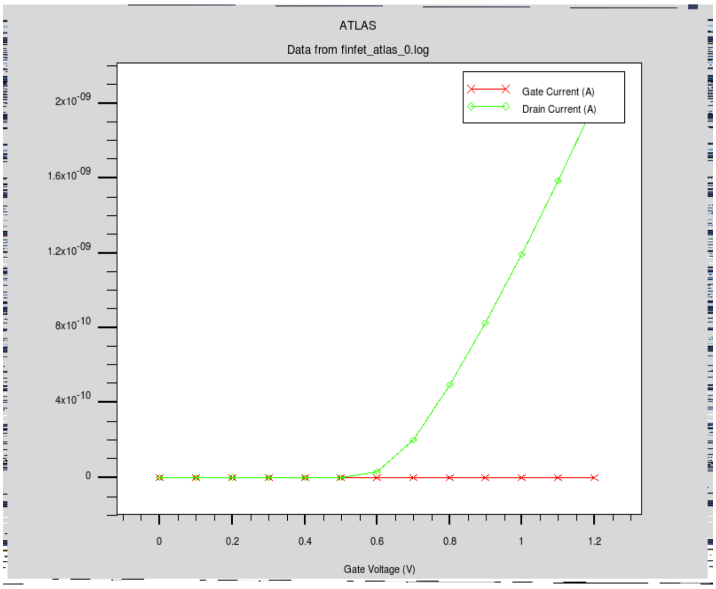

Fig.5- Ids/Ig Vs Vgs characteristics of FinFET designed by ATLAS Command Syntax

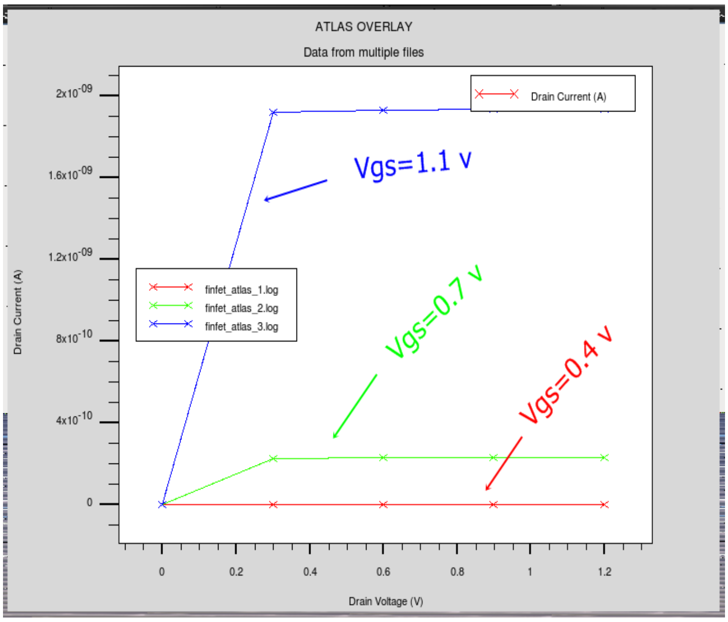

Fig.6- Ids Vs Vds characteristics of FinFET designed by ATLAS Command Syntax

As one can see easily in the V-I characterstics of Fig.5 the threshold voltage of this device is around 0.62V. and the V-I characteristics for varying Vgs is shown in Fig.6. So the effect of varying the Vgs is easily seen in Fig.6. hence greater the value of Vgs will lead to the greater value of Id i.e. drain current that is the result of large no of charge carriers present in the channel due to higher electric field present there by the higher Vgs voltages.

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Extracted Parameter stored in file results.final

Vth=0.623031
subVth=0.0603581
gate_leakage=0 A
BETA=3.6392e-08
THETA=0.212372
Ion= 1.1899e-09 A
Ioff=1.5e-15 A
DIBL= 70 mv/V
drain_leakage=4.32061e-09 A/um

VI. CONCLUSION AND FUTURE SCOPE

We have studied the Silvaco Tcad tool's working, functioning and its various capabilities. Silvaco is a complete TCAD tool suite including various process, stress simulator, optical simulator and device simulator, by using that we can design a semiconductor device and we can choose any material type as there are many available options to select in from them. Moreover of this you can define custom material type by using silvaco's process simulator and DeckBUILD tool, as this option is also available here.

Silvaco TCAD can model and process FinFET, SOI, TFT, Solar cell, SONOS non-volatile memory, organic devices like OLED, Optoelectronic devices, effect of noise on structures, MESFET, LED, LASER, EPROM, Diode, CCD, BJT and many other devices. It can also simulate these devices[16].

Using the SILVACO TCAD Tool, we can model and process any semiconductor device. We can also extract the various parameters of the semiconductor device, and we can do circuit analysis of semiconductor devices, and we can analyse the effects of short channel effect, and narrow channel effect of various devices.

The TG-FinFET device is designed and modeled using silvaco's device simulators and V-I characteristics is drown successfully by using the available graphical tool TonyPLOT and TonyPLOT3D successfully and after that various parameter is extracted successfully.

It is very easy to study the impact of the geometry and doping of this 3-D device using Device3D, ATLAS and other related device simulators. Indeed more and more people take a look at this novel structure since it is an attractive successor to the single-gate MOSFET. Here we modeled a 3-D FinFET device. FinFET is a basic digital device which can be used as an inverter, Flip-flop, Switch, and it can be a part of any combinational and sequential circuit.

p-type device can be modeled as scaling rules may differ for that. And other analysis can be performed on FinFET devices. And we can analyse the device by varying all the possible process parameters. And after making a optimal device one can use that device to make a circuit. And after that one can perform circuit level simulations to find out the circuit level important parameters.

For silicon technology, as scaling of semiconductor device, process variations inevitably become a critical issue for ultra-small volume transistors. Besides the structure problem, the random dopant fluctuation (RDF) effect also can lead to a dramatic increase in threshold voltage variation even for FinFET with a lightly doped body. The decreased impurity atoms in a tiny fin result in a random placement, contributing to the threshold voltage variation.

For III-V technology, although nitride electronics development has been booming recently, the progress of III-V devices, including both wide bandgap materials (GaN, AlN and AlGaN) and narrow bandgap materials (InAs, InGaAs), has been hampered by electrically active defects that manifest as traps affecting device performance and reliability. To minimize those negative impacts and continue the advancement of III-V semiconductors, a fundamental understanding of the defects is indispensable and the correlations of defects to the performance and reliability degradation is required.

To speed up the exploration of various effects, TCAD, the powerful gear, can be applied for a comprehensive understanding of III-V device electrical behaviors. It is recommended that the surface defects model should be developed based on the enhanced characterization and convincing physics support. TCAD will also play an important role in the model development and validation. Although the ideal physics prediction and the TCAD modeling imply InGaAs can conduct high current under low bias, the high density interface states within the III-V transistor greatly reduce the free carrier and restrict the maximum performance.

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***Sachin kumar**, M.Tech in VLSI DESIGN and Technology from YMCA University of Science & Technology Faridabad Haryana, India during 2013-2015. He received his B.Tech degree in Electronics and Communication Engineering from Bharat Institute of Technology Meerut Uttar Pradesh, India in 2012. His major area of research is the Recent developments or advancements in transistors technology to solve the current problems of scaling in semiconductor industry.

***Shilpa goyal**, M.Tech in VLSI Design and Technology from YMCA university of science & Technology, Faridabad, India during 2013-2015. She received her B.Tech degree in Electronics and Communication Engineering from Kaithal, India in 2012.

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