VHDL Implementation of Audio Processing Using Adaptive Filter

G Saipriya, T Thammi Reddy

Abstract*— *In this paper, we display the Implementation of Audio processing utilizing VHDL. The Adaptive channel is connected to the signal with the end goal of noise cancellation. Hence reduces the delay of the signal furthermore enhancing the nature of the signal. The Major application range of this paper will be in the computerized correspondences by interfacing a few different load up utilizing inbuilt I/O's, each with various information channels that will speak with one another progressively over a rapid correspondence join. The fundamental issue of this paper is the execution of the filtered signal using adaptive filter.The process includes the functions of ADC and DAC.

***Index Terms*—ADC, DAC, VHDL Adaptive filter.**

I. INTRODUCTION

In general, the first phase of Digitally processing audio is to change over the analogue audio signal to a digitized representation utilizing an analogue to digital converter (ADC). The digital signal preparing is then completed before being bolstered into a digital to analogue converter (DAC) to make a analogue signal from the digital one. The ADC and DAC are most regularly offered as one IC package.[4] In the most recent couple of decades the interest for compact and embedded digital signal processing (DSP) frameworks has expanded significantly. Applications, for example, phones, amplifiers, and digital audio devices are applications with stringent imperatives, such as, area, speed and power consumption utilization. These applications require an execution that meet these limitations with the briefest time to advertise. The conceivable option usage that can be utilized extent from an ASIC custom chip, general purpose processor (GPP) to DSP processors. While the first decision could give the arrangement that meets all the hard limitations, it does not have the adaptability that exist in the other two, furthermore its configuration cycle is any longer. Reconfigurable figuring is increasing much consideration as a prototyping furthermore, usage innovation of advanced frameworks. Utilizing programmable devices (like FPGAs) for DSP applications could contract the crevice between the adaptability of GPP, and programmable DSP processors, and the elite of devoted equipment utilizing ASIC innovation[1]. The relevance of a FPGA framework as a equipment base for real time audio processing in an earphone based increased reality sound framework. Such frameworks superpose simulated audio signals with the real sound. One of the elements of such a framework is to quench undesirable sound sources of the genuine environment, a task known as adaptive noise cancellation (ANC). ANC systems are recognized by their distinctive objectives that lead to distinctive architectures.[6]

In the Existing Method of this design the signals ,were not filtered so in the presence of noise the delay was more in the signal. In order to overcome that, the signals are filtered to cancel the noise and reduce the time of delay so as to improve the latency.

II. BLOCK DIAGRAM OF PROPOSED DESIGN

The proposed design consists of the ADC, DAC, Filter, Memory. Through which the process can be done. The block diagram is shown below

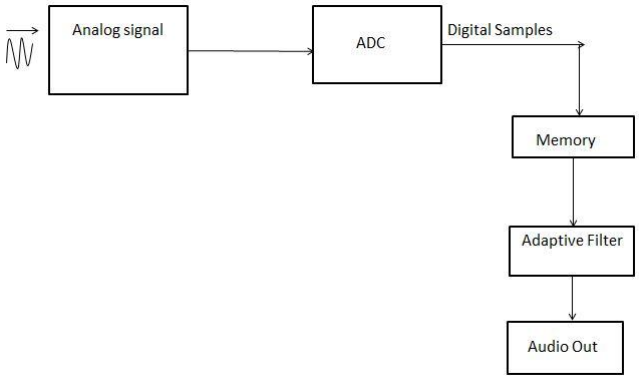

Fig.1.Block Diagram of Proposed Design

The main aim of the proposed design is to take an analog signal covert the signal into digital samples using ADC. These digital samples are stored in a memory i.e.,NAND flash memory for the purpose of Filtering. The stored signals are filtered using adaptive filter. The output is shown in the form of simulation. The tools used for this design are Xilinx ISE design suite13.2 for synthesis in order to check the delay and the simulation tool is Mentor Graphics HDL designer.[10] The delay reduces compared to the existing method which was implemented without filter.

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III. ADAPTIVE FILTERING USING MCM

In the last decades, the field of digital signal processing, and particularly adaptive signal processing, has developed enormously due to the increasingly availability of technology for the implementation of the emerging algorithms. These algorithms have been applied to an extensive number of problems including noise and echo canceling, channel equalization, signal prediction, adaptive arrays as well as many others. [2]-[5]An adaptive filter may be understood as a self-modifying digital filter that adjusts its coefficients in order to minimize an error function. This error function, also referred to as the cost function, is a distance measurement between the reference or desired signal and the output of the adaptive filter. The Basic block Diagram of Adaptive filter is shown below

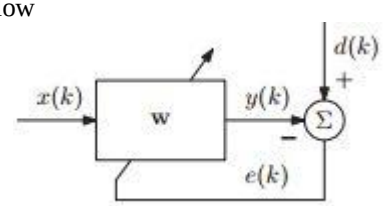

Fig .2. Basic Diagram of Adaptive filter

Due to the desired real-time characteristic, the adaptive filter performance must take into account practical levels of computational complexity and limited-precision representation of associated signals and coeffi- cients. The effort in obtaining fast versions of more complex algorithms results from the desire of reducing the computational requirements to a minimal number of operations, as well as reducing the size of memory necessary to run these algorithms in practical applications. On the other hand, a limited-precision environment generates quantization errors which drive the attention of designers to numerical stability, numerical accuracy, and convergence robustness of the algorithm.

In this Paper the MCM factor is used to apply the adaptive filtering technique. MCM means the Multiple constant Multiplications .Each digital sample gets multiplied by the digital sample in order to filter the signal. This can be shown in below equation

MCM0 := H0*mx……(1)

Where, MCM-Multiple Constant Multiplication
H0- Digital Sample
mx-Filter Coefficient

By using this factor the digital samples are filtered to get noise free output with reduced delay compared to the existing design with out filter.

The Memory used to store the digital samples is NAND flash memory where the data is stored in the form of 1's and 0's.These memory can be checked using the Mode select State diagram for entering the data in order to check whether it is empty or full. The state diagram for this method is shown below

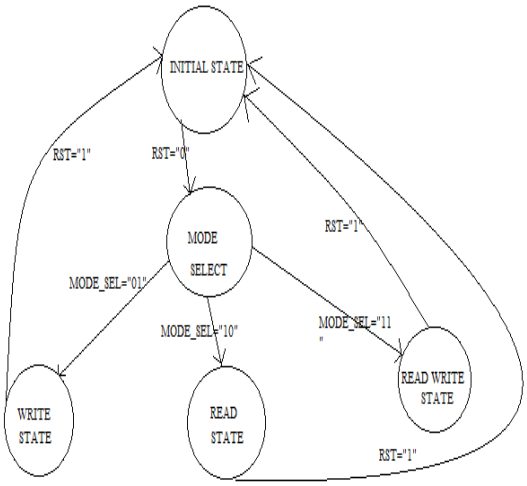

Fig.3. State diagram for Memory mode selection

IV. SIMULATION & SYNTHESIS RESULTS

The simulation result for the proposed design is done using Mentor Graphics HDL designer and it is shown below

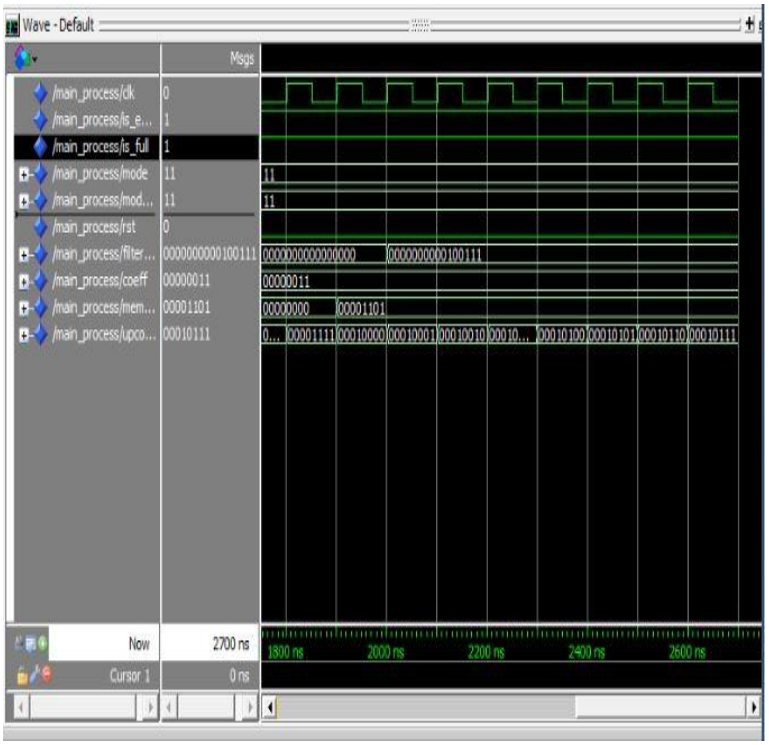

Fig..4. Simulation Result of the Proposed Design

The synthesis report for the Proposed design audio processed with filter

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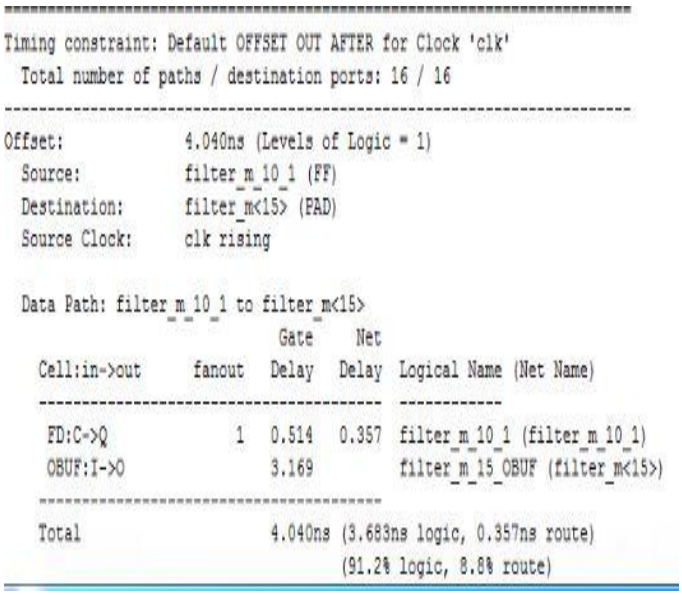
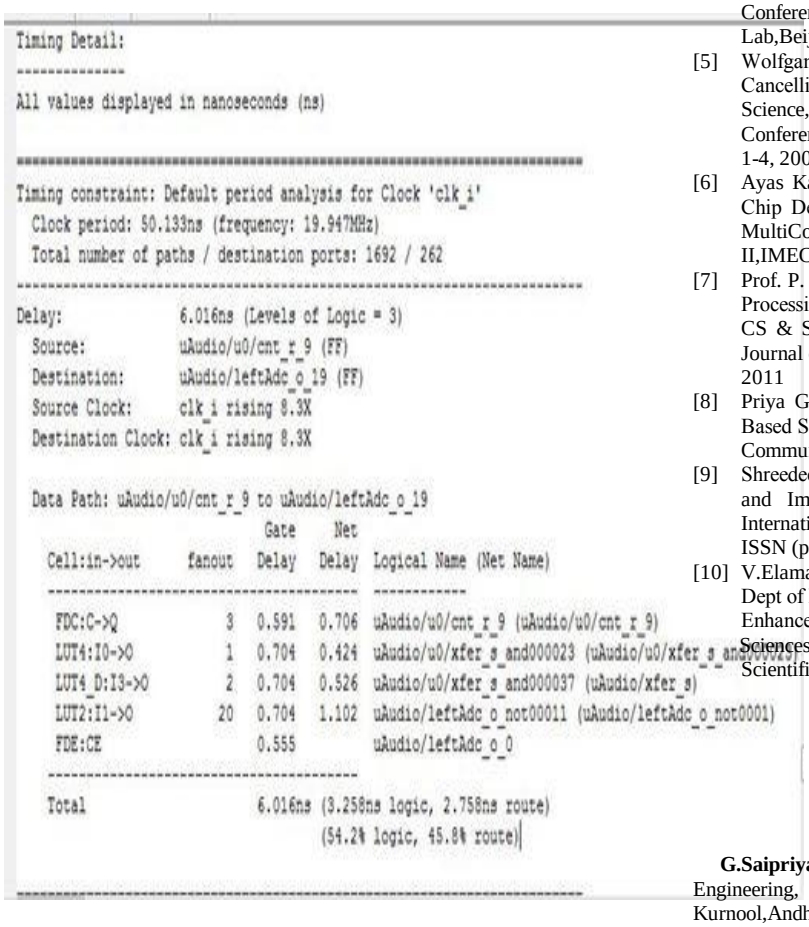


```
Timing constraint: Default OFFSET OUT AFTER for Clock 'clk'
  Total number of paths / destination ports: 16 / 16
--------------------------------------------------------------------------------
Offset:              4.040ns (Levels of Logic = 1)
  Source:            filter_m_10_1 (FF)
  Destination:       filter_m<15> (PAD)
  Source Clock:      clk rising

  Data Path: filter_m_10_1 to filter_m<15>
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     FD:C->Q              1    0.514   0.357  filter_m_10_1 (filter_m_10_1)
     OBUF:I->O                 3.169          filter_m_15_OBUF (filter_m<15>)
    ----------------------------------------
    Total                      4.040ns (3.683ns logic, 0.357ns route)
                                       (91.2% logic, 8.8% route)
```

Fig.5. synthesis report of the proposed design

The synthesis report for Existing design without filter



```
Timing Detail:
--------------
All values displayed in nanoseconds (ns)

================================================================================
Timing constraint: Default period analysis for Clock 'clk_i'
  Clock period: 50.133ns (frequency: 19.947MHz)
  Total number of paths / destination ports: 1692 / 262
--------------------------------------------------------------------------------
Delay:               6.016ns (Levels of Logic = 3)
  Source:            uAudio/u0/cnt_r_9 (FF)
  Destination:       uAudio/leftAdc_o_19 (FF)
  Source Clock:      clk_i rising 8.3X
  Destination Clock: clk_i rising 8.3X

  Data Path: uAudio/u0/cnt_r_9 to uAudio/leftAdc_o_19
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     FDC:C->Q             3    0.591   0.706  uAudio/u0/cnt_r_9 (uAudio/u0/cnt_r_9)
     LUT4:I0->O           1    0.704   0.424  uAudio/u0/xfer_s_and000023 (uAudio/u0/xfer_s_and0000)
     LUT4_D:I3->O         2    0.704   0.526  uAudio/u0/xfer_s_and000037 (uAudio/xfer_s)
     LUT2:I1->O          20    0.704   1.102  uAudio/leftAdc_o_not00011 (uAudio/leftAdc_o_not0001)
     FDE:CE                    0.555          uAudio/leftAdc_o_0
    ----------------------------------------
    Total                      6.016ns (3.258ns logic, 2.758ns route)
                                       (54.2% logic, 45.8% route)

================================================================================
```

Fig.6. synthesis report of the existing design

By comparing results the total delay for existing and the Proposed design it reduced to 1.97 ns.

V. CONCLUSION

This paper presents the implementation of audio processing applying adaptive filtering using VHDL. This process reduces the delay in the signal thus reduces the latency of the signal. If this paper is implemented in hardware using FPGA then the cost also becomes low. The advantage of this process is the quality of the audio signals can be improved

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