LOW POWER SRAM CELL OF LEAKAGE CURRENT AND LEAKAGE POWER REDUCTION

K.VENUGOPAL P.SIREESH BABU

Abstract - A SRAM cell must meet requirements for operation in submicron. As the density of SRAM increases, the leakage power has become a significant component in chip design. The power Consumption is a major issue of today's CMOS Technology. Leakage power is major issue for short channel devices. As the technology is shrinking the leakage current is increasing very fast. so, several methods and techniques have been proposed for leakage reduction in CMOS digital integrated circuits. This paper idea of 6T, 8T and 10T models with sleep transistors. SRAM cell with sleep transistor shows better leakage reduction approach than Conventional approaches. Here in this paper Analog environment virtuoso (cadence) simulator is used for analysis of the power associated with CMOS SRAM cell for 180nm technology.

Index Terms - 6T Conventional SRAM cell, Leakage current and leakage power, 6T, 8T and 10T sleep transistor models, Sub-threshold leakage current reduction.

K.Venugopal is the student of M.Tech VLSI and Embedded Systems,Prakasam Engineering College, kandukur,Prakasam(Dist),AndhraPradesh, INDIA 523105.

P.Sireesh Babu M.Tech(PhD),Asst. Professor in Prakasam Engineering College,kandukur, prakasam(Dist),AndhraPradesh,INDIA 523105.

I. INTRODUCTION

SRAMs have become a critical component of many VLSI chips. In today's world the increase of density of Integrated Circuits can be viewed as result due to exponential increase in fabrication process of VLSI circuits. For the Deep submicron technology circuit, the size of CMOS integrated circuits is shrinking day by day. So, the power dissipation is a major issue for the short channel devices and the performance of digital integrated circuits is challenged by higher power consumption [1]. Scaling also results in higher speed of operation and improves the performance of the device. Decreased threshold voltage and thinner gate oxide also increases the leakage current [2]. 6T SRAM cell basically consists of four cross-coupled transistors. There are two NMOS access and driver transistors. In 8T method there are two extra NMOS transistors connected in series called 'stack' approach[3].

II. RELATED WORK

The low power reduction techniques reduce the leakage based on the dependencies of the tunneling currents on the terminal voltages, the gate oxide thickness, and the type of the transistor. In standby mode of SRAM bit-cell, there are several sources for leakage current, e.g., the sub-threshold current due to low threshold voltage, etc., As process technology is scaled down, threshold voltage and leakage current variations are

ISSN: 2278 – 7798 All Rights Reserved © 2015 IJSETR

increased. Leakage power is a high priority consideration due to feature scaling in high performance processor design. In order to maintain performance, however, this has required a corresponding reduction in the transistor oxide thickness to provide sufficient current drive at the reduced supply voltages. To further reduce the leakage current, the stacking effect is used by switching off the stack transistors when the memory is ideal. The transistors have been lowered which also contributes to leakage currents and reduces the battery life dramatically. Static power consumption is a major concern in nanometer technologies. There are many sources of sub-threshold leakage flow in MOS transistors. The authors in [4] examine the various SRAM cell models (8T and 10T) associated with the conventional 6T SRAM cell. Thus, this paper concludes that leakage reduction through sleep transistor method gives the best performance over the other models. In this [5] The result section concludes that the sleep transistor method is the best one because it reduces almost 98% sub-threshold leakage power as compared to the other models.

III. BASIC SRAM MODELS

A. Conventional 6T SRAM cell design

6T SRAM cell each bit in SRAM is stored on four transistors that form two cross coupled inventor. Two additional access transistors serve to control access to storage cell during read and write operation. Access to the cell is enabled by the word line which controls the two access transistor which in term control, whether the cell should be connected to the bit line BL and BLB. Static Random Access Memory (SRAM) is a type of semiconductor memory and it is volatile in nature. SRAM contains a latching circuitry to store each bit (0 or 1). The Basic 6T SRAM memory cell is shown below [6].

Two NMOS pass transistors are used to control the access to the cell during write operations and these are connected through the bit lines and word line [7]. Here there are two nodes Q and QB which store two alternate bits 0 and 1 and vice-versa. For the accurate and proper operation of the SRAM cell, the sizes of the transistors are designed properly.

1) 6T SRAM Write Operation

For the proper write operation, bit line BLB is kept at '1' and bit line BL is kept at '0'. The word line will always be high for the proper write operation. By choosing the proper size of the transistors, the BLB and BL line data would be transferred to nodes QB and Q[8]. For the write operation, assume that '1' is stored at node Q and '0' is stored at node QB. The transistors M1 and M5 are 'ON' and transistors M3 and M4 are in 'ON' state [9]. If we select BLB=1 and BL=0 then these node voltages ('1' and '0') .

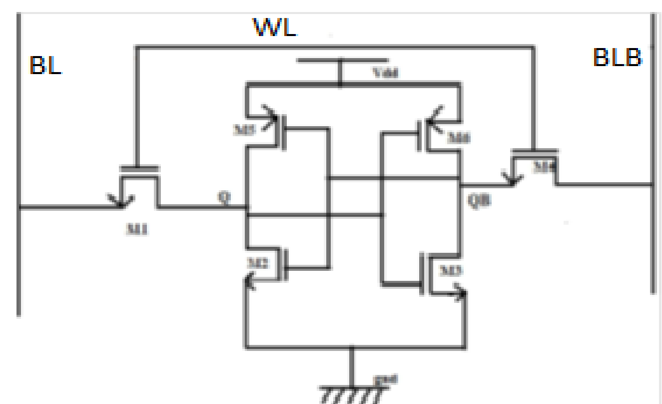


Fig. 6TSRAM Cell

ISSN: 2278 – 7798 All Rights Reserved © 2015 IJSETR

B. 8T SRAM Model

This is similar to that of 6T SRAM cell except that there are additional stack transistors below the NMOS transistors. The additional stack NMOS M7 and M8 transistors increase the threshold voltage (V_{th}) in order to reduce the sub-threshold current so that the leakage power will be reduced. Some leakage reduction models based on stack effect are in [10].In Fig. six transistors (M2, M3, M5, M6, M7 and M8) are cross-coupled [11].

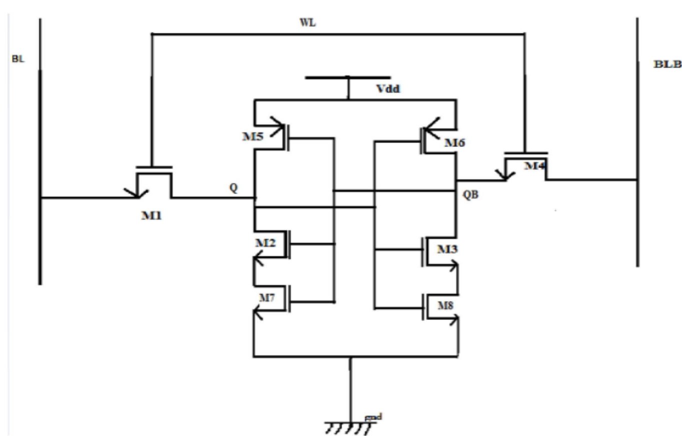


Fig. 8TSRAM Cell

C. 10T SRAM Model

In 10T SRAM model there are two PMOS (M5 and M6) and two NMOS (M9 and M10) transistors connected to the conventional 6T SRAM circuit in a 'stack' form. In Fig. eight transistors (M2-M3, M5-M6, M7-M8 and M9-M10) are cross-coupled. The pair of M5-M6 and M9-M10 are called leakage control transistors. Here two leakage control transistors NMOS (M9 and M10) and PMOS (M5 and M6) are connected with two symmetrical invertors. Here in Fig. drain terminals of both the transistors (M7 and M2) or, (M8 and M3) are connected to the nodes Q and QB and produce output voltages, respectively. By the properties of leakage control transistors (M5-M6) and (M9-M10), they will work near its cut-off region, so their resistances will be lesser than their OFF resistances, thus allowing a little conduction [12]. Even though the resistances are not as high as their OFF state resistances, they increase the resistance from V_{dd} to ground path, controlling the flow of lower leakage currents, resulting in leakage power reduction.[13].

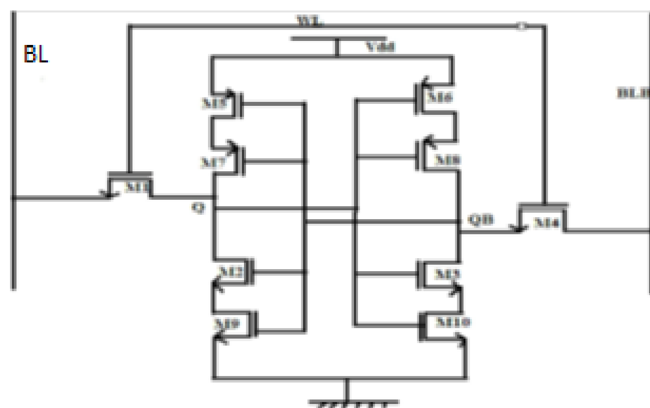


Fig. 10TSRAM Cell

IV. LEAKAGE CONTROL SRAM MODELS

In this section instead of stack transistors sleep transistor approach is used. Sleep transistors are the two extra transistors connected to the SRAM load circuit.

A. 6T SRAM with sleep transistors

Solutions for leakage reduction are required at both process technology and circuit levels [14]. One of the method at circuit level to reduce the leakage power is by adding two sleep transistors in 6T SRAM circuit. So, leakage power is reduced in a stand-by mode when sleep transistors are in cut-off state [15]. In below Fig., the NMOS sleep transistor (M8)

ISSN: 2278 – 7798
All Rights Reserved © 2015 IJSETR

is connected to V_{dd} and the PMOS sleep transistor (M7) is connected to ground. In the active mode of operation, both the sleep transistors NMOS (M8) and PMOS (M7) pass transistors' property; the voltage at the source node of M8 would be V_{dd}-V_{th} whereas the voltage at the source node of M7 would be ~V_{th}. In the stand-by mode of operation both the sleep transistors M8 and M7 are turned off and these transistors provide very small sub-threshold leakage current flows.

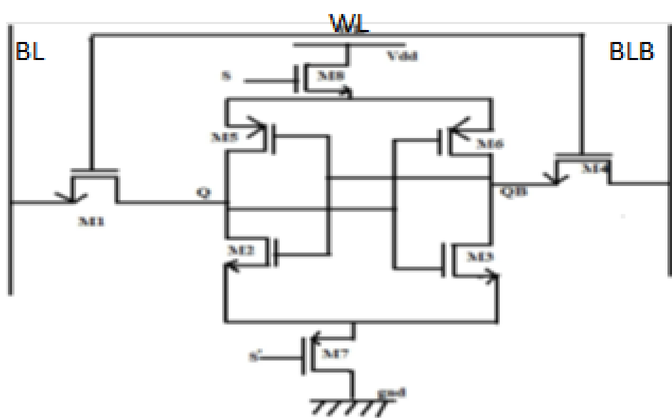


Fig. 6T SRAM Sleep Transistors

B. 8T SRAM with Sleep Transistors

In this section, method of 8T transistors with sleep transistors is discussed. Here two sleep PMOS (M7) and NMOS (M10) transistors are connected with pull-up (M5 and M6) and pull-down (M2 and M3) networks, respectively. In the basic 8T model, the leakage reduction is due to decrease in threshold voltage (V_{th}) and due to stack effect of NMOS (M8 and M9) transistors in pull-down network.

In below Fig., the NMOS sleep transistor (M10) is connected to V_{dd} and the PMOS sleep transistor (M7) is connected to ground. In active mode of operation both the sleep transistors M7 as well as the M10 are turned on. So, the source terminal voltage of the NMOS (M10) would be ~(V_{dd}-V_{th}) and the source terminal of the PMOS (M7) would be ~V_{th}. In stand-by operation the basic SRAM load circuit is disconnected from the supply voltage. So, due to the higher impedance path is formed between V_{dd} to ground, a very small sub-threshold leakage current flows. The technique is called forced sleep technique.

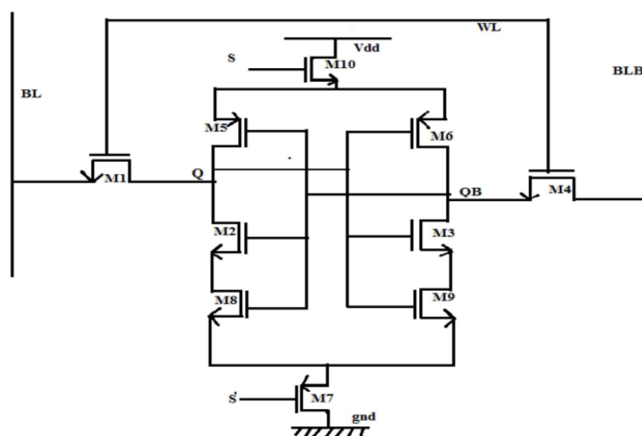


Fig. 8T SRAM Sleep Transistors

C. 10T SRAM with Sleep Transistor

Here two PMOS M5 and M6 transistors and two NMOS M9 and M10 transistors are connected in stack form. There are eight cross-coupled transistors connected serially. There are two sleep transistors (M11 and M12).

In below Fig., the NMOS sleep transistor (M11) is connected to V_{dd} and the PMOS sleep transistor (M12) is connected to ground [17]. During active mode both NMOS and PMOS sleep transistors (M11 and M12) are turned "ON". So NMOS (M11) transistor is connected to V_{dd}(S=1). During sleep mode, it is not efficient in passing V_{dd} so when the inputs are low, the output voltage is reduced to ~ (V_{dd}-V_{th}). Smaller leakage current I_{ds} will flow through the transistors and the stack

ISSN: 2278 – 7798
All Rights Reserved © 2015 IJSETR

transistors also. The PMOS (M12) is connected to ground. When the input signal (S'=1) is high, the output is ~V_{th}. Thus smaller leakage current I_{ds} will flow through the transistors and leakage is reduced.

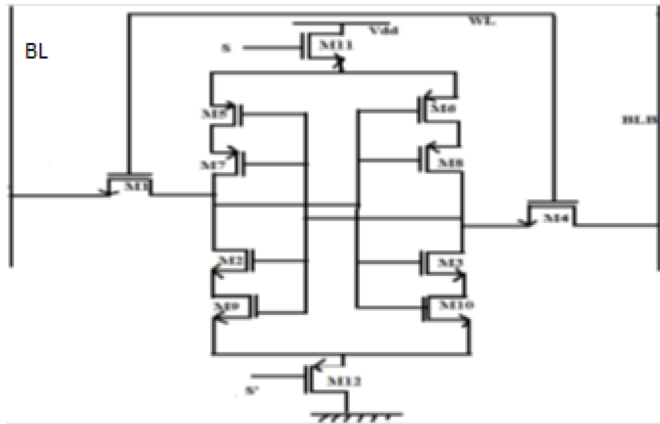
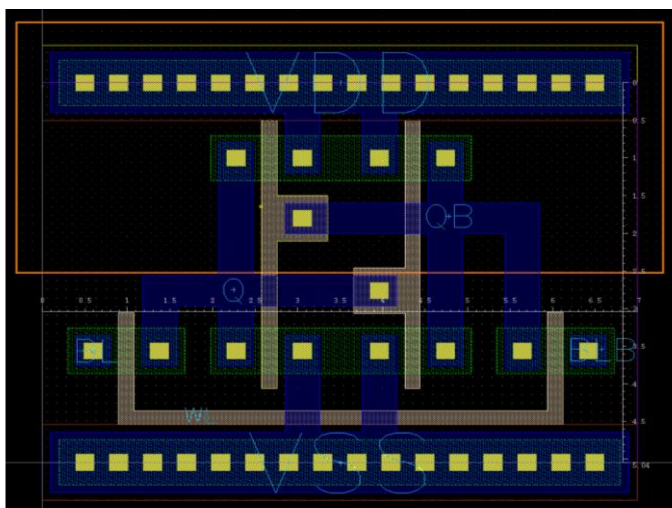


Fig. 10T SRAM Sleep Transistors

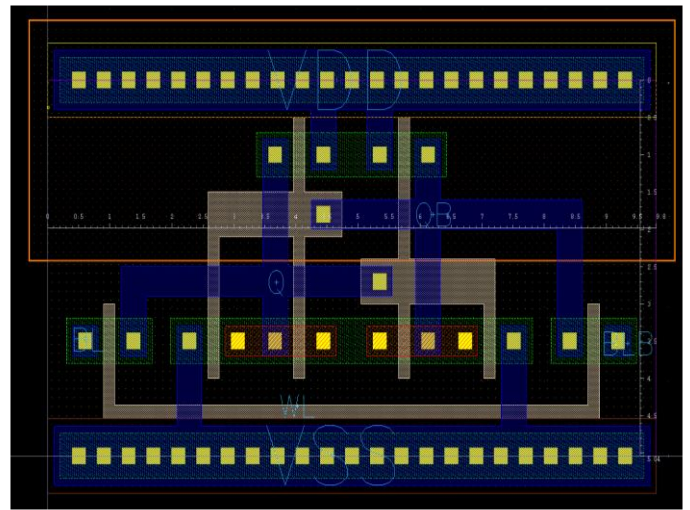
V. Area Reduction SRAM Cells Layouts

Now a day's Space is a mainly important because integrated chip is designed in micrometer ranges. This type of SRAM Cell Layouts Designs Almost Reduced Space better than other type of designs Layouts.

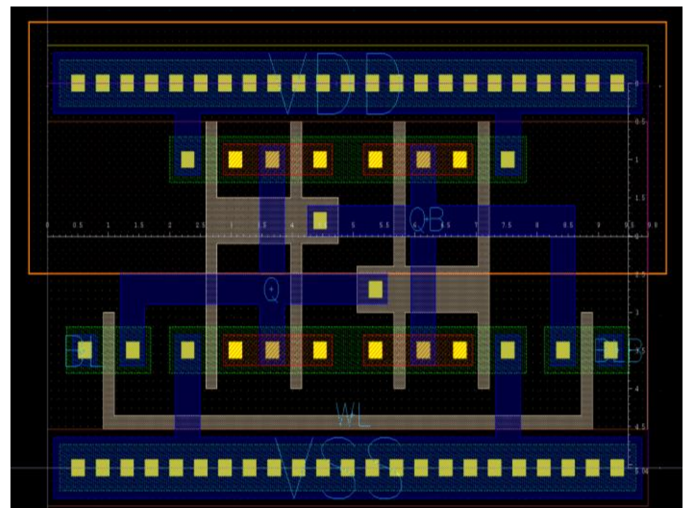
A. 6T SRAM Cell Layout
This type consumed less space. This is the Basic Layout of SRAM Cell Design.



B. 8T SRAM Cell Layout

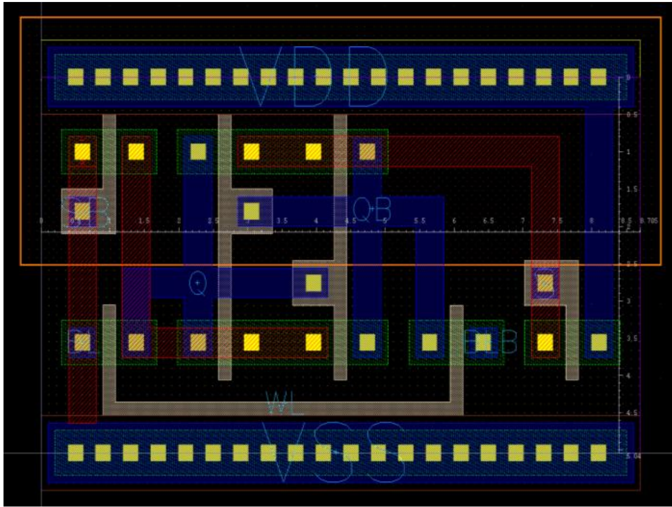


C. 10T SRAM Cell Layout

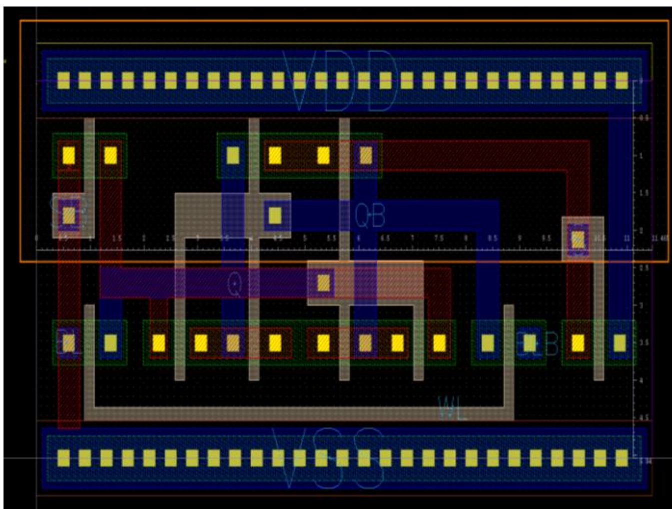


D. 6T SRAM Sleep Transistor Layout

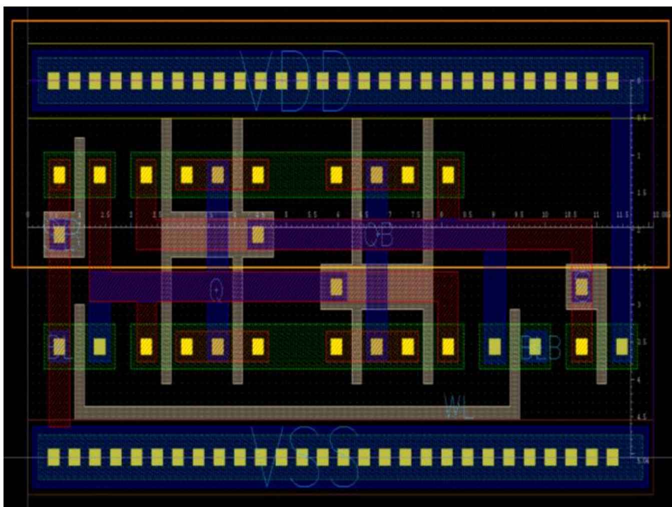
ISSN: 2278 – 7798 All Rights Reserved © 2015 IJSETR



E. 8T SRAM Sleep Transistor Layout



F. 10T SRAM Sleep Transistor Layout



VI. RESULTS

In this paper Cadence virtuoso simulator is used to find out the sub-threshold leakage reduction in CMOS SRAM cell models with 180nm technology. Table shows, leakage current is very high for the basic SRAM models (6T, 8T and 10T). SRAM models with sleep transistors yields far better performance over the basic SRAM models. Similarly, the 8T SRAM sleep transistor model yields almost 98% leakage current and power reduction over basic 8T SRAM models and for 10T model, sleep transistor model yields almost 99% reduction of leakage current and leakage power over basic 10T SRAM model.

TABLE

comparison of leakage power for various cells

circuit (180nm Technology)	Total Write Leakage Current (pA)	Total Write Leakage Power (pW)
6T SRAM Cell [18]	82.26	148.1
6T SRAM with sleep transistors	0.251	0.452
8T SRAM cell model [19]	19.39	34.9
8T SRAM with sleep transistors	0.218	0.392
10T SRAM model [20]	12.77	22.99
10T SRAM with sleep transistors	0.1915	0.344

ISSN: 2278 – 7798
All Rights Reserved © 2015 IJSETR

VII. CONCLUSION

Study of the results show that, 10T SRAM with sleep model is the best technique and it yields more than 98% leakage power reduction as compared to the basic 10T SRAM cell and almost 99% leakage power as over the basic 6T SRAM cell, which is the major advantage of short channel devices. The sleep circuits reduce leakage power when these operate in "stand-by mode" due to inefficient passing of the voltages (pass-transistors property). In this paper as the number of transistors increase leakage power reduces but area and delay also increase more and more. Hence the authors conclude the proposed SRAM circuits specially sleep transistor circuit, used for low power designs can be used for low power applications.

VIII. REFERENCES

[1]. Y. Taur and T. H. Ning, "Fundamentals of Modern VLSI Devices", New York, USA: Cambridge University Press, 1998, ch. 3, pp. 120-128.

[2]. Kim. N, Austin. T, Baauw.D, Mudge. T, Flautner. K, HU. J, Irwin. M, Kandemir.M, and Narayanan.V, "Leakage Current: Moore's Law Meets Static Power", IEEE Computer, vol. 36, pp. 68-75, December 2003.

[3]. International Technology Roadmap for Semiconductors by Semiconductor Industry Association, 2002. [online] Available: http://public.itrs.net.

[4]. soumyaGadag,raviraj D. Chougla, "Design and Analysis of 6T SRAM Cell with Low power Dissipation",International Journal of Engineering Research and Application(IJERA),vol. 2,Issue 6,pp.1695-1698, Nov.-Dec.2012.

[5]. TajrianIzma, Parag Barua, Md. RejaurRahman,and Priyanka Sengupka, "Novel Approaches to Low Leakage and Area Efficient VLSI Design" Ph.D thesis, Dept. Electrical and Electronics Eng., BARC Univ., Dhaka, August 2011.

[6]. Neeraj Kr. Shukla, shilpi Birla, R.K Singh, and Manisha Pattanaik, "Speed and Leakage power tran-off in Various SRAM Cirtuits", International Journal of Computer and Electrical Engineering (IJCEE),Singapore,Vol.3,No.2,Apr.2011, pp.244-249.

[7]. KeivanNavi, RoshanakZabihi, Majid Haghparast, TourajNikobin, "A Noval Mixed Current and Dynamic Voltage Full Adder", World Applied Sciences Journal, Vol.4,no.2,pp. 289-294,2008.

[8]. A.DeepakLourts, and L. Dhulipalla, "Design and implimentation of 32nm FINFET based 4*4 SRAM cell array using 1-bit 6T SRAM",International Conference on Nanoscience, Engineering and Technology (ICONSET),pp.177-180,280,28-30 November 2011.

[9]. KavithaKhare, NilayKhareKulhade, and pallavi Deshpande, "VLSI Design and Analysis of Low Power 6T SRAM Cell Using Cadence Tool",InternationalConference on Semiconductor Electronics (ICSE),pp.117-1 21,Malaysia, November 2008.

[10]. S. Narendra, V.DE,S.Borak, D.A. Antoniadis, and A.P. Chandrakasan, "Full-Chip Subthreshold Leakage Power Prediction and Reduction Techniques for Sub-0.18um CMOS,"IEEE Journal of Solid-State Circuits, Vol.39,n0.2,pp.501-510,Febrary 2004.

[11]. Z.Chen,M.Jhonson,L. Wei and K. roy, "Estimation of Standby Leakage Power in CMOS Circuits, Considering Accurate Modeling of Transistor Stack",Internationalsymoposium on Low Power Electronics and Design, pp.239-244,August 1998.

[12]. S.Mutoh,T.Douseki,andY.Matsuya, "1v Power Supply High-speed Digital Circuit Technology with Multithreshold-Voltage CMOS",IEEE J.Solid-state ,Circuits,vol.30,pp.847-854,Aug.,1995.

[13]. Atluri Jhansi rani, K. Harikrishore, Fazal Noor Basha, and V.G. SanthiSwaroop, "Designing and Analysis of 8 Bit SRAM Cell with Low threshold Leakage Power" International

ISSN: 2278 – 7798 All Rights Reserved © 2015 IJSETR

Journal of Modern Engineering Reseach (IJMER), vol.2,Issue.3, pp.733-741, May-June 2012.

[14]. M.Powell ,S.H.Yang,B.Falsafi, K.Roy and T.n. Vijay Kumar, "Gated-Vdd: A Circuit Technique to Reduce Leakage in Deep Submicron Cache Memories",International Symposium on Low Power Electronics and Design,pp. 90-9, July 2000.

[15]. Andrei Povlov, O. Semenov and ManojSachdev, "Sub-quarter micron SRAM cells stability in low-voltage operation: a comparative analysis" ,IEEE International Integrated Reliability Work Shop Final Report,pp.168-171,21-24 october 2002.

[16]. M.Johnson, D.Somasekhar, L.Chiou, and K.Roy, "Leakage control with efficient use of transistor stacks in single threshold CMOS", IEEE Trans. on VLSI Systems, vol.10,no.1, pp.1-5, Feb 2002.

[17]. J.c Park, V.J. Mooney III, and P. Pfeiffenberger, "Sleep Stack Reduction of Leakage Power," proceeding of the International Workshop on Power and Timing Modeling, Optimization and Simulation, pp.148-158,September 2004.

[18]. ParidhiAthe and S. Dasgupta, "A Compararative Study of 6T,8T and 9T Decanano SRAM Cell", IEEE Symposium on Industrial Electronics and Application (ISIEA 2009),vol.2,pp.889-894,Kuala Lumpur Malaysia,October 4-6,2009.

[19]. Weijie Cheng, BaolongZhou,Huarong Zheng, and Yeonbae,Chung,"Stack-Transistor Based Differential 8T SRAM Cell for Embedded Memory Application", IEEE International Conference on Electron Devices and Solid State Circuit (EDSSC 2012), pp.1-2,Bangkok, December 3-5 2012.

[20]. A.Feki , B.Allard , D. Turgis , J. Lafont , and L.Ciampolini , "Proposal of a new ultra low leakage 10T Sub-Threshold SRAM bit Cell ", International SOC Design Conference (ISOCC 2012), pp.470-474, jeju Island , November 4-7 2012.

ISSN: 2278 – 7798 All Rights Reserved © 2015 IJSETR