Low power high speed hybrid CMOS Full Adder By using sub-micron technology

Ch.Naveen Kumar[1]
Assistant professor,ECE department
GURUNANAK institutions technical campus
Hyderabad-501506

A.V. Rameshwar Rao[2]
Assistant professor .ECE department
GURUNANAK Institutions technical campus
Hyderabad-501506

***Abstract*—In the recent year, many other new circuits are proposed using less number of transistors with less delay and extremely low power requirement. An adder consisting with less transistors don't give full swing outputs for all input combinations and there is difference in output level for various combinations and these circuits have very low driving capabilities. other circuits also are proposed in but they are doing not give full swing output for all input combinations and power requirement is more.. The carry select adder is meant using hybrid CMOS full adder logic style and proposed full adder by dividing it in three modules in order that it are often optimized at various levels.[1] First module is an XOR-XNOR circuit, that generates full swing XOR and XNOR outputs at the same time and have an honest driving capability. It also consumes minimum power and provides better delay performance. Second module is total circuit that is additionally a X-OR circuit and uses carry input and also the output of the primary module as input to get total output. Third module may be a carry circuit which uses the output of the primary stage and other inputs to get carry output. within the new full adder design new full adder circuit is proposed which reduce the facility consumption, delay between perform to hold in and PDP by 10 to 100%. Simulations area unit disbursed on LT-PICE&ELECTRIC mistreatment TSMC 0.45µm CMOS Scale. So far designing the high performance arithmetic circuit's minimization of the power and delay of the full adder circuit is required**

Keywords: One bit CMOSFull Adder, XOR , XNOR Modules.

I. INTRODUCTION

The new variety of low power CMOS Full Adder has been designed and XOR and XNOR modules unit participating within the important role for coming up with the carry opt for full adder. several logic styles for coming up with the whole adder are projected. In arithmetic of full adder commonly single CMOS structure is used for the whole style, just like the quality static CMOS full adder is based on regular CMOS structure with commonplace pull -up and pull-down [5]transistors providing good output results foremost disadvantage of this circuit is high input capacitance and use no. of PMOS, due to that the speed of this structure is degraded. The speed of dynamic. its several demerits like charge sharing, high clock load, higher switch activities and lower noise immunity and it wants high power for driving the clock lines. Another logic styles unit transmission-gate full adder (TGA) and transmission perform full adder (TFA) based totally upon transmission gates and transmission perform theory. These full adders unit really low power overwhelming, but have really low driving capabilities. Full adder could also be a basic building block for various arithmetic circuits like multipliers, compressors, comparators therefore on. the ability demand and output delay of these circuits is greatly relying upon the ability demand and delay of the whole adder circuits. thus for coming up with the high performance arithmetic circuits, decrease of the ability and delay of the whole adder circuit is required.

II. HYBRID –CMOS LOGIC DESIGN

In hybrid-CMOS design,[3] the XOR and XNOR A of and B inputs because the intermediate signal at the output of module I. These input signals and Cin are accessible for the input of module II and module III. thus a replacement expression for total and carry exploitation XOR output H and XNOR output HB.Let us discuss well concerning the three Modules.

A..Module-I

This circuit is widely used in hybrid CMOS logic style. This circuit requires low power and provides low delay and due to the feedback transistors at the output connected with supply voltage and ground provide good driving capability. But some combination of inputs such as "00" and "11" it provides little bit higher delay. When H will be at logic 0 H' will be at logic 1, both transistors will be on and output will be connected to C_{in}, So when C_{in} will be at logic '1' output will be connected to logic '1' and when it will be at logic '0' output will also be connected to logic '0'.

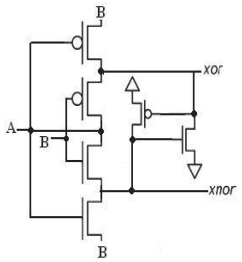

Fig.1 Module I circuit (a)

ISSN: 2278 – 7798

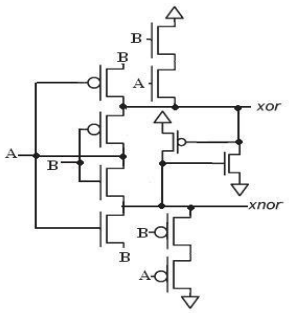

Fig.2 Module I circuit (b)

Both the transistors will be in off state for H to be at logic '1'. When the inputs H and C_{in} will be at logic '1', then the output is low, it is implemented by connecting two NMOS in series with their gate terminals connected to H and C_{in}, source terminal of one of the NMOS is connected to the grounded and the source terminal of other is connected to the output . Similarly, when H is at logic '1' and C_{in} is at logic '0', the output is at logic 1 so we use two PMOS in series with source terminal of one of the PMOS at logic high, drain terminal of other PMOS at output and the gate terminals are connected with H and C_{in} respectively.

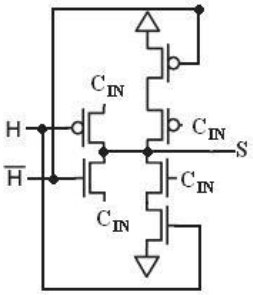

Fig.3 Module I circuit (c)

When both inputs will be at logic '1' then output will be connected to ground and the output will be at logic '0', when H will be at logic '1' and C_{in} will be at logic '0' both inputs Hǫ and C_{in} will be at logic '0' and both transistor will be on and output will be connected to power supply and we get logic '1' at the output.

B.Module-II

In the designing of circuit we try to avoid the use of inverters to reduce the power consumption and the logic high passes by PMOS while Logic low passes by NMOS to get the minimum delay .

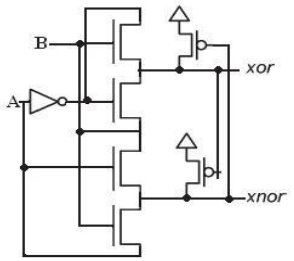

Fig.4 Module II Proposed circuit (c)

C.Module-III

Module III circuit is a multiplexer which select C_{in} if H is at logic '1' else selects A or B as the output C_{out} . In the proposed circuit we use transmission gate with H and H'at the gate terminals of NMOS and PMOS[2] respectively to pass the C_{in} to C_{out} for H at logic high or when other inputs A and B are at different logic level. When the H is at logic '0' or both inputs A and B are at same logic level we have to pass any of these inputs to the output. So we use one PMOS and one NMOS to pass input A by one transistor and other input B by another transistor. By the use of these two inputs from two sides it improves the performance of the circuit.

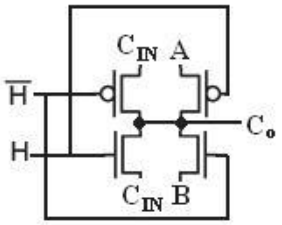

Fig.5 Module III Proposed circuit

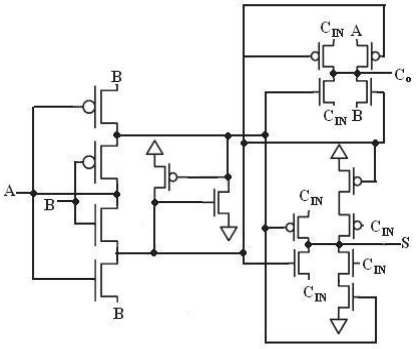

Fig . 6 Proposed Full Adder Circuit

III. PROPOSED 16 TRANSISTOR BASED FULL ADDER

A basic full adder has three inputs and two outputs which are sum and carry. Full adder cell is designed with CPL and Multiplexing Control Input technique for both sum and carry operations. The Sum and Carry operations are based on the equations 1 & 2 mentioned below:

Sum = A⊕ B⊕ C (1)

Carry = (A⊕ B)C + AB (2)

Sum equation contains XOR gates whose design using CPL logic is desired for low power system, whereas the Carry is designed as per equation. The inputs A, A's complement (A'), B, and B's complement (B') are fed to the pass transistors and forms an XOR logic gate. These four inputs construct an XOR logic operation at the transistor level, which is designed using two transistors.

To reduce the amount of transistors, the output of the gate (A⊕ B) is fed through a NOT gate from the differential node to the pass transistors as a management input. Whereas, Cin is treated as variable input, that's fed through the pass semiconductor unit supply terminal. At now, the practicality performed by the circuit is reminiscent of the add operation, sum A⊕B⊕C, and 6 transistors are used. As mentioned

ISSN: 2278 – 7798

earlier, the amount of transistors within the carry operation may be reduced by taking A⊕ B as the input from the add operation circuit AND with Cin so as to turn out the operation equivalent to (A⊕ B)Cin, that solely uses another 2 transistors. Meanwhile, the inputs A, A', B, And B' are fed into pass transistors so as to provide an AND computer circuit, that represents the AB operation .The dissipation of power that happens throughout the active mode of the circuit is active power. This active power consists of dynamic power additionally as the static power. It is measured by giving input vectors to the circuit, then shrewd the typical power dissipation and examination the result with the bottom adder i.e. standard 1-bit CMOS

IV.Implemented CARRY SELECT ADDER using new full adder :

The carry-select adder typically consists of 2 ripple carry adders and a electronic device. Adding 2 n-bit numbers with a carry-select adder is finished with 2 adders (therefore 2 ripple carry adders) so as to perform the calculation double, just one occasion with the idea of the carry being zero and therefore the alternative forward one. when the 2 results are calculated, the right add, still because the correct carry, is then designated with the electronic device once the right carry is known[8].The number of bits in every carry choose block are often uniform, or variable. Within the uniform case, the optimum delay happens for a block size of . Once variable, the block size ought to have a delay, from addition inputs A and B to the do, capable that of the electronic device chain leading into it, so the do is calculated simply in time. The delay comes from uniform size, wherever the perfect range of full-adder components per block is capable the root of the amount of bits being supplementary, since that may yield Associate in Nursing equal range of MUX delays.

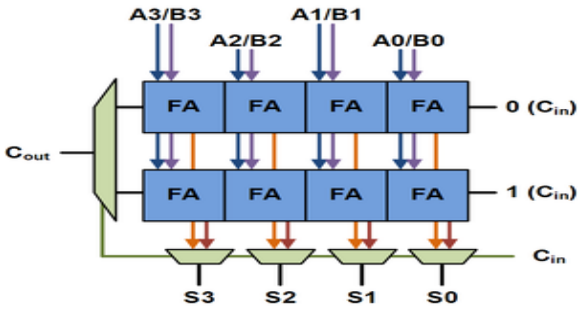

Fig.8 4-bit Carry Select Adder

V .THE NEW FULL ADDER

The new improved 16T adder cell requires only 16 transistors to realize the adder function shown in figure. 4,It produces the better result in threshold loss, speed and power by sacrificing four extra transistors per adder cell. Even though the transistor count increases by four per adder cell, it reduces the threshold loss problem, which exists in the SERF by inserting the inverter between XOR Gate outputs to form XNOR gate.

The newly proposed adder implement the Sum using XNOR-XNOR and Cout using PMOS – NMOS We can also build to produce Cout using NMOS-NMOS and PMOS-PMOS. But the delay and power dissipation of PMOS-NMOS is better than other two kinds of producing Cout .The proposed XNOR gate is designed by putting inverter at the output of the XOR gate in order to improve the threshold loss problem, which exists in the SERF adder. Out of the three methods, PMOS-NMOS based Cout gives the better result in power, speed and threshold loss problem.

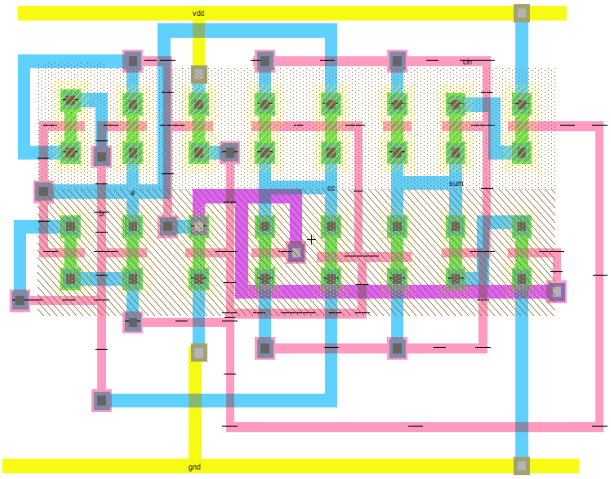

Fig 9.16T Full Adder lay out

Totally eight adders including the SERF adder are taken for comparison with the newly proposed adder. These adders are compared with respect to their power consumption and total delay by providing all the possible input vector combinations. The results proved that the newly proposed adder is efficient as it consumed the least power and eliminated the threshold loss problem. The present research work has presented a new improved 16T adder cell to construct full adders using only 16 transistors. Based on our extensive simulations, the new improved 16T adder cell consume considerably less power in the order of micro watts and has 48% higher speed and reduces 50% threshold loss problem compared to the previous different types of transistor adders.

VI. LT-SPICE TOOL

The simulation and synthesis are carried out for all the designs. The performance evaluation of existing adder designs and the proposed adder designs is carried out using LT SPICE tool in 90 nm and 45 nm scale . All the parameters such as delay, area, total power, and power-delay product are tabulated.

LT-spice is a high performance SPICE simulator, schematic capture and waveform viewer with enhancements and models for easing the simulation of switching regulators. Our enhancements to SPICE have made simulating switching regulators extremely fast compared to normal SPICE simulators, allowing the user to view waveforms for most switching regulators in just a few minutes. Included in this download are LT-spice , Macro Models for 80% of Linear Technology's

ISSN: 2278 – 7798

switching regulators, over 200 op amp models, as well as resistors, transistors and MOSFET models

VII SIMULATION RESULTS

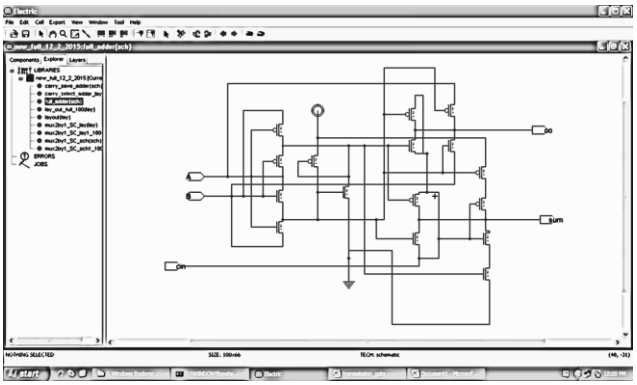

Fig (a) .Full adder Schematic

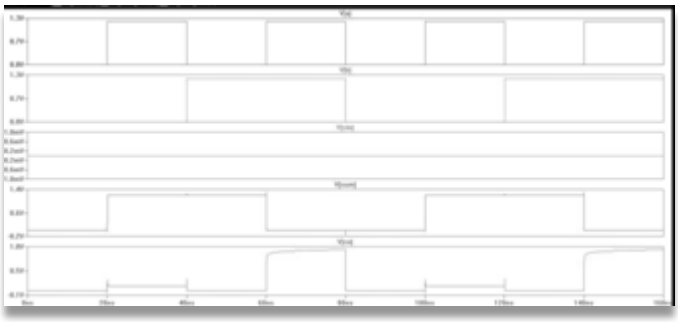

Fig (b) Simulation Result of Fulladder

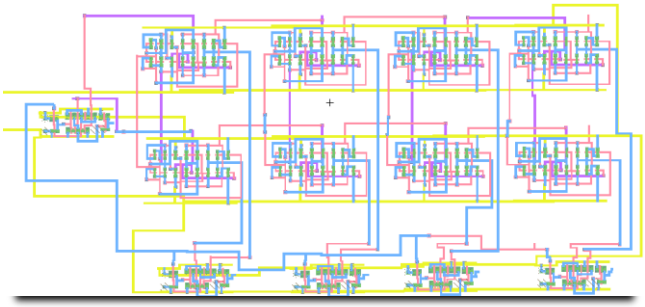

Fig (c) Carry select adder layout

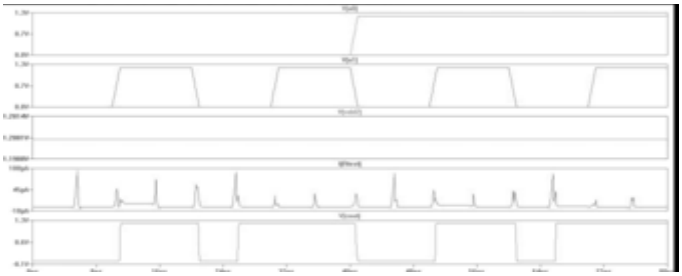

Fig (d) Simulation Result of carry select adder

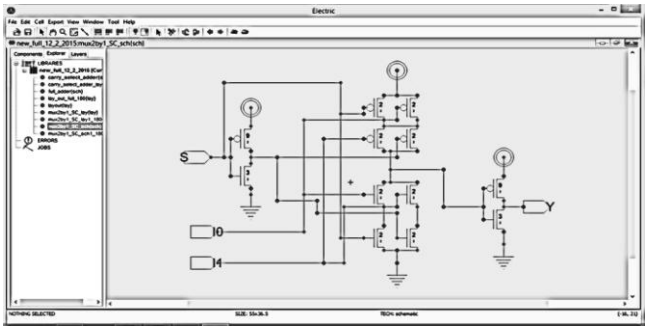

Fig (e) Schematic Of Mux 2_1

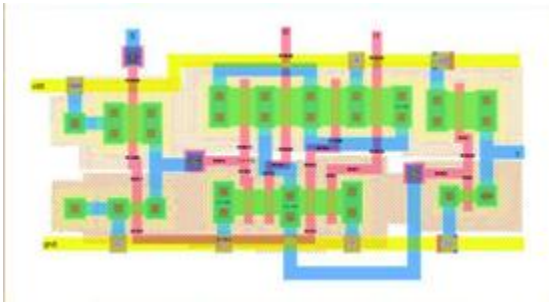

Fig (f) Layout Of Mux 2_1

VIII .TABLE

	FULL ADDER OF180 NM	FULL ADDER OF 130NM
POWER(uw)	1.5168	0.036
DELAY SUM	0.1025	0.075
DELAY CARRY	0.115	0.094
PDP SUM	0.155472	0.027
PDP CARRY	0.174432	0.03384

Table .1

VIII. CONCLUSION

Hybrid-CMOS style vogue provides a lot of freedom to the designer to pick out completely different modules I a circuit relying upon the applying. victimization the adder categorization and hybrid-CMOS style vogue, several full adders are often designed. as an example, a completely unique full adder hybrid-CMOS design vogue is given during this paper that targets low PDP. The planned hybrid-CMOS full adder has higher performance than most of the quality full-adder cells attributable to the novels style modules planned during this paper. It performs well with offer voltage starting from one.2V to 1.8V. once embedded in an exceedingly parallel adder chain, it outperforms all the opposite adders creating it appropriate for larger arithmetic circuits.

ISSN: 2278 – 7798

REFERENCES

[1] N. Weste, and K. Eshranghian, "Principles of CMOS VLSI Design: A System Perspective," Reading MA: Wesley, 1993.

[2] Sung-Mo Kang, and Y. Leblibici, "CMOS Digital Integrated Circuits: Analysis and Design," Tata McGraw Hill, 2003.

[3] J.Rabaey, "Digital Integrated Circuits: A Design Prospective," Prentice-Hall, Englewood Cliffs, NJ, 1996.

[4] R. Zimmermann and W. Fichtner, "Low-power logic styles: CMOS versus pass-transistor logic," IEEE Journal of Solid-State Circuits, vol. 32, no.7, pp. 1079–1090, Jul. 1997.

[5] N.Weste and K. Eshraghian, "Principles of CMOS VLSI design," in A System Perspective. Reading, MA: Addison-Wesley, 1993.

[6] N. Zhuang and H. Wu, "A new design of the CMOS full adder," IEEE Journal of Solid-State Circuits, vol. 27, no. 5, pp. 840–844, May 1992.

[7] D. Radhakrishnan, "Low-voltage low-power CMOS full adder," IEEE Proc. Circuits Devices Syst., vol. 148, no. 1, pp. 19–24, Feb. 2001.

[8] M. Zhang, J. Gu, and C. H. Chang, "A novel hybrid pass logic with static CMOS output drive full-adder cell," in Proc. IEEE Int. Symp. Circuits Syst., May 2003, pp. 317–320.

Mr. CH.NAVEEN KUMAR receivedB.Tech Degree in Electronics and Communication Engineering and M.Tech Degree in VLSI design .Currently working as Assistant Professor in Department of Electronics and Communication Engineering,GURUNANAK institutions Technical campus ,Hyderabad. And previously worked asa Application engineer in VLSI domain.

Mr. A.V.RAMESHWAR RAO received B.Techdegree in Electronics and Communication Engineering and completedM.Tech in VLSI&ES from SCIENT institute of Technology ,Hyderabad. Areas of interesting in low power VLSI systems. Presently working as a assistant professor in the department of ECE in GURUNANAK institutions technical campus

ISSN: 2278 – 7798