COMPARATIVE ANALYSIS OF CARBON NANOTUBES AS VLSI INTERCONNECTS

Priya Srivastav, Asst. Prof. Anup Kumar

***Abstract*— Carbon nanotubes have been proposed as the future VLSI interconnect material in this paper. The performance comparison of copper and CNT interconnect is done on the basis of delay and power parameters. The delay and power of CNT and copper interconnect is calculated using 45 nm technology. Both delay and power are calculated by RC and RLC delay models.**

***Index Terms*— Carbon nanotube (CNT), Multiwall carbon nanotube (MWCNT), Singlewall carbon nanotube (SWCNT)**

1. INTRODUCTION

Throughout most of the past history of integrated circuits interconnects were not having so much of importance but with the introduction of deep submicron technologies this scenario for interconnect has been completely changed [1]. Earlier gate delay was having much importance than interconnect delay but now-a-days as the feature size is reducing the interconnect delay is becoming more important as compare to gate delay. This is because for higher frequencies interconnect no longer behaves as a simple resistor but it also has associated capacitance and inductance. Interconnect is generally divided into three types based on their length of wires which are local, semiglobal and global. Local interconnects are the one used for short distance connections at device level. Semiglobal interconnect are used to connect devices within a block. Similarly global interconnects are used to connect long interconnects between the blocks including power, ground and clocks. A VLSI chip is generally characterized by the parameters like parasitic resistance, capacitance and inductance. Leaving some defects like scaling, skin effect, electron surface scattering, electromigration and grain boundary effects under the constraints of increasing size, power consumption, crosstalk and delay. Reason behind the replacement of copper has been reviewed. With the reduction in feature size and rise in frequencies copper faces various challenges. To meet out with these challenges various alternatives have been introduced by various researchers. Carbon nanotubes have come into picture as prominent interconnect to replace copper. The applicability of carbon nanotubes as VLSI interconnects has also been discussed.

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Priya Srivastav *Department of Electronics and Communication Engineering, Ajay Kumar Garg Engineering College,. Ghaziabad, India,*

Asst. Prof. Anup Kumar*, Department of Electronics and Communication Engineering, Ajay Kumar Garg Engineering College, Ghaziabad, India,*

2. WHY COPPER REPLACED ALUMINIUM INTERCONNECT

For several semiconductor technologies aluminium was used as on chip interconnect material but for technologies below submicron aluminium started to cause signal delay which also affected the reliability of the integrated circuit. The interconnect delay is mostly affected by resistive and capacitive part. Various alternatives to aluminium were considered in 1990s to reduce the RC delay caused by aluminium. Silver, gold and copper were found the most appropriate interconnect material which could replace aluminium due to their low electrical resistivity [2].
Although gold has high resistance to electromigration but it also creates deep levels in band gap due to diffusion in silicon and thus affects the electronic properties of the device. Similarly silver also creates deep levels in band gap and diffuses in SiO_2 and also silver has low resistance to electromigration due to its low melting point. Copper appeared to be most appropriate material because it has half of the resistivity (1.7 mWcm) as compare to aluminium/0.5 % Cu alloys (3.0 mWcm) and with electromigration of the order of ten times better than aluminium. Adding to more merits copper has a higher melting point (1357K) than aluminium (933K) which gives advantage in electromigration and stress migration as well. Today for advanced integrated circuits copper is widely used as on chip interconnects.

3. CHALLENGES FOR COPPER INTERCONNECTS

With the reduction in feature size and introduction of higher frequencies for the integrated circuits the requirement of lower resistance and higher bandwidth have become major concern for interconnects. It was realized in earlier decade that even copper is not capable of fulfilling the demands of high speed interconnects. As the dimension reaches to electron mean free path of the interconnect the effect of surface scattering and grain boundary effect is increased. Simultaneously due to scaling technologies copper also faces increased delay problems as well as power dissipation problems. Copper also faces various problems at higher frequencies which are skin effect, dispersion, electromigration and signal degradation.

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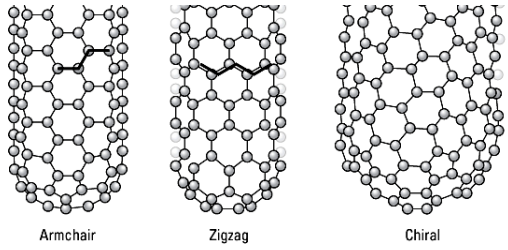
4. FUTURE INTERCONNECT: CARBON NANOTUBE

The performance and reliability of an integrated circuit is largely affected by interconnects. Carbon nanotubes have some unique properties which can help to meet out with the major interconnect challenges [3, 4]. The properties which make carbon nanotubes most eligible candidate for the replacement of copper are large current conduction capacity, large electron mean free path, high mechanical and thermal stability [5, 6].

The graphene sheets rolled up into cylinders form carbon nanotubes which have diameter of the order of a nanometer. The direction in which they are rolled is known as chirality. Based on the chirality three types of nanotubes can be obtained which are named as armchair, zigzag and chiral which are shown in Fig.1 (a-c).



(a) (b) (c)

Fig. 1 Different structures of CNTs based on chirality

CNTs can be classified into single walled (SWCNT) and multiwalled (MWCNT) depending on their interconnect applications. SWCNTs can be either metallic or semiconductor depending on its chirality and the typical diameter it has is about 1nm [7]. On the other hand MWCNTs are mainly metallic and have diameters in a wide range of diameters in a wide range of a few to hundreds of nanometers. Due to the thermal conductivity as high as 5800W/mK and current carrying ability upto 10^{14}A/m^2 CNTs are the most attractive interconnect materials. The most important property which makes CNT more reliable than other interconnect material is its nature of ballistic electron flow even when the length of conductor is less than electron mean free path. Since CNT exhibits a large number of properties they can be used for various applications

5. EQUIVALENT CIRCUIT MODEL OF COPPER

The winbond TSM model [8] is used for the calculation of parasitic resistance, capacitance and inductance. The model consists of global layer interconnect lines with coupling above the ground. According to the model the thickness of the interconnect is t, width is w and h is height of the interconnect which is shown in Fig. 2.

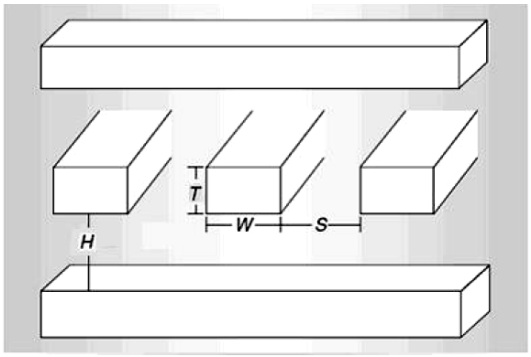


Fig. 2 Geometry of global interconnect

5.1 Equivalent Resistance

The equivalent resistance of copper having length l and resistivity ℓ is given by Eqn. 1.

$$R = \frac{\ell l}{wt} \tag{1}$$

5.2 Equivalent capacitance

The total effective capacitance of copper interconnect is given by Eqn. 2

$$C_g = \varepsilon\left[\frac{w}{h} + \left\{2.22\left(\frac{s}{s+0.7h}\right)^{3.19}\right\} + \left\{1.17\left(\frac{s}{s+1.51h}\right)^{0.76}\left(\frac{t}{t+4.53h}\right)^{0.12}\right\}\right]$$

$$\varepsilon = \varepsilon_0\varepsilon_r \tag{2}$$

Where ε_0 is dielectric permittivity and ε_r is relative dielectric permittivity of copper.

5.3 Equivalent inductance

Inductance associated with copper interconnect is given by Eqn. 3.

$$L_s = \frac{\mu_0 l}{2\pi}\left[\ln\left(\frac{2l}{w+t}\right) + \frac{1}{2} + \frac{0.22(w+t)}{l}\right] \tag{3}$$

Where mutual inductance is given by Eqn. 4.

$$M = \frac{\mu_0 l}{2\pi}\left[\ln\left(\frac{2l}{d}\right) - 1 + \frac{d}{l}\right] \tag{4}$$

Where μ_0 is the permeability of free space.

So the final equivalent circuit model for copper which is designed using parasitic is shown in Fig. 3.

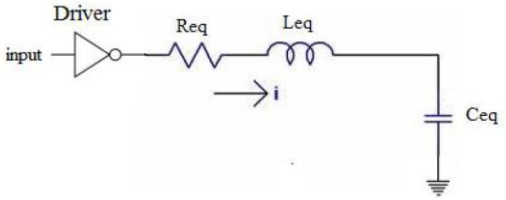


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Fig. 3 Equivalent circuit model of copper interconnect

6. EQUIVALENT CIRCUIT MODEL OF SWCNT

An isolated SWCNT on the ground plane is shown in Fig. 4. The separation between the ground and nanotube is given by d for SWCNT [10]. An equivalent circuit model for an isolated SWCNT is shown in Fig. 5.

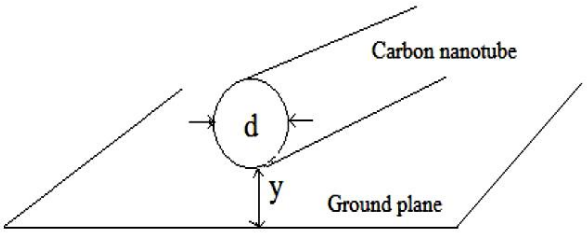

Fig. 4 CNT with diameter d, over a ground plane and distance y, below it

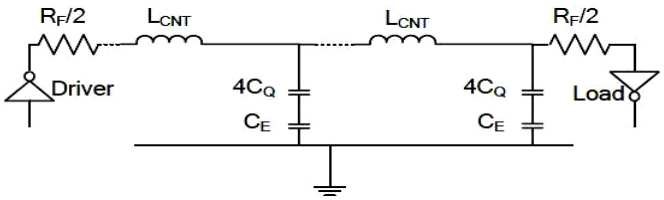

Fig. 5 Equivalent circuit model for an isolated SWCNT

6.1 Resistance of an isolated SWCNT

According to the Landauer-Buttiker formula if a 1D system has N channels in parallel then the conductance will be given by $G = \left(Ne^2/h\right)T$ [9]. Each nanotube has four conducting channel in parallel due to its spin degeneracy and sub lattice degeneracy of electrons. Thus assuming perfect contacts for ballistic SWCNT the fundamental resistance will be given by Eqn. 5.

$$R_F = \frac{h}{4e^2} \tag{5}$$

For the length less than the mean free path of electrons in a CNT the resistance will be equal to its fundamental resistance but if the length exceeds its mean free path, the formula for resistance becomes as in Eqn. 6.

$$R_{CNT} = \left(\frac{h}{4e^2}\right)\frac{L}{L_0} \tag{6}$$

Where L is the length of CNT and L_0 is the length of mean free path. The mean free path of electrons in a CNT is typically 1 μm.

6.2 Capacitance of an isolated SWCNT

CNT has two different origins for capacitance which are electrostatic capacitance and quantum capacitance. The charge stored by the CNT ground plane system is known as electrostatic capacitance and is given by Eqn. 7 in which CNT consists of diameter d and placed a distance y away from ground plane.

$$C_E = \frac{2\pi\varepsilon}{\ln\left(\frac{y}{d}\right)} \tag{7}$$

The quantum electrostatic energy stored in the nanotube is known as quantum capacitance which given by Eqn. 8.

$$C_Q = \frac{2e^2}{hv_F} \tag{8}$$

Where h is Planck's constant and V_F is the Fermi velocity.

6.3 Inductance of an isolated SWCNT

An isolated SWCNT can have mainly two types of inductance which are named as magnetic inductance and kinetic inductance. The expressions for both the inductances are given by Eqn. 9.

$$L_M = \frac{\mu}{2\pi}\ln\left(\frac{y}{d}\right)$$
$$L_K = \frac{h}{2e^2 v_F} \tag{9}$$

Since $L_K >> L_M$ the value of L_M does not provide any significant impact on delay of the interconnects.

7. EQUIVALENT CIRCUIT MODEL FOR MWCNT

MWCNT is made up of number of identical SWCNT packed hexagonally [10]. Each CNT is assumed to have six surrounding neighbors who have their centers separated by a uniform distance x which are shown in Fig. 6.

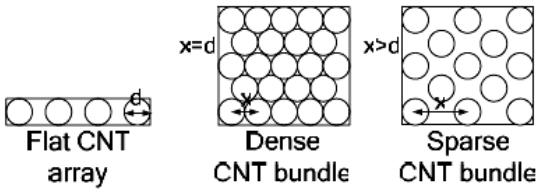

Fig.6 Flat CNT array and CNT bundle with varying density of metallic CNT

7.1 Equivalent resistance of MWCNT

The effective resistance of a CNT bundle is given by Eqn. 10 where $R_{isolated}$ is the resistance of an isolated CNT and n_{CNT} is the total number of CNTs forming the bundle.

$$R_{bundle} = \frac{R_{isolated}}{n_{CNT}} \tag{10}$$

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The number of CNTs in a bundle can be calculated using Eqn. 11 in which n_w is the number of columns and n_H is the number of rows.

$$n_w = \left\lfloor \frac{w-d}{x} \right\rfloor ; n_H = \left\lfloor \frac{h-d}{\left(\frac{\sqrt{3}}{2}\right)x} \right\rfloor + 1 \quad (11)$$

$$n_{CNT} = n_W n_H - \frac{n_H}{2}, \quad \text{if } n_H \text{ is even}$$

$$= n_W n_H - \frac{n_H - 1}{2} \quad \text{if } n_H \text{ is odd}$$

7.2 Equivalent capacitance of MWCNT

The total effective capacitance of the bundle of SWCNT is the combination of electrostatic and quantum capacitance and is given by Eqn. 12.

$$\frac{1}{C_{bundle}} = \frac{1}{C_Q^{bundle}} + \frac{1}{C_E^{bundle}} \quad (12)$$

Where total electrostatic capacitance is given by Eqn. 13 and quantum capacitance is given by Eqn. 14.

$$C_E^{bundle} = 2C_{En} + \frac{n_W - 2}{2} C_{Ef} + \frac{3(n_H - 2)}{5} C_{En} \quad (13)$$

$$C_Q^{bundle} = C_Q^{CNT} . n_{CNT} \quad (14)$$

7.3 Equivalent inductance of MWCNT

The inductance of a CNT bundle (excluding kinetic inductance) is given by Eqn. 15.

$$L_{bundle} = \frac{L^{CNT}}{n_{CNT}} \quad (15)$$

8. SIMULATION AND RESULTS

The performance comparison of copper and CNT interconnect is done using the schematic shown in Fig. 7. The schematic consists of an inverter following the equivalent circuit model of copper and CNT respectively. The equivalent circuit model consists of a resistance and inductance in series following a capacitance in parallel. The values of these parasitics have been calculated using the equations described in above section. Then the performance has also been analyzed for RC π model for both copper and CNT. Here the performance comparison of copper and CNT is done taking consideration of global interconnect only. The length of the global interconnect is taken as 1000 µm. The width of the interconnect is taken as 102.5 nm. The values of parasitics calculated are listed in Table 1. All the simulations are performed on Tanner EDA tool using 45 nm technology.

Table 1 Parameters for global interconnect.

INTERCONNECT (Global)	INTERCONNECT PARAMETERS		
	R (Ω)	L (pH)	C (fF)
COPPER	1110.45	1.849	37.04
CNT	272.0133	58.49	5.428

The waveforms observed after the simulation for the equivalent circuit model of copper and CNT are shown in Fig. 7 and Fig. 8 respectively.

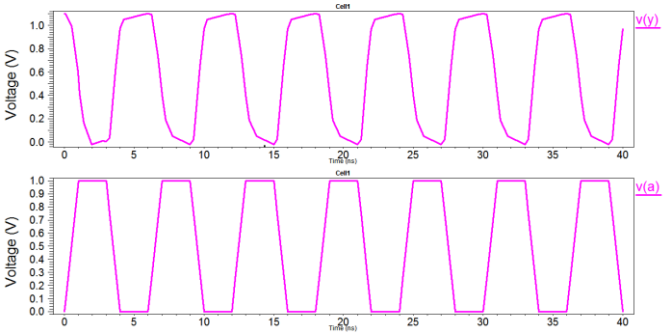

Fig. 7 Simulated waveform of equivalent circuit model for copper

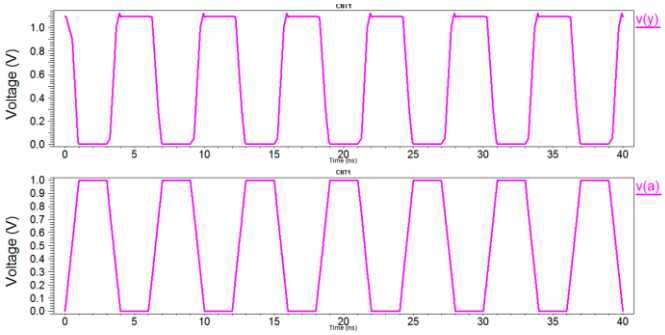

Fig. 8 Simulated waveform of equivalent circuit model for CNT

The waveforms observed after the simulation for the RC π model for both copper and CNT are shown in Fig. 9 and Fig. 10 respectively.

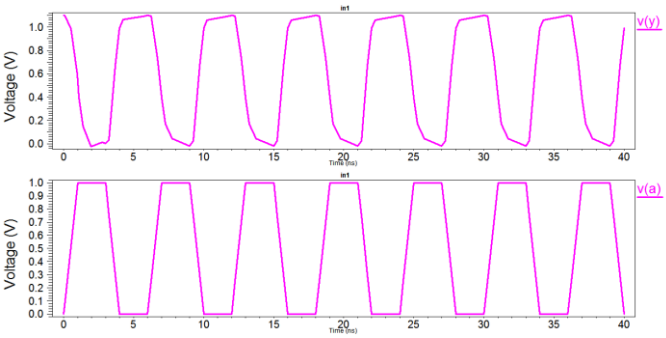

Fig. 9 Simulated waveform of RC π model for copper

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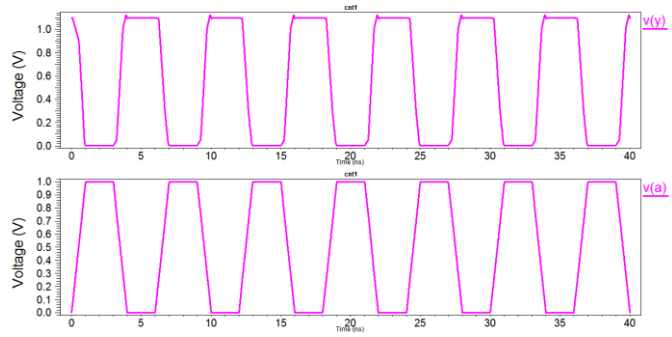

Fig. 10 Simulated waveform of RC π model for CNT

Table 2 Comparison table of delay and power parameters

INTERCONNECT	LENGTH	DELAY	POWER
COPPER	1 µm	0.8806 ns	7.5273 µW
CNT	1 µm	0.8617 ns	2.5043 µW

Table 2 shows the comparison of delay and power for both copper and CNT interconnects. Fig. 11 shows a plot of delay for CNT/CU for the length 1000 µm where as Fig. 12 shows a plot of power for CNT/CU for the length 1000 µm.

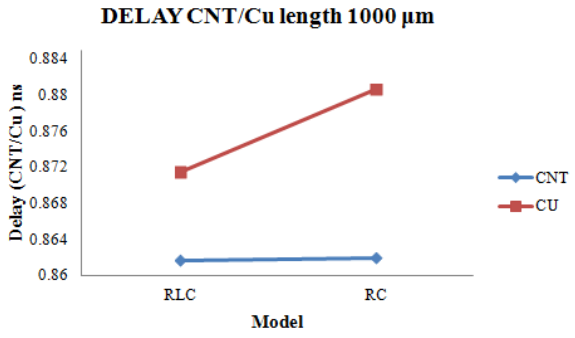

Fig. 11 Delay for both copper and CNT

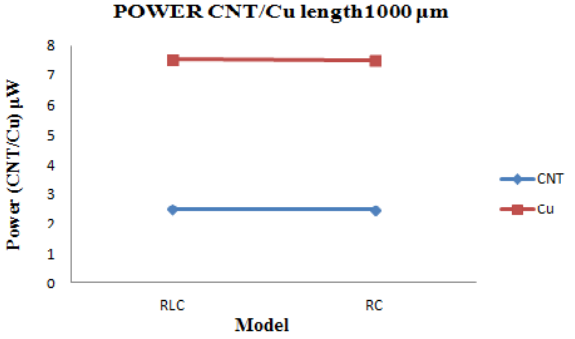

Fig. 12 Power for both copper and CNT

9. CONCLUSION

RC and RLC π models have been designed to calculate the delay and power of the interconnect. The results have been derived using deep submicron technology of 45 nm technology. The calculated delay of the RC π model circuit for copper is 0.8806 ns whereas delay for CNT interconnect is 0.8617 ns. The power of RC π model circuit for copper is 7.5273 µW where as power for CNT interconnect is only 2.5043 µW. From the results it is concluded that CNTs are the better candidate for VLSI interconnects as compare to performance of copper as an interconnect.

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Priya Srivastav received the B.Tech degree in Electronics and Communication Engineering from SMS Institute of Technology, Lucknow in 2012 She is pursuing M.Tech in VLSI Design from Ajay Kumar Garg Engineering College, Ghaziabad. Currently she is working on project named as analysis of carbon nanotubes as VLSI interconnects.

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Anup Kumar received the B.Tech degree in Electronics and Communication Engineering from VIET, Ghaziabad in 2009. He earned his M.Tech degree in VLSI Design from Thapar University in 2012. His area of interest is VLSI interconnects.

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