Comparison of images recognition using VHDL and multiclass SVM

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Abstract—

Image processing is processing of images using mathematical operations. Image processing is used in very large and expanding areas. VHDL (VHSIC Hardware Description Language) is a language used to express complex digital systems concepts for documentation, simulation, verification and synthesis. Nowadays VHDL is used as a tool for image processing. Support Vectors Machines (SVM) is one of the best known methods in pattern classification and image classification. The aim of this study is to evaluate the results of the implementation of the operator wear in the HDL for image processing. Then the potentiality of SVM evaluated on image recognition and the results compared to VHDL. The results indicated that VHDL has better performance than multi-class SVM.

Index Terms— **Image processing, VHDL, multi-class SVM, Image recognition.**

I. Introduction

Image processing is a method to convert an image into digital form and perform some operations on it, in order to get an enhanced image or to extract some useful information from it. It is a type of signal dispensation in which input is image, like video frame or photograph and output may be image or characteristics associated with that image. Usually Image Processing system includes treating images as two dimensional signals while applying already set signal processing methods to them. In many applications image processing is used for finding a group of pixels in an image that somehow belong together to finding out number of objects in image[1,2].

Image processing requires high computational power and the ability to experiment with algorithms [3-5].

Recently, reconfigurable hardware devices in the form of field programmable gate arrays (FPGAs) have been proposed as a way of obtaining high performance at an economical price [3, 4]. FPGA technology has become a viable target for the implementation of real time algorithms suited to video image processing applications [6, 7].

Those are part of Current reconfigurable computing technology, which in some ways represent an ideal alternative for image and video processing. FPGAs generally consist of a system of logic blocks, such as look up tables, gates, or flip-flops, just to mention a few, and some amount of memory, all wired together using a vast array of interconnects [6]. FPGAs are configured by using hardware design languages like Verilog HDL (Verilog) and Very High Speed Integrated Circuits (VHSIC) HDL (VHDL).VHDL is strongly typed allowing finding bugs in a design in early verification process [8].

Image classification is one of classical problems of concern in image processing. The goal of image classification is to predict the categories of the input image using its features. There are various approaches for solving this problem such as k nearest neighbor (KNN), Adaptive boost (Adaboosted), Artificial Neural Network (ANN), Support Vector Machine (SVM) [9].

SVM is one of the best known methods in pattern classification and image classification. It is designed to separate of a set of training images two different classes,(x1, y1), (x2, y2), ..., (xn, yn) where xi in Rd, d-dimensional feature space, and y in {-1,+1}, the class label, with i=1..n [1]. SVM builds the optimal separating hyper planes based on a kernel function (K). All images, of which feature vector lies on one side of the hyper plane, are belong to class -1 and the others are belong to class+1 [10].

The SVM minimizes classification errors by maximizing the margin between the two classes in a feature space induced by a kernel, and minimizing complexity by using least training points to support the decision hyper plane. To classify an image at test time, an SVM requires matching it against a small subset of the training data, namely, its support vectors (SVs) [11].

In the multiclass case, though, the union of the sets of SVs of each binary SVM may almost correspond to the full training set, potentially yielding an unacceptable computational complexity at test time [11].

The aim of this study is to evaluate the results of the implementation of the operator wear in the HDL for image processing. The software implementation of the developed algorithm using MATLAB tool is discussed in this paper, as well as the hardware architecture developed using VHDL language. Then the potentiality of SVM evaluated on image recognition and the results compared to VHDL. Test results for both implementations were presented and compared. The results indicated that VHDL has better performance than multi-class SVM.

II. Materials and Methods

Morphology is a theory and technique for the analysis and processing of geometrical structures, based on set theory and

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random functions. Morphology deals with shapes of images in Image Processing. Binary mathematical morphology is based on two basic operators: Dilation, and erosion. The basic morphological operators are erosion, dilation, opening and closing (figure 1)

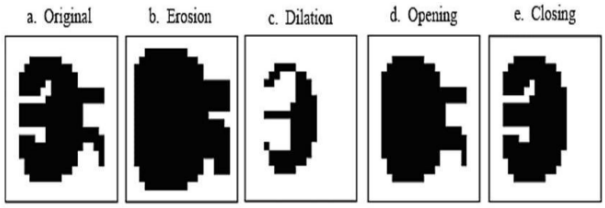

Fig 1. The basic morphological operators

VHDL (VHSIC hardware description language) is a high level description language for system and circuit design. The language supports various levels of abstraction. VHDL allows a mixture of various levels of design entry abstraction [12].

VHDL is not a case sensitive language. One can design hardware in aVHDL IDE (for FPGA implementation such as Xilinx ISE, Altera Quartos, or Synopsys Simplify) to produce to generate an appropriate test bench for a particular circuit or VHDL code, the inputs have to be defined correctly. VHDL is frequently used for two different goals: simulation of electronic designs and synthesis of such designs. Many FPGA vendors have free (or inexpensive) tools to synthesize VHDL for use with their chips, where ASIC tools are often very expensive. In this research such filters will be implemented in FPGA platform using VHDL [12]. FPGA circuit will be as Figure 2 for calculating morphology, including erosion and dilation. Because the morphology operation is a binary operation and also should make its design structure which required operators applied on the bits.

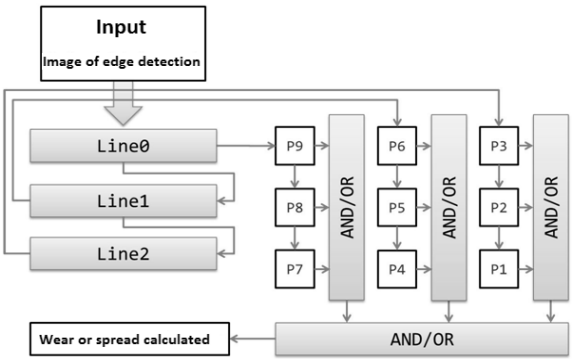

Fig2. Architecture of the calculating morphology with FPGA

The Support Vector Machine (SVM) is a supervised learning paradigm that has found important applications in image classifications. An SVM model is a representation of the examples as points in space, mapped so that the examples of the separate categories are divided by a clear gap that is as wide as possible.

Multiclass SVM aims to assign labels to instances by using support vector machines, where the labels are drawn from a finite set of several elements. The dominant approach for doing so is to reduce the single multiclass problem into multiple binary classification problems. Common methods for such reduction include: Building binary classifiers which distinguish between (i) one of the labels and the rest (one-versus-all) or (ii) between every pair of classes (one-versus-one). Classification of new instances for the one-versus-all case is done by a winner-takes-all strategy, in which the classifier with the highest output function assigns the class (it is important that the output functions be calibrated to produce comparable scores). For the one-versus-one approach, classification is done by a max-wins voting strategy, in which every classifier assigns the instance to one of the two classes, then the vote for the assigned class is increased by one vote, and finally the class with the most votes determines the instance classification. Directed acyclic graph SVM (DAGSVM) , Error-correcting output codes, Crammer and Singer proposed a multiclass SVM method which casts the multiclass classification problem into a single optimization problem, rather than decomposing it into multiple binary classification problems [13].

SVMs have been generalized to structured SVMs, where the label space is structured and of possibly infinite size. The one of aim of this paper is to evaluate the potentiality of SVM on image recognition and image classification tasks. The basic SVMs are for two-class problem. However it should be extended to multiclass to classify into more than two classes. There are two basic strategies for solving q-class problems with SVMs.

III. Results and Discussion

HDL code was written by Matlab 2014 and tool HDL Coder. Then, the results of the simulation are examined. Due to the high volume of calculations, limited hardware resources and slow algorithm in this case is not possible to apply the all information. For this reason, training with less volume of data was performed for SVM.

Top features of the final images are then processed using the PCA can be extracted. The images used in the simulation, the size of 300 × 300 pixels, which is faster to perform calculations were resized to 100 × 100. The image recognition using neural network was performed.

In this method, image width and height of some area is divided. In each region, taking into account the center pixels, horizontally and vertically neighboring pixel density is calculated. Each region will have two characteristics. Figure 3 shows the result of erosion operator.

a) The image edge detection

b) Image by applying of erosion operator

Fig3. Appling the erosion operator on the image

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Figure 4 shows structure of selected features by PCA.

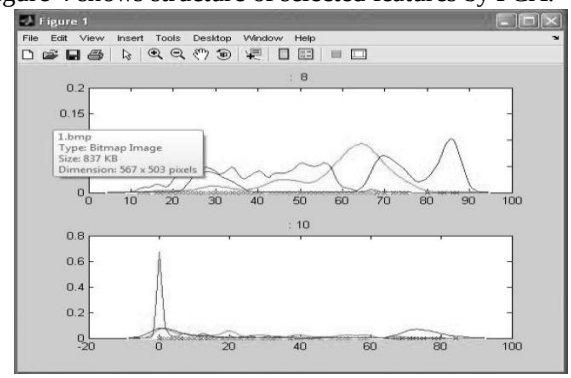

Fig4.Selection of Features using PCA structure

In order to increase the accuracy in the calculation of the detection system with a 10-fold Cross Validation technique is used. The above operation is repeated with three different upstream of data for training and testing was done.

These ratios are as follows:
30% of the training data and 70% of test data
50% of the training data and 50% of test data
80% of the training data and 20% of test data

The proposed method based on FPGA by VHDL

In the first case by considering 30% of training data and 70% of testing data, the obtained results are as follows. Table1the results of this simulation are shown.

Table 1.Resultsof FPGA for 30% of the training data and 70% of test data

Fold	Train Recog.	Test Recog.	Performance
1	96.7288	98.0553	0.0491398
2	96.6663	98.1517	0.0494787
3	97.8145	98.7517	0.0286515
4	92.9383	93.9248	0.12426
5	96.963	98.3927	0.0441967
6	95.7407	96.882	0.069814
7	97.8148	98.8697	0.0270655
8	94.6543	95.7409	0.0834038
9	96.2963	97.6588	0.0576152
10	93.4206	94.2677	0.113024
avg	95.9038	97.0695	0.0646649

The result in terms of percentage for Recognize images is up to 96% and 98% in training and test, respectively.

Tables 2 and 3 the results of simulation are shown for 50% of the training data and 50% of test data and 80% of the training data and 20% of test data, respectively.

Table 2. Results of FPGA for 50% of the training data and 50% of test data

Fold	Train Recog.	Test Recog.	Performance
1	94.8889	96.2385	0.0729628
2	97.6295	99.5402	0.0309351
3	96.6519	98.4847	0.0494892
4	96.7481	98.6055	0.0469914
5	96.8519	98.922	0.0448836
6	96.2963	97.8594	0.0572476
7	96.1185	97.6029	0.0624307
8	96.504	98.2361	0.0526204
9	95.3111	96.676	0.0625243
10	97.5185	99.4799	0.0324845
avg	96.4519	98.1645	0.051257

Table 3. Results of FPGA for20% of the training data and 80% of test data

Fold	Train Recog.	Test Recog.	Performance
1	96.5667	98.0721	0.0548093
2	96.9333	98.6767	0.0475693
3	97.5779	99.2927	0.0353977
4	96.3611	97.7981	0.0545302
5	97.7389	99.441	0.0319495
6	97.1278	98.9392	0.0442737
7	95.5889	96.9313	0.0610085
8	95.0719	96.3499	0.0796161
9	96.7056	98.46	0.0526094
10	95.6278	96.7716	0.0620987
avg	96.5300	98.0733	0.0523862

The overall recognition rate obtained SVM method is 98%.

The image recognition by SVM multi class

In the first case by considering 30% of training data and 70% of testing data, the obtained results are as follows. Table4the results of this simulation are shown.

Table 4. Results of SVM multi class for30% of the training data and 70% of test data

Fold	Recog. Rate
1	78.9836
2	78.1481
3	78.0423
4	79.2593
5	78.477
6	78.0307
7	78.5185
8	77.7778
9	78.3712
10	77.619
Avg	78.3228

The result in terms of percentage for Recognizerate is 78%.Tables 5 and 6 the results of simulation are shown for 50% of the training data and 50% of test data and 80% of the training data and 20% of test data, respectively.

Table 5. Results of SVM multi class for50% of the training data and 50% of test data

Fold	Recog. Rate
1	79.318
2	79.9259
3	80.755
4	79.7037
5	81.037
6	79.7037
7	79.911
8	80.5185
9	79.7187
10	79.9259
avg	80.0517

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Table 6. Results of SVM multi class for20% of the training data and 80% of test data

Fold	Recog. Rate
1	80.7407
2	81.146
3	80.1852
4	81.6667
5	79.9629
6	80.3704
7	81.4815
8	80.7407
9	80.3704
10	80.1852
avg	80.6850

The results show the maximum of Recognize rate for the SVM method up to 80% in case of 20% of the training data and 80% of test data. The overall recognition rate obtained SVM method is 79%.It can observe that VHDL method provide more accurate result than SVM method.

IV. Conclusion

Image processing has a very big potential to do virtually anything. In this paper, the image processing for image recognize investigated by the VHDL. The simulation results were obtained are verified using MATLAB, as well as the hardware architecture developed using VHDL language. Then the potentiality of SVM evaluated on image recognition and the results compared to VHDL. Test results for both implementations were presented and compared. The results indicated that VHDL has better performance than multi-class SVM.

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