Analysis of a Sensor Based BLDC Motor With Bridgeless SEPIC Converter For PFC And Speed Control

Anju Rajan P, Divya Subramanian

***Abstract*— This paper presents a Power Factor Correction (PFC) single phase AC-DC bridgeless Single Ended Primary Inductor Converter (SEPIC) converter which feeds a Brush Less Direct Current (BLDC) motor to improve Power Factor (PF) at the supply mains. The proposed system includes a Power Factor Correction (PFC) circuit to improve the power quality at the ac mains with lesser number of components. Conventional PFC circuits contains a Diode Bridge Rectifier (DBR) at the input side which leads to severe conduction losses and hence reduced efficiency. The absence of an input DBR and the presence of only one diode in the current flowing path during each cycle results in less conduction loss compared to existing PFC rectifiers. So bridgeless topology is used here. By implementing Discontinuous Conduction Mode (DCM) it ensures almost unity PF in a simple and effective manner, which ensures zero current turn on in power switches. Speed control can also be achieved by controlling the DC link voltage of the Voltage Source Inverter (VSI) feeding the BLDC motor. Simulations of the proposed method have been carried out using MATLAB/Simulink.**

***Index Terms*— BLDC, Bridgeless double switch SEPIC, Hall Sensors, Matlab/simulink, Power Quality.**

I. INTRODUCTION

Brushless Direct Current (BLDC) motors are recommended and preferred for many low and medium power applications due to their high efficiency, high flux density per unit volume, low maintenance, low electromagnetic interference, high ruggedness, and a wide range of speed control [1]. Due to these features BLDC motors finds application in low power motor drives such as fans, HVAC, medical equipments, transportation etc. BLDC motor is basically a kind of three phase synchronous motor that uses position detectors to sense the rotor postion and also an inverter to control the armature currents and the speed. A BLDC motor's armature is situated in the stator, the rotor is made up of magnets and its operating characteristic has similarities as of a DC motor. A conventional DC motor uses a mechanical commutator [2-3] which results in wear and tear in the brushes and requires constant maintenance, whereas the BLDC motor employs electronic commutation which results it in a virtually maintenance free environment. The BLDC motor is fed and driven by DC voltage but current commutation is done by solid-state switches. The commutation instants will be determined by the rotor position and the position of the rotor is determined either by position sensors like Hall sensor, position encoder and resolver etc or by any of the sensorless techniques. The two main types of BLDC Motors are Trapezoidal type and Sinusoidal type. The trapezoidal motor is a more attractive alternative for most applications because it is simple, low price and higher efficiency. Three-phase Voltage Source Inverter (VSI) as shown in fig.1. It performs the operation of an electronic commutator based on the rotor position signals for the generation of proper commutation sequence. Usually the three-phase VSI of the BLDC drive will be fed from a single-phase supply through a Diode Bridge Rectifier (DBR) and it is followed by a smoothening DC capacitor. Due to the uncontrolled charging of the capacitor a large current will be drawn from the mains and it results in a distorted current. As a result many Power Quality (PQ) problems arise such as poor power factor (PF), high Total Harmonic Distortion of AC main current etc. There are many international PQ standards such as IEC 61000, IEEE 519 etc [4]. All these international standards emphasizes that low harmonic contents and near unity PF current should be achieved at the AC mains by various loads. So an improved power quality converter must be introduced for almost all the BLDC drive connected systems [5]. Hence the efforts of introducing the use of power factor correction (PFC) converters for the power quality enhancement has been started. PFC consist of a buck-boost converter for PFC at front-end followed by another DC – DC converter in second stage for voltage regulation. For low power application a fly back or a forward converter has been used as a second stage and a full-bridge converter for higher power applications [6]. A Single Ended Primary Inductor Converter (SEPIC), as a single stage PFC converter, is proposed for Power Factor Correction in a BLDC motor [7]

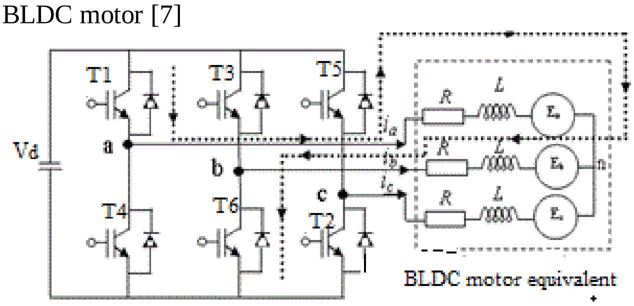

Fig 1. BLDC motor with inverter

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II. PROPOSED SYSTEM

The proposed system consists of AC-DC bridgeless converter for PFC. In the proposed system a single voltage sensor is used which senses the dc link voltage and compares it with reference voltage. This feature of BLDC motor reduces the cost and also improves the performance. The SEPIC rectifier is a high step-up AC-DC converter which is placed between the AC source and the motor. The variations in the motor speed will not disturb the AC source and maintain power quality. Block diagram and circuit diagram of the proposed bridgeless SEPIC converter fed BLDC drive is as shown in fig 2 (a) and fig 2 (b).

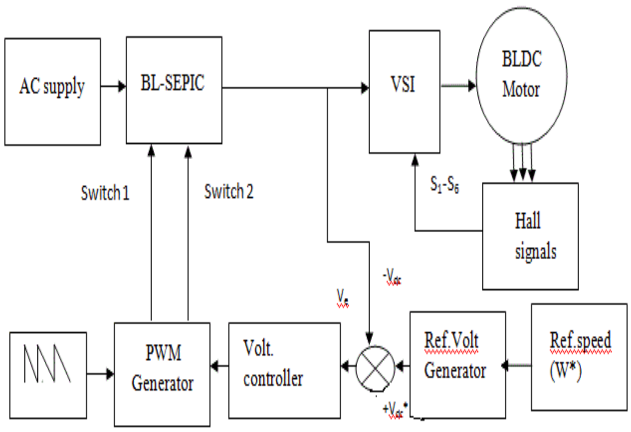

Fig 2 (a). Block diagram of the proposed system

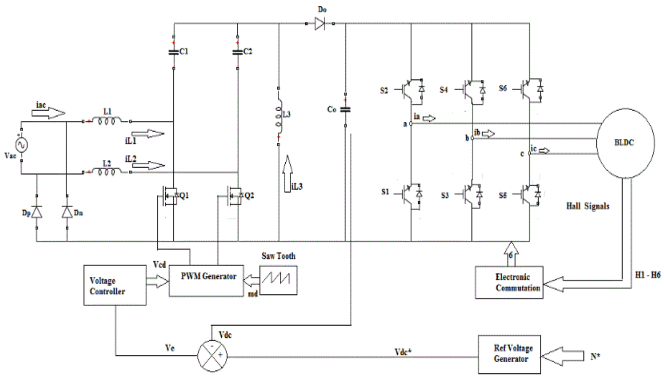

Fig 2 (b). Circuit diagram of the proposed system

The selection of mode of operation of a PFC converter is very important because it directly affects the rating and cost of the components used in the PFC converter. The modes of operation in which a PFC converter is designed to operate are the continuous conduction mode (CCM) and discontinuous conduction mode (DCM) . In CCM, the current in the inductor or the voltage across the intermediate capacitor will be continuous and in DCM the current or the voltage reaches zero and remains discontinuous for some time. In the case of CCM the DC link voltage and the supply voltage must be sensed and hence it requires two voltage sensors and increases the cost. In DCM, it requires only one voltage sensor for dc link voltage control, and inherent PFC is achieved at the ac mains, so DCM is preferred for low-power applications.

The parameters obtained in the BL-SEPIC converter are designed for the operation in discontinuous inductor current mode (DICM) to obtained nearly unity power factor corrected phases at AC mains. The DC link voltage can be controlled by and hence the speed of the motor can also be controlled by varying the duty ratio of the switches 1 and 2 of the BL-SEPIC converter.

III. BRIDGELESS SEPIC PFC CONVERTER

In the proposed system Bridgeless topology is adapted due to certain advantages like reduce conduction losses from rectifying bridges which increases the overall system efficiency. Bridgeless topology has the advantage of reduced Total Harmonic Distortion (THD) due to input diode reduction. The bridgeless converter circuit is as shown in fig 3, in which the converter operates separately over positive and negative cycles. This circuit is simple and easy to implement, therefore there are fewer limitations to choosing the main passive components. This circuit can be adapted into a single-switch bridgeless converter, which has low conduction loss and requires fewer components. Unlike the boost converter, the SEPIC converters offer several advantages in PFC applications which are given below:

- Easy implementation of transformer isolation.
- Inherent inrush current limitation during start-up and overload conditions.
- Lower input current ripple.
- Less electromagnetic interference (EMI) associated with the DCM topology.

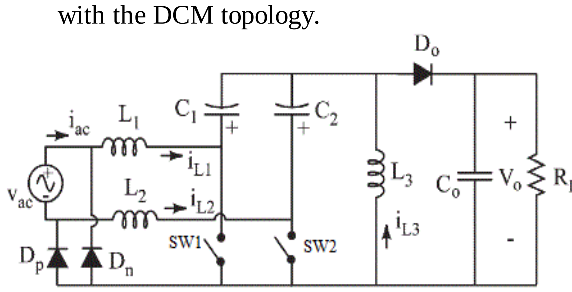

Fig 3. Proposed bridgeless SEPIC converter

The proposed topology is obtained by connecting two DC–DC SEPIC Converter one for each half-line period of the input voltage. By referring to Fig 3 there are one or two semiconductors in the current flowing path. Each of the rectifier utilizes two power switches (SW_1 and SW_2), two low-recovery diodes (D_p and D_n), and a fast diode (D_o). However, the two power switches can be driven by the same control signal, which significantly simplifies the control circuitry. Compared to a conventional SEPIC converter or other topologies, it uses an additional inductor which results in better thermal performance with the two inductors compared to a single inductor. Because each power switch is operating during half-line period. The components voltage stress is also reduced by employing the proposed system compared to other converter topologies.

The bridgeless rectifier shown in Fig 3 is constructed by connecting two DC–DC converters. Referring to Fig 3 during the positive half-line cycle, The diode D_p will be in forward biased condition first DC–DC SEPIC circuit L_1–SW_1–C_1–L_3–D_o is active through diode D_p, which

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connects the input ac source to the output ground. During the negative half-line cycle, the second DC–DC SEPIC circuit, $L_2–SW_2–C_2–L_3–D_o$, is active through diode D_n, which connects the input ac source to the output ground. The circuit has the symmetry, so is sufficient to analyse the circuit during the positive half-period of the input voltage. The rectifier is operated when the switch SW_1 is turned on then diode D_p is forward biased by the sum inductor currents i_{L1} and i_{L2}. As a result, diode D_n is reversed biased by the input voltage. The output diode is reversed biased by the reverse voltage (v_{ac} + V_o). Thus, the loss due to the turn-on switching losses and the reverse recovery of the output diode are considerably reduced., Equations for both rectifiers are identical, provided that the voltages on the capacitors for the SEPIC rectifier.

$$v_{c1}(t)=v_{c2}(t)+v_{ac}(t)=\begin{cases} v_{ac}(t) & 0\le t\le \frac{T}{2} \\ 0 & \frac{T}{2}\le t\le T \end{cases} \quad (1)$$

A. Modes of operation

During a positive cycle the circuit operation in one switching period T_s is divided into three distinct operating modes, as shown in Fig 4(a) to Fig 4(c), which is described as follows.

Mode 1 [t_0, t_1]: During this stage, the three-inductor currents i_{L1}, i_{L2} and i_{L3} linearly increase at a rate proportional to the input voltage v_{ac}. The rate of increase of the three inductor currents is given by

$$\frac{di_{Ln}}{dt}=\frac{V_{ac}}{L_n} \qquad n=1,2,3 \quad (2)$$

During this stage, the switch current is equal to the sum of the three inductors currents. Thus, the peak switch current I_{SW1-pk} is given by

$$I_{sw1-pk}=\frac{v_m}{L_e}D_1T_s \quad (3)$$

where, the equivalent value is

$$\frac{1}{L_e}=\frac{1}{L_1}+\frac{1}{L_2}+\frac{1}{L_3} \quad (4)$$

Let D_1 be the duty cycle of switch SW_1 . This interval lasts as long as when SW_1 is in ON condition. When the SW_1 is turned off it initiates the next subinterval.

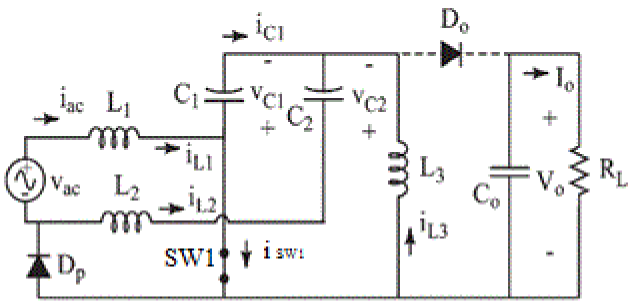

Fig 4(a) SW_1 ON

Mode 2 [t_1, t_2]: At the instant t_1, switch SW_1 is turned off, diode D_o will be turned on, which provides a path for the three inductor currents. Diode D_p remains conducting to provide a path for i_{L1} and i_{L2}. During this stage, the three inductor currents i_{L1}, i_{L2}, i_{L3} linearly decrease at a rate proportional to the output voltage V_o. And the three inductors currents are given by

$$\frac{di_{Ln}}{dt}=\frac{-V_0}{L_n} \qquad \text{where n=1,2,3} \quad (5)$$

At the end of this mode the output diode current i_{DO} smoothly reaches to zero and D_o becomes reverse biased. The normalized length of this interval is given by

$$D2=\frac{D1}{M}\sin(\omega t) \quad (6)$$

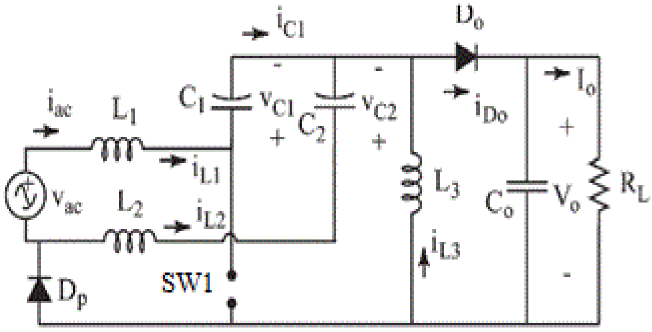

Fig 4(b). SW_1 in OFF condition

Mode 3 [t_2, t_s]: Since during the previous stage the current through the diode D_0 reached to zero, During this stage both SW_1 and D_o are in their off-state. Diode D_p provides a path for i_{L3}. The three inductors will start to discharge and behave as current sources, which keeps the currents constant. So the voltage across the three inductors will be zero at the end of this stage. Capacitor C_1 will be in a state to be charged by i_{L1}, and C_2 will be discharged by the inductor curent i_{L2}.

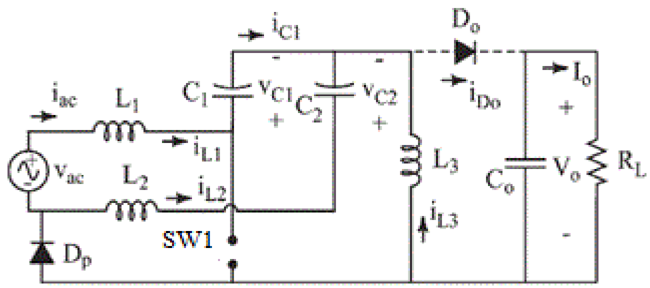

Fig 4(c): DCM topology

IV. CONTROL OF THE BL-SEPIC CONVERTER OPERATING IN THE DCM

In this approach, a reference voltage (V_{dc}^*) corresponding to the particular reference speed (N^*) is generated by

$$V_{dc}^*=k_b N^* \quad (7)$$

where k_b represents the BLDC motor's voltage constant and N^* is the reference speed. The output voltage V_{dc} of the BL-SEPIC converter is also sensed and is compared with the reference voltage to generate a voltage error (V_e). The voltage error V_e at any instant "k" is given as

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$$V_e(k) = V^*_{dc}(k) - V_{dc} \quad (8)$$

This voltage error is given to the PI controller to generate a controlled output (V_{cd}) given as

$$V_{cd}(k) = V_{cd}(k-1) + k_{pv}\left\{V_e(k) - V_e(k-1)\right\} + k_{iv}V_e(k) \quad (9)$$

where k_{pv} and k_{iv} are the proportional and integral gain of the voltage PI controller. The controller output (V_{cd}) is compared with the high frequency sawtooth waveform to generate the PWM signal to be given to PFC converter switches as

$m_d(t) < V_{cd}(t)$ then $S_{w1} = 1$, else $S_{w1} = 0$

$m_d(t) > V_{cd}(t)$ then $S_{w2} = 1$, else $S_{w2} = 0$

where S_{w1} and S_{w2} denotes the switching signals as 1 and 0 for MOSFETs 1 and 2 to switch ON and OFF, respectively.

V. OPERATION OF HALL SENSORS FOR ROTOR POSITION SENSING

The stator windings should be energized in the correct sequence for the operation and the proper functioning of a BLDC motor. For the correct switching of the inverter switches, the information regarding the rotor position is necessary. For this purpose, the rotor angular position needs to be detected using some method. To rotate the BLDC motor the stator windings should be energized in a sequence. It is important to know the Rotor position in order to understand which winding will be energized following the energizing sequence. There are two methods of rotor position detection. They are

- Sensor methods
- Sensor less methods

Using any of the above mentioned methods, the rotor position is detected and based on which the inverter switching is carried out so that the stator windings are energized in a particular sequence.

A. Sensor method

In sensor methods, an auxiliary device such as an optical encoder, resolver or hall sensors can be used to detect the rotor position. Hall Effect sensors are a common type of sensors used for the detection of rotor position sensors in BLDC motors. The rotor position is used by a speed controller for motor speed control.

B. Sensor less method

The many disadvantages of the sensor methods have given way to the development of the sensor less methods. There are many sensor less methods of rotor position detection, some of which are the Back emf Method, Rotor Position Detection from Third Harmonic of Back emf, Observer Based Method, Inductance Variation Sensing Method, Flux Linkage Variation Sensing.

In this paper sensor based rotor position sensing method is adopted. Rotor position is sensed using Hall-effect sensors embedded into the stator. Most BLDC motors have three Hall sensors inside the stator that is the non-driving end of the motor. It works on the principle that whenever the rotor magnetic poles pass near the Hall sensors they give a high or low signal indicating the N or S pole is passing near the sensors. Based on the combination of these three Hall sensor signals, the exact sequence of commutation can be determined.

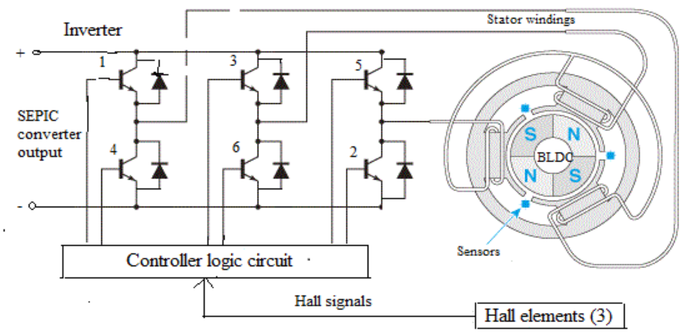

Fig 5. BLDC with sensor

The three phase BLDC motor is operated in a two phase-ON fashion, that is the two phases will be energized and produces high torque while third phase is off. The two phases energized will depend on the position of the rotor. The signals from the position sensors produce a three digit number that changes every 60^0. In a three phase star connected BLDC motor each interval starts with the rotor and stator field's line 120^0apart and ends when they are 60^0 apart. Maximum torque is reached when the field lines are perpendicular. Current commutation is done by six-step inverter as shown in a simplified form in fig 5. The switches are shown as bipolar junction transistors but MOSFET switches are most common. Table1 shows the switching sequence, the current direction and the position sensor signals.

TABLE1: Switching Sequence.

Switching intervals	Seq no	Post. Sensors			S/w closed		Phase current		
		H 1	H 2	H 3			A	B	C
0-60	0	1	0	0	1	4	+	-	off
60-120	1	1	1	0	1	6	+	off	-
120-180	2	0	1	0	3	6	off	+	-
180-240	3	0	1	1	3	2	-	+	off
240-300	4	0	0	1	5	2	-	off	+
300-360	5	1	0	1	5	4	off	-	+

VI. SIMULATION RESULTS

The performance of the BL-SEPIC converter fed BLDC drive is simulated in MATLAB/simulink environment. The performance of operation is evaluated on the basis of various performance parameters. DC link voltage (V_{dc}) is used for the performance evaluation of the PFC SEPIC converter. Supply voltage (v_s), supply current (i_s) are used for estimating the power quality of the system. The speed (N), electromagnetic Torque (T_e), stator current (i_a) and back emf of the motor are used to determining the satisfactory operation of the BLDC motor. PQ indices such as Power Factor and Total Harmonic Distortion (THD) of the supply

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current are analyzed for determining PQ at ac mains. The simulink model of the proposed system and the simulated waveforms of different parameters are as shown in the figures given below.

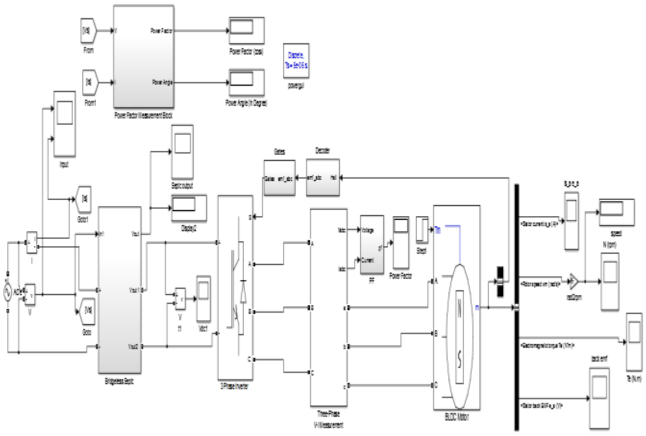

Fig 6. Simulink model of the proposed system.

Fig.6 shows the full Matlab/simulink model of the proposed system. It consists of mainly three blocks of BL-SEPIC converter, 3 phase Inverter and BLDC motor. The BL-SEPIC shown as a subsystem in the fig 6 can be understood in the fig 7.

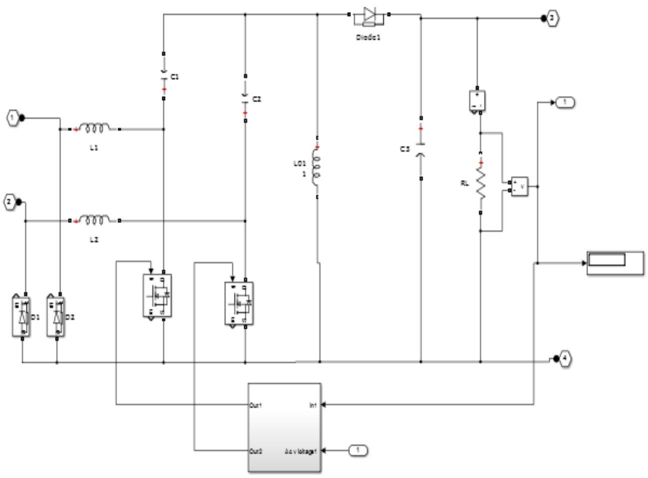

Fig 7. Simulink model of the BL-SEPIC converter.

The control portion which is shown as a subsytem in the fig 7 is shown as in fig 8.

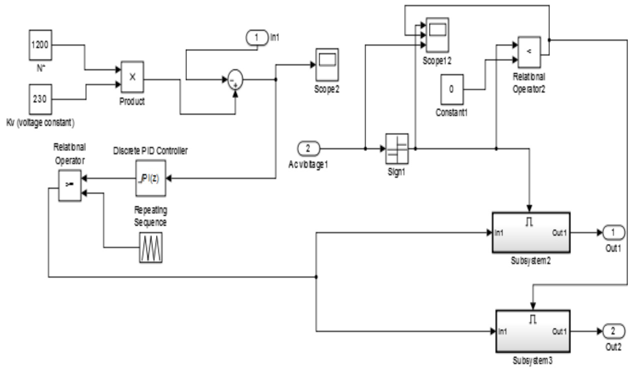

Fig 8.Simulink model of the Control circuit.

The reference speed is treated as a corresponding voltage signal and is compared with the DC link voltage, whose error signal is given to a PI controller. It minimizes the error to a respective value and compares with the sawtooth waveform for pulse generation. In fig 8 the signals showing 1 and 2 are the generated pulses to the switches of the BL-SEPIC converter. These pulses are generated by a closed loop action of the BL-SEPIC converter along with a reference speed.

Voltage and current waveforms at the ac mains are as shown in fig.9, shows the current follows the voltage almost in phase and also the Power Factor is measured as 0.959 which is almost near to unity.

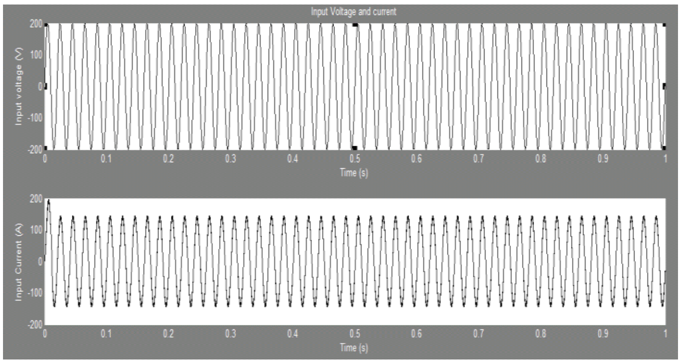

Fig 9. Input side voltage and current waveform

Output voltage waveform of the BL-SEPIC converter or the DC link voltage waveform is as shown in the fig.10

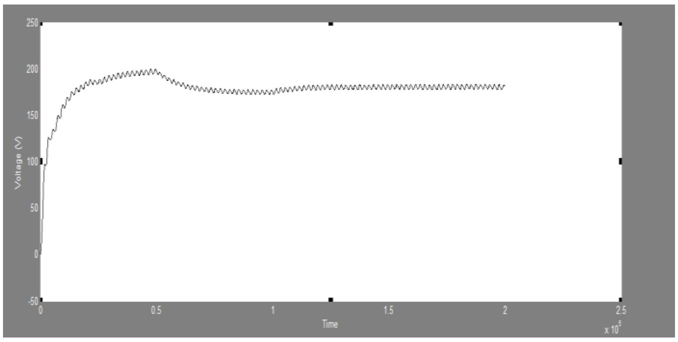

Fig 10. Output voltage waveform of BL-SEPIC converter

For a reference speed of 1200 rpm the motor speed, Electromagnetic Torque, Stator currents and back emfs are shown in figures from fig 11 to fig 14 which shows the performance of the BLDC motor.

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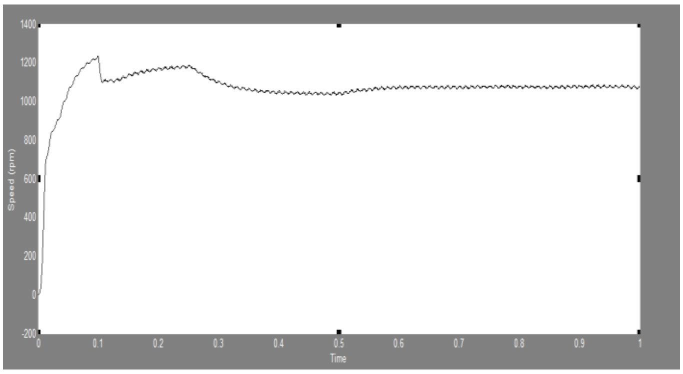

Fig 11. Speed of the BLDC motor

The load torque value of the BLDC motor used is 3 Nm. The developed torque has an average value of around 3Nm which is shown in fig 12

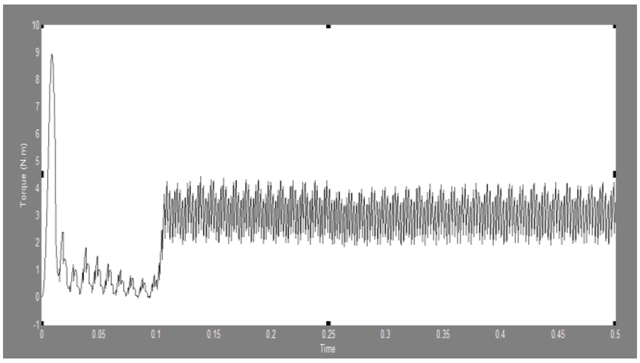

Fig 12. Torque waveform

The stator current waveforms are obtained which has a phase shift of 120^0 is as shown in fig.13

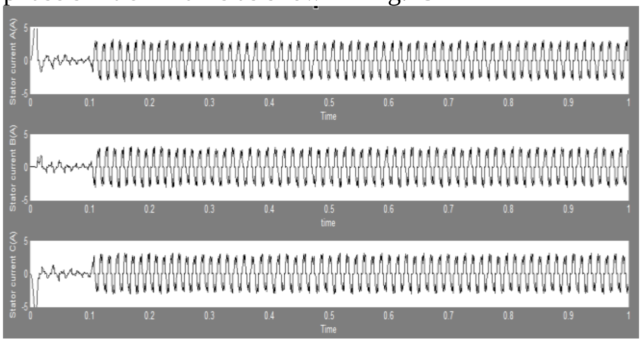

Fig 13. Stator currents

Fig 14 shows the generated trapezoidal back emf of the BLDC motor in three phases which are also 120^0 phase shifted.

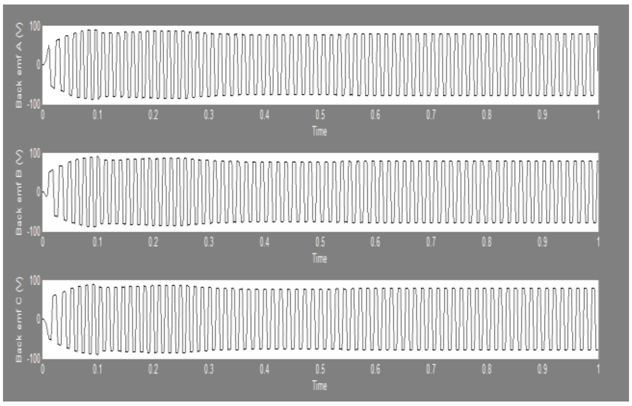

Fig 14. Trapezoidal Back emf

As seen from fig 15, the THD mains current of the BL-SEPIC converter fed BLDC motor is observed under 5%, which is the requirement of power quality.

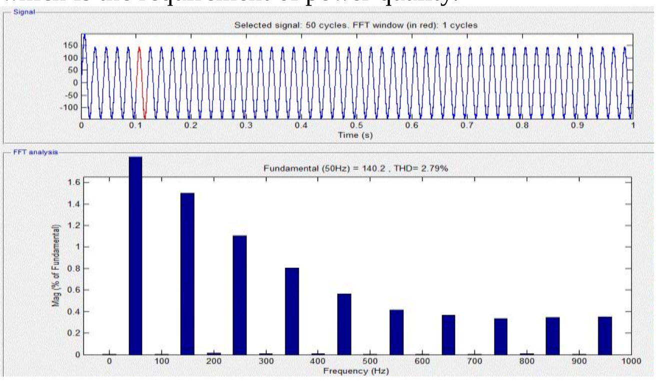

Fig 15. THD at the supply mains

VII. HARDWARE DESCRIPTION

The experimental set up of the entire hardware is as shown in fig 16. It consists of a BL-SEPIC converter, Inverter, BLDC motor drive, controllers and the driver circuits.

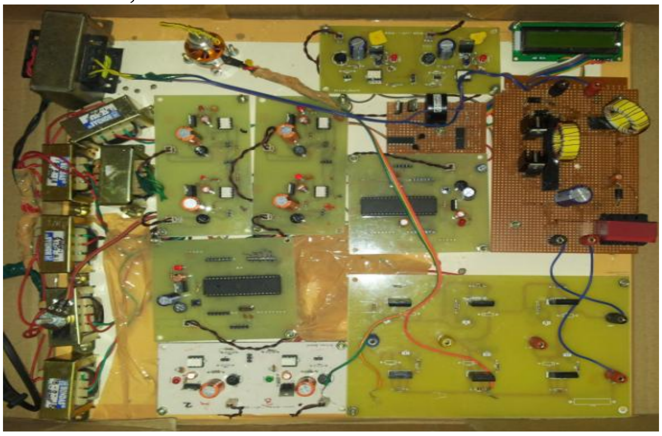
Fig 16 Hardware set up.

The switches in the converter are operated at 20Khz. The controller employed is ATmega 16 microcontroller. Here two controllers are used, which generates the gate pulses for the switches in BL-SEPIC converter and for the inverter switches. Due to practical difficulties and cost considerations construction of the hardware section of power factor correction and closed loop speed control of BLDC Motor, a BL-SEPIC converter is designed for 15V. The microcontroller is supplied with a +5V which is generated and regulated from the power supply unit.

VIII. CONCLUSION

A single phase ac-dc bridgeless SEPIC converter for VSI fed BLDC motor has been simulated using MATLAB/Simulink and implemented. It has been observed that the bridgeless topology ensures less input current distortion. The capability of the system is analyzed and verified via simulation results. The simulation studies indicate that the power factor is nearly unity and obtained low THD by using BL-SEPIC converter, which satisfies the international standards. The

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PFC converter operates in DCM which uses a single voltage sensor for dc link voltage control, and inherent PFC is achieved at the ac mains. By implementing a voltage follower approach, a simple control is implemented to control the voltage and hence controls the speed of the BLDC motor. A satisfactory performance has been achieved for speed control and supply voltage variation with power quality indices. The proposed scheme is a recommended solution applicable to low-power BLDC motor drives.

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