

ARM Processor Architecture

Evolution and Applications

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Abstract— As of 2014, ARM is the most widely used 32-bit instruction set architecture in terms of quantity produced. Many of the electronics gadgets around the world became a part of our daily life and we have become completely dependent on them for performing most of our work. Due to its variety of the features, many of these gadgets are fitted with embedded processors that not only occupy less space but also ensure that users get smooth experience whilst using the device [8].

Keywords— ARM architecture, RISC processor, CPSR register, modes of operation, ARM versions, CISC architecture etc

I. INTRODUCTION

Advanced RISC machine (ARM) is the first reduced instruction set computer RISC processor for commercial use, which is currently being developed by ARM holdings. In 1983, in England, Acorn Computer Ltd officially launched an Acorn RISC Management Project after being inspired to design its own processor by Berkeley RISC, one of the high impact projects under ARPA's (Advanced Research Projects Agency, now converted to DARPA) VLSI projects, dealing with RISC based microprocessor design led by David Patterson who coined the term RISC[2].

The ARM processor is based on the RISC architecture, where RISC stand for Reduced Instruction Set Computer. ARM processor finds applications in digital TVs, set-top boxes, smart phones, mobile, laptops etc. Nowadays, there are several embedded architectures in use such as ARM architecture developed by ARM Ltd, Atmel's ARV architecture, TI's MSP430 architecture and many more. However the extensively used and most popular embedded architecture among many companies is the ARM Ltd's ARM architecture.

As the name suggests it does not mean that the processors with less than 100 instructions are qualified to RISC category, but instead they should have the highly optimized instruction set. ARM in the beginning was known as Acorn RISC Machine with VLSI Technology Inc. as its silicon partner, ARM came up with ARM1, the first ARM silicon on April 20, 1985. Now ARM became the acronym for Advanced RISC Machine.

RISC features can be implemented in CISC processor but would require much more hardware. A typical RISC architecture consists of a large uniform register file, load and store architecture, simple addressing mode and uniform fixed length instruction field. Due

to these characteristics we achieve high performance, low code size, low power consumption and low silicon area.

Organization of the paper is like this. *Chapter 1* gives the brief introduction of the paper. It also focuses on the evolution of the ARM processor. Features of ARM processor are described in Chapter II. Also explains instruction set of ARM processors. *Chapter 3* extracts architecture of ARM processor. It gives operating modes of ARM processor. General purpose registers are also explained in this chapter. Some of the special registers such as SPSR, CPSR also given in this chapter. *Chapter 4* mentions the various series of ARM cortex processor and their corresponding applications.

Finally, conclusion is drawn on the entire paper and mentioned under this head followed by the acknowledgment and references.

ARM architecture evolution

The ARM architecture has evoked through many stages, the smart phones employ ARMv5 architecture and the later releases. Hardware Floating Point Unit is the major change brought in ARMv7 to provide more speed than the software based floating point. Even DSP instructions were added to the set to improve the ARM architecture for use in Digital Signal Processing and multimedia applications. In ARMv7 Thumb 2 instructions also added to obtain the code density. The new ARMv8 has undergone a considerable change by using 64-bit architecture. Therefore this ARM architecture with brilliant features is widely accepted by many organizations[4].

II. FEATURES OF ARM ARCHITECTURE

British Multinational Semiconductor and software design company, ARM Holding Inc, offers complete solutions that are essential for the manufacturing process, but company does not manufacture ICs moreover it provides software development tools under the brand Keil and Real view. It also provide ARM architecture licensing for the companies that want to manufacture ARM based CPU or 'System On Chip' Product.

The ARM architecture is a simple hardware design allowing things to left off the chip. It provides small die-shaped chip which helps in reducing cost. Its low cost simple pipeline construction adds the benefits to embedded application.

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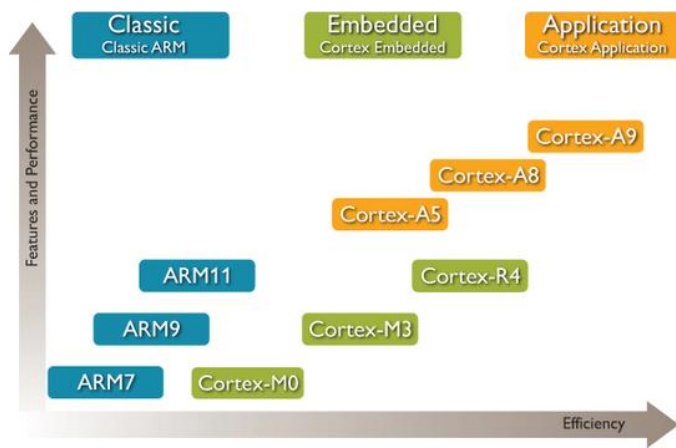


Fig. 1. ARM architecture evolution

ARM Instruction set

ARM allows an instruction set called ‘Thumb’, which comprises 32-bit instructions to 16-bits, enabling programs to be coded much more density than standard RISC instruction set. Processors enabled to execute ‘Thumb’ also allow 32-bit instructions to run on the same hence allowing 16-bit and 32-bit instructions to mix together without affecting the performance maintaining powerful computing capabilities.

The instruction set of in ARM processor are classified as ARM instruction set, Thumb instruction set and Jazelle mode. ARM mode is a standard 32-bit instruction set. a Thumb instruction set is a 16-bit compressed form that provides better performance than Complex Instruction Set Computer. Jazelle DBX allows some ARM processor to execute java byte codes[5].

Features of ARM Processor

ARM is a 32-bit instruction set architecture. Today many embedded applications like smart phones, set-top boxes, digital television, digital camera use ARM processors due to their cost effectiveness and low power consumption. ARM architecture is compatible with all four major OS i.e. Symbian OS, Palm OS, Windows and Android OS.

III. ARM ARCHITECTURE

An ARM processor consists of 31 general purpose 32-bit register. Sixteen registers namely R0-R15 are visible, which means they can be modified by the user whereas other registers help to speed up the execution process. Some registers play some special roles like R14 acts as a link register (LR), R15 acts as a Program Counter (PC) and R13 acts as a Stack Pointer[1].

A. ARM processor modes of operation

There are seven modes of operations as shown in Fig. 1. These modes are categorized as user mode, prevailed mode and exception mode. User mode is a normal program execution mode in which the system resources are unavailable. If some exception occurs, then the mode is

changed to the exception mode. In exception mode, all system resources are available[7].

Mode	Description	
Supervisor (SVC)	Entered on reset and when a Software Interrupt instruction (SWI) is executed	Privileged modes
FIQ	Entered when a high priority (fast) interrupt is raised	
IRQ	Entered when a low priority (normal) interrupt is raised	
Abort	Used to handle memory access violations	
Undef	Used to handle undefined instructions	
System	Privileged mode using the same registers as User mode	Unprivileged mode
User	Mode under which most Applications / OS tasks run	

Fig. 1. ARM processor modes of operations [7]

System & User	FIQ	Supervisor	Abort	IRQ	Undefined
R0	R0	R0	R0	R0	R0
R1	R1	R1	R1	R1	R1
R2	R2	R2	R2	R2	R2
R3	R3	R3	R3	R3	R3
R4	R4	R4	R4	R4	R4
R5	R5	R5	R5	R5	R5
R6	R6	R6	R6	R6	R6
R7	R7	R7	R7	R7	R7
R8	R8_fiq	R8	R8	R8	R8
R9	R9_fiq	R9	R9	R9	R9
R10	R10_fiq	R10	R10	R10	R10
R11	R11_fiq	R11	R11	R11	R11
R12	R12_fiq	R12	R12	R12	R12
R13	R13_fiq	R13_svc	R13_abt	R13_irq	R13_und
R14	R14_fiq	R14_svc	R14_abt	R14_irq	R14_und
R15 (PC)	R15 (PC)	R15 (PC)	R15 (PC)	R15 (PC)	R15 (PC)

Fig. 2. ARM processor important registers [7]

B. Important registers in ARM

There are two important registers in ARM, namely Current Program Status Register (CPSR) and Saved Program Status Register (SPSR). CPSR is similar to PSWR register in 8051 micro-controller, which indicate some important flag bits like carry bits and zero flag bits as shown in Fig. 2. Whereas SPSR is used in execution modes. Whenever exception occurs the content of CPSR are copied in SPSR[6]. The organization of

register in an ARM processor is shown in Fig. 3.

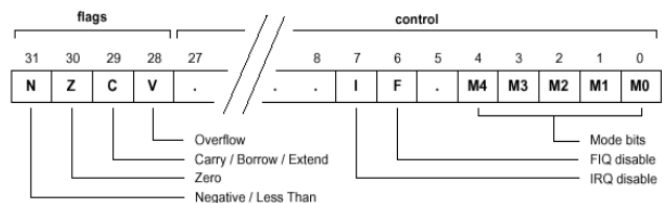


Fig. 3 ARM processor CPSR registers

IV. APPLICATION DOMAINS OF ARM PROCESSOR

There are following series of ARM Cortex processor Cortex A, Cortex R, Cortex M. The types and their applications are mentioned as below.

A. ARM Cortex A-Application Processors

The ARM Cortex-A is a group of 32-bit and 64-bit RISC ARM processor cores licensed by ARM Holdings. The cores

are intended for application use, and consists of the 32-bit ARM Cortex-A5, ARM Cortex-A7, ARM Cortex-A8, ARM Cortex-A9, ARM Cortex-A12, ARM Cortex-A15, and ARM Cortex-A17 MPCore,[1] and the 64-bit ARM Cortex-A53, ARM Cortex-A57, and ARM Cortex-A72 [8].

Applications include:

1. Smartphones
2. Netbooks
3. eReaders
4. Digital TV
5. Home Gateways
6. Servers and Networking

B. ARM Cortex R-Real-time Embedded Processors

Cortex Real-time Embedded processors have been developed for deeply embedded real-time applications where the need for low power and good interrupt behaviour are balanced with exceptional performance and strong compatibility with existing platforms.

Applications include:

1. Automotive braking systems
2. Powertrain solutions
3. Mass storage controller
4. Networking & Printing

C. ARM Cortex M-Embedded Processors

Cortex-M series processors have been developed primarily for the microcontroller domain where the need for fast, highly deterministic, interrupt management is coupled with the desire for extremely low gate count and lowest possible power consumption.

Applications include:

1. Microcontrollers
2. Mixed signal devices
3. Smart sensors
4. Automotive body electronics and airbags

CONCLUSION

ARM processor core is the engine within the system that fetches ARM (and possibly Thumb) instructions from the memory and execute them. ARM cores are very small typically occupying just a few square millimeters of the chip area. Modern VLSI technology allows a large number of additional system components to be incorporated on the same chip. The ARM7TDMI is the current low end ARM core and is widely used across a range of applications, most notably in many digital mobile telephones. ARM processors up to ARM7 employ a simple 3-stage pipeline with stages like fetch, decode and execute.

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