

DTMF Signal Generation and Detection Using Effective DFT (Goertzel algorithm) Technique on FPGA

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Abstract— Dual-tone multi-frequency (DTMF) is a signaling standard in telecom applications that produces two tones simultaneously for each key press. The DTMF tones are chosen such that decoding the pressed key from the received tones is easier. The DTMF tone detection is very crucial block in several telecom based embedded systems. As the current generation embedded systems are looking for key feature of low power, the DTMF detection algorithm also must be implemented with low power schemes[1].

The DTMF detection can be done with FFT based technique which is power consuming type and it requires more hardware. In this project the FPGA based DTMF detection with very low power and low area using Goertzel algorithm will be implemented in VHDL.

In the first phase of the project we shall implement FFT based DTMF detection using Xilinx FFT core. The area, timing and power results will be analyzed. In the second phase the Goertzel algorithm will be implemented and similar analysis will be carried out which demonstrates that the Goertzel algorithm consumes less power and can still efficiently detect the DTMF tones. To test the project at various stage DTMF tone generator module also will be implemented with digital carrier generators[2].

Index Terms— DTMF, FFT, Goertzel algorithm, VHDL, FPGA.

I. INTRODUCTION

Dual tone multi frequency (DTMF) is a method of representing digits with tones for transmission over an analog communication channel. DTMF tones are used by all touch tone phones to represent the digits on a touch tone keypad. DTMF technology provides a robust alternative to rotary telephone systems and allows user-input during a phone call. This feature has enabled interactive, automated response systems such as the ones used for telephone banking, routing customer support calls, voice mail, and similar applications[3].

A DTMF tone consists of two superimposed sinusoidal signals selected from two frequency groups. The frequency groups represent rows and columns on a touch tone keypad as shown in the below figure 1. Each DTMF tone must contain one sinusoid from the high-frequency group (1209, 1336, 1477 and 1633 Hz) and one sinusoid from the low frequency

group (697, 770, 852 and 941 Hz). This allows a touch tone keypad to have up to 16 unique keys[4].

	Col 1 1209Hz	Col 2 1366Hz	Col 3 1477Hz	Col 4 1633Hz
Row 1 697 Hz	1	2	3	A
Row 2 770 Hz	4	5	6	B
Row 3 852 Hz	7	8	9	C
Row 4 941 Hz	*	0	#	D

Fig. 1 Touch Tone Keypad

The frequencies selected for DTMF tones have some distinguishing characteristics and unique properties.

- 1) All tones are in the audible frequency range allowing humans to detect when a key has been pressed.
- 2) No frequency is a multiple of another.
- 3) The sum or difference of any two frequencies does not equal another selected frequency.

The second and third properties simplify DTMF decoding and reduce the number of falsely detected DTMF tones. The unique properties allow DTMF receivers to detect when a user has pressed multiple keys simultaneously and reject any tones that have harmonic energy. Harmonic energy can only be generated by speech/noise and not by the sum of two valid DTMF frequencies[5].

II. IMPLEMENTATION

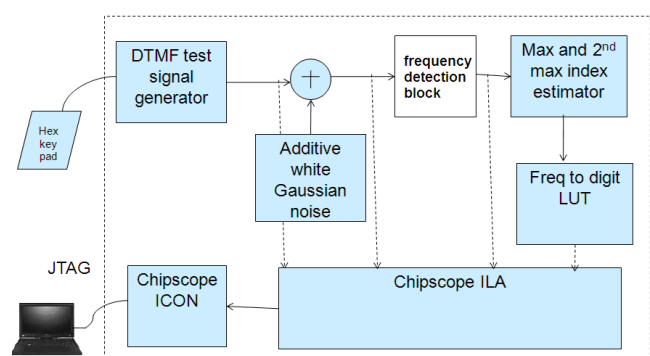


Fig. 2 General module of DTMF detection

The above figure 2 shows the block diagram of DTMF (Dual tone multiple frequency) detection and it consists of following modules.

- 1) Hex key pad
- 2) DTMF test signal generator
- 3) Additive white Gaussian noise
- 4) Frequency detection block
- 5) Magnitude/index estimator
- 6) Frequency to digit look-up table

Hex Keypad is an external component which gives input to the module. The signal from column is taken as input, where as row and display are the output signals. DTMF test signal generates the carrier frequencies according to the key pressed. These frequency waves are generated by a DDS core. The tone generator takes these two cosine waves generated from DDS cores and add them in order to produce one wave called tone out. The tone out, which is the output from tones generator is Mixed with Gaussian noise, which comes from many natural sources, such as the thermal vibrations of atoms in conductors (referred to as thermal noise or Johnson-Nyquist noise), shot noise, black body radiation from the earth and other warm objects, and from celestial sources such as the Sun.

Now, the generated Gaussian noise signal is given as input to the frequency detection block. The Output of the frequency detection block is indices and magnitudes. As per the scope of the project, there are two variants of frequency detector block.

They are:

- 1) FFT-128 core
- 2) Goertzel algorithm

A. FFT- 128 core

The Fast Fourier Transform (FFT) implements the Cooley-Tukey FFT algorithm, a computationally efficient method for calculating the Discrete Fourier Transform (DFT). A FFT is an efficient algorithm to compute the discrete Fourier transform (DFT) and it's inverse. There are many distinct FFT algorithms involving a wide range of mathematics from complex number arithmetic to group theory and number theory. The below figure 3 shows the block diagram of frequency detection module with FFT 128 core

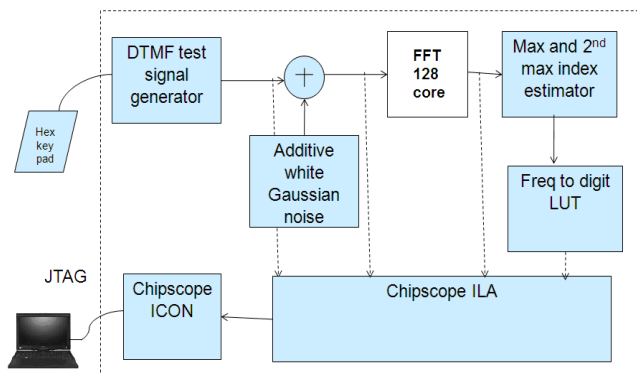


Fig. 3 Block diagram with FFT 128 core as frequency detection module

The FFT core computes an N-point forward DFT or inverse DFT (IDFT) where N can be 2m, here m is 3 to16. For fixed-point inputs, the input data is a vector of N complex values. For single-precision floating-point inputs, the input data is a vector of N complex values represented as dual 32-bit floating-point numbers with the phase factors represented as 24 or 25-bit fixed-point numbers.

All memory is on-chip using either block RAM or distributed RAM. The N element output vector is represented by using bits for each of the real and imaginary components of the output data. Input data is presented in natural order and the output data can be in either natural or bit/digit reversed order. The complex nature of data input and output is intrinsic to the FFT algorithm, not the implementation.

Three arithmetic options are available for computing the FFT:

- Full-precision unscaled arithmetic.
- Scaled fixed-point (user provides scaling schedule).
- Block floating-point (run-time adjusted scaling).

The point size N, choice of forward or inverse transform, scaling schedule and the cyclic prefix length are run-time configurable. Transform type (forward or inverse), scaling schedule and cyclic prefix length can be changed on a frame-by-frame basis. Changing the point size resets the core. Four architecture options are available: Pipelined, Streaming I/O, Radix-4, Burst I/O, Radix-2, Burst I/O, and Radix-2 Lite, Burst I/O[6].

B. Goertzel algorithm

The Goertzel algorithm is a digital signal processing (DSP) technique for identifying frequency components of a signal, published by Dr. Gerald Goertzel in 1958. While the general Fast Fourier transform (FFT) algorithm computes evenly across the bandwidth of the incoming signal. The Goertzel algorithm looks at specific, predetermined frequencies. Some applications require only a few DFT frequencies. The block diagram of Goertzel algorithm is shown in below figure 4.

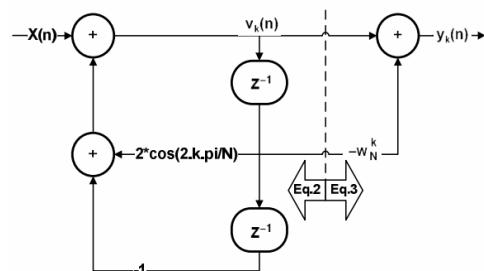


Fig. 4 Goertzel algorithm

One example is frequency-shift keying (FSK) demodulation, in which typically two frequencies are used to transmit binary data; another example is DTMF, or touch-tone telephone dialing, in which a detection circuit must constantly monitor the line for two simultaneous frequencies indicating that a telephone button is depressed.

Goertzel's algorithm reduces the number of real-valued multiplications by almost a factor of two, relative to direct

computation via the DFT equation. Figure 5 shows the block diagram of frequency detector using Goertzel algorithm. For a length of N, the Goertzel's series is

$$H_k(z) = \frac{1 - W_N^k z^{-1}}{1 - 2 \cos\left(\frac{2\pi k}{N}\right) z^{-1} + z^{-2}}$$

Where,

$$k = 0, 1, \dots, N - 1 \tag{1}$$

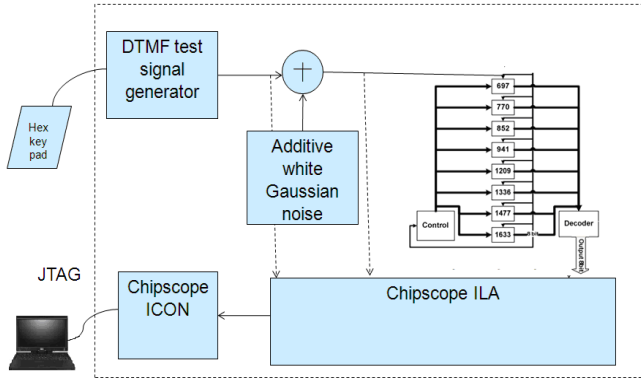


Fig. 5 Goertzel algorithm block as frequency detector

III. SIMULATION RESULTS

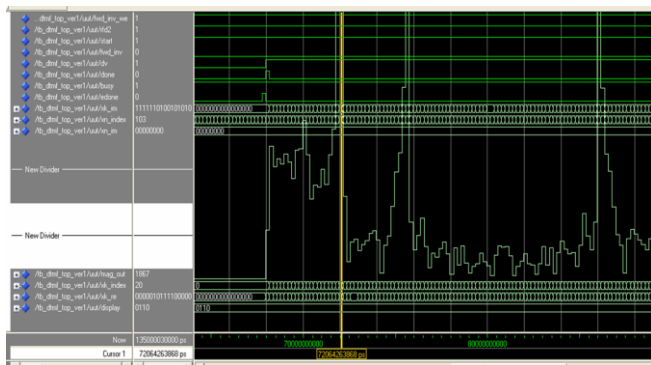


Fig. 6 simulation results FFT as frequency detector block

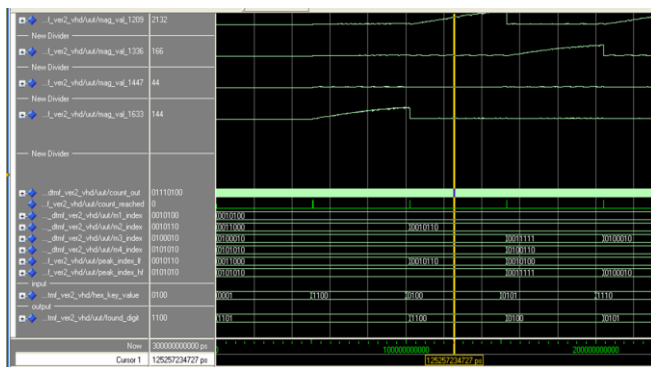


Fig. 7 simulation results of Goertzel algorithm block as frequency detector

IV. CONCLUSION

In this paper, we implemented DTMF signal generation and detection on FPGA in two phases. In the first phase we implemented FFT based DTMF detection using Xilinx FFT core and in the second phase we implemented very low power and low area technique using Goertzel algorithm as frequency detector block which can still efficiently detect the DTMF tones.

The Modelsim Xilinx Edition (MXE) is used for simulation and functional verification. Xilinx ISE is used for synthesis and bit file generation. The Xilinx Chipscope is used to test the results on Spartan 3E 500K FPGA board.

REFERENCES

- [1] Gay, S.L.; Hartung, J.; Smith, G.L.; , "Algorithms for multi-channel DTMF detection for the WE DSP32 family ," Acoustics, Speech, and Signal Processing, 1989. ICASSP-89., 1989 International Conference on , vol., no., pp.1134-1137 vol.2, 23-26 May 1989.
- [2] Tadokoro, Y.; Haneda, Y.; , "A Dual-Tone Multifrequency Receiver Using Synchronous Additions and Subtractions," Communications, IEEE Transactions on , vol.35, no.4, pp. 414- 418, Apr 1987.
- [3] Schwingshackl, D.; Mayerdorfer, T.; Strausnigg, D.; , "Universal Tone Detection Based on the Goertzel Algorithm," Circuits and Systems, 2006. MWSCAS '06. 49th IEEE International Midwest Symposium on , vol.1, no., pp.410-413, 6-9 Aug. 2006.
- [4] Kaiyi Zhang; Xiaoqing Yu; Wangen Wan; , "A digital tone decoder based on a modified Goertzel algorithm," Audio, Language and Image Processing, 2008. ICALIP 2008. International Conference on , vol., no., pp.779-783, 7-9 July 2008.
- [5] S. Park and D. M. Funderburk, "DTMF detection having sample rate decimation and adaptive tone detection." United States Patent, Feb. 1995. Patent Number: 5,392,348.
- [6] G. Goertzel, "An Algorithm for the evaluation of finite trigonometric Series", Amer. Math. Monthly, Vol.65, Jan. 1958, pp.34-35

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