Dual Stack Conditional Push-Pull Pulsed Latches

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***Abstract* — In this paper, a novel class of pulsed latches of high speed under minimum energy consumption is designed and implemented in 65-nm CMOS technology. This conditional push-pull pulsed latch adopts a push-pull output stage, which is driven by two split paths with a conditional pulse generator. It is implemented in two versions, respectively, without (CP^3L) and with (CSP^3L) shareable conditional pulse generator. The implemented pulsed latch outperforms the well known transmission gate pulsed latch (TGPL). The CP^3L and CSP^3L designs are faster than transmission gate pulsed latch (TGPL) by 2.01X (1.19X) for the minimum ED design. The incremented energy dissipation is further reduced by employing dual stack approach.**

***Keywords*— Flip-flops(FFs), leakage power, low power techniques, nanometer CMOS, process technologies, pulsed latches, VLSI.**

I. INTRODUCTION

FLIP-FLOPS (FFs) and latches are ubiquitous elements in CMOS circuits based designs which makes the major portion of the synchronous circuits and, in particular, of both high speed and low energy microprocessors [8]. FFs data-to-output delay (D-Q) and power dissipation affect the processor's clock period and overall power. FFs are part of the clock network, which is responsible for 30%-50% of the whole chip energy budget, and dissipates 80% of clock power [9-11]. Since VLSI systems are power limited, it is important to reduce the power dissipation in these timing elements as it reduces the overall system power consumption.

Energy efficiency of FFs and latches is even more critical now as speed can be improved only through improvements in energy efficiency of these elements. Thus, Energy-Efficient designs with minimum energy (delay) for a given speed (energy) constraint is crucial. Latches are mainly used to reduce sequencing overhead on a high-performance processor. In addition to enabling high performance designs, pulsed latch can also enable low-power designs due to its smaller size and lighter clock load. A low-voltage swing latch can be used to reduce power dissipation further.

In this paper, a new pulsed latch driven by a conditional pulse generator is designed and implemented in 65-nm CMOS. The main idea is to adopt a push pull output stage of the pulsed latch is driven by two split paths for rise and fall output transitions. Thereby it reduces both the path effort and the parasitic delay. By adopting half latches in the split paths the capacitance at the output of the first stage is further reduced. Two versions are presented, the Conditional Push-Pull Pulsed Latch (CP3L), and a version with a Shareable (CSP3L) Pulse Generator (PG). The adoption of a fast push-pull second stage, which requires a conditional PG, enables 50-to-100% delay improvements compared to the traditional latches [3].

This paper is organized as follows. In Section II, all the existing FF topologies are presented and a best reference is chosen for comparison with the implemented topology. The main idea and operation of the conditional push-pull pulsed latch is described in Section III, and their detailed circuit implementation in both versions is discussed in Section IV. In Section V, low power techniques and a effective way of implementing power gating is explained. Dual stack method is described in Section VI. Measurements results and comparison with state-of-the-art topologies are discussed in Section VII. Conclusions are reported in Section VIII.

II. STATE-OF-THE-ART TOPOLOGIES

To achieve a desired energy-delay tradeoff, various classes of FFs have been proposed depending on the features of the application like high speed, low energy, low standby energy, etc. Selecting the most suitable FF topology for a given application is not a simple task. An appropriate analysis and comparison strategies are applied to compare large number of FF classes (4) and topologies (19) in a 65-nm CMOS technology. Among the state-of-the-art topologies, four existing FF topologies viz., Transmission gate pulsed latch (TGPL), Transmission gate FF (TGFF), Adaptive coupling FF (ACFF), Skew-tolerant FF (STFF) are studied and a best reference is chosen for comparison [4].

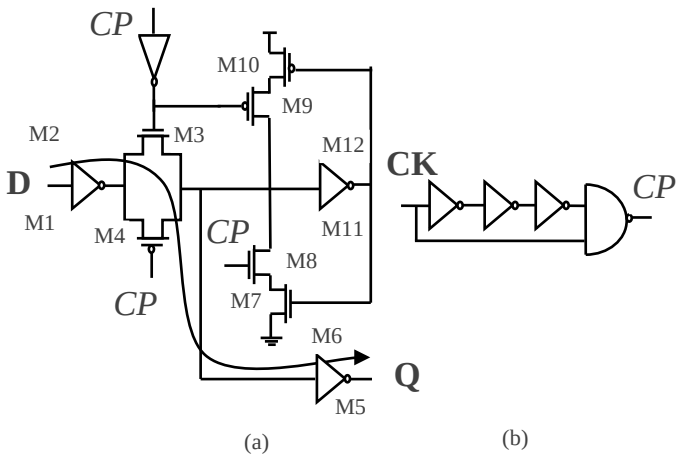

Fig. 1. (a) TGPL topology. (b) Pulse generator topology.

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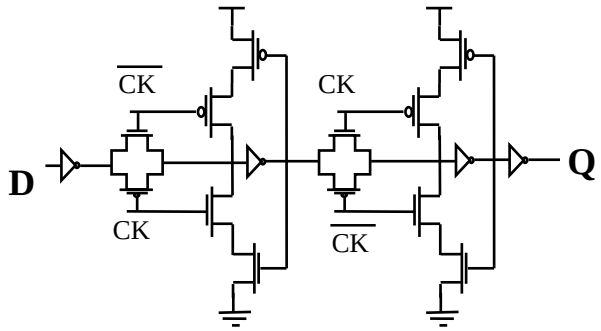

Fig. 2. Transmission Gate Flip-Flop(TGFF)

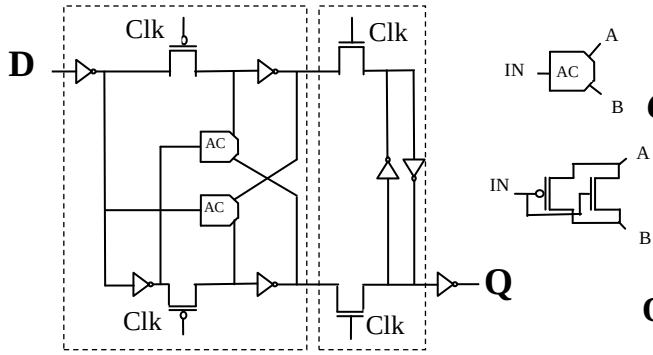

Fig. 3. Schematic diagram of ACFF

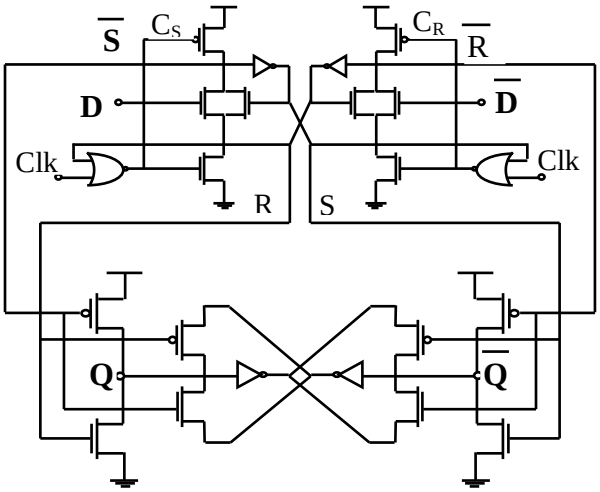

Fig. 4. Skew Tolerant Flip-flop(STFF)

Among the existing classes of FFs, pulsed latches exhibit the best energy efficiency from moderate to high performance design targets. The transmission gate pulsed latch (TGPL) (see fig 1) [7] is the most energy-efficient FF in a large portion of the design space, ranging from high speed to minimum energy-delay (ED) product designs, while simple Master-Slave FFs, TGFF[7] (see fig 2)and ACFF(see fig 3)are the most energy-efficient in the low-power E-D space region[5]. TGPL also has the lowest data-in to output (D-Q) delay along with skew-tolerant FF (STFF) (see in fig 4). However, the latter has considerably worse energy efficiency [6]. Hence, the TGPL will be adopted as a reference for high-speed energy-efficient designs.

III. CONDITIONAL PUSH-PULL PULSED LATCH

Basic operation

The general scheme of the conditional push-pull pulsed latch is shown in the Fig. 5[1]. In order to reduce the delay and make it energy efficient, a push-pull output stage is adopted in its output stage. The push-pull output stage is driven by two split paths that alternatively generate two pulsed signals, active-high reset (R) and active-low set (S). The set and reset pulses are generated after the falling clock edge through the conditional pulse generator in Fig. 5.

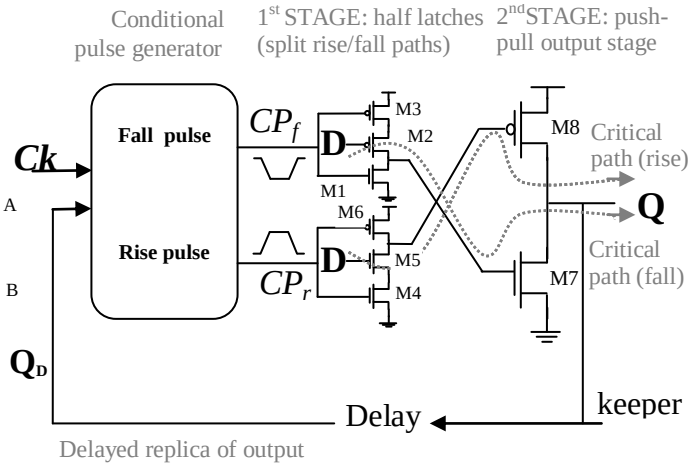

Fig. 5. General scheme of the implemented class of pulsed latch

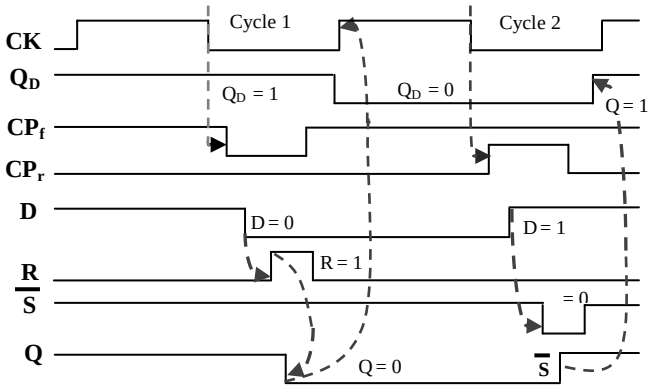

Fig. 6. Waveforms of internal signals of the general scheme in Fig. 7

Fig. 6 depicts the main waveforms of the internal signals. At the falling clock edge (cycle 1 in Fig. 6), the pulse generator checks the previous output Q_D, whether low or high.

(i) If Q_D = 1, through CPf, a fall pulse is generated. The rise path is remained unchanged. If D=1, half latch M4-M6 is disabled and R retains its previous value. And if D = 0, the M1–M3 half latch is enabled, and a high pulse (R) is generated in fall path. Thus making M7 in output stage ON and the output Q is pull down.

(ii) If Q_D= 0, through CPr, a rise pulse is generated. Fall path is unchanged. If D = 0, the latch M4–M6 is disabled and keeping S high. If D = 1, the latch M4–M6 is enabled and the CPr pulse pulls down S by turning M8 ON and output, Q is high.

IV. IMPLEMENTATION OF CONDITIONAL PUSH-PULL PULSED LATCH CONCEPT: CP^{3}L AND CSP^{3}L TOPOLOGIES

The novel pulsed latch in Fig. 5, in which critical path is lightly loaded to meet optimum speed and power product can be implemented in two versions, respectively, without (Section IV-A) and with (Section IV-B) shareable pulse generator.

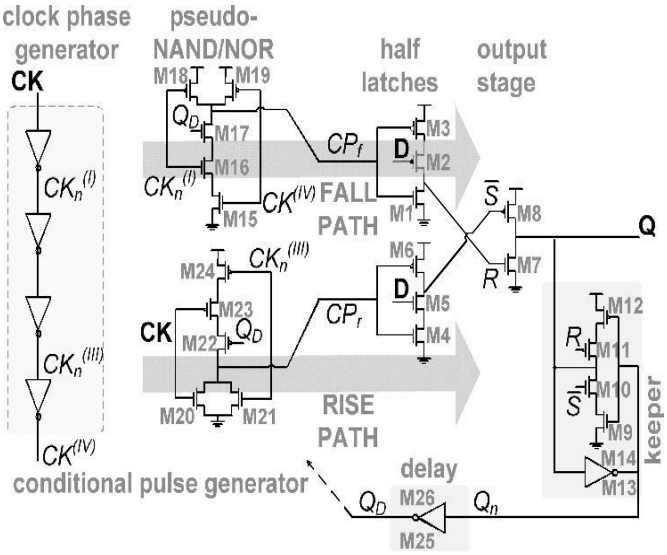

Fig. 7. CP^{3}L topology (area in dashed line is shareable among multiple cells).

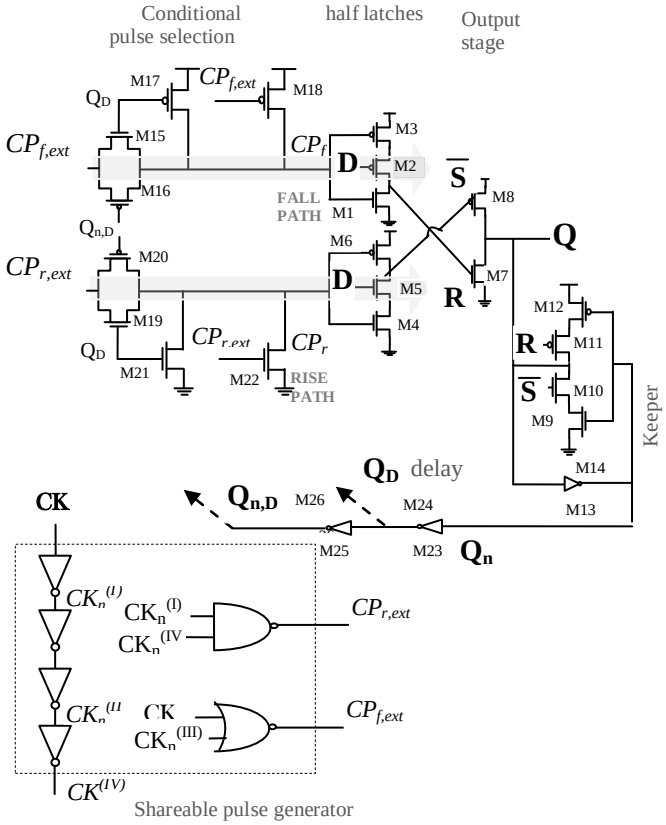

Fig. 8. CSP^{3}L topology (area in dashed line is shareable among multiple cells).

IV(A). CP^{3}L : Conditional Push-Pull Pulsed Latch

The Conditional push-pull pulsed latch (CP^{3}L) is depicted in Fig. 7. The output Q is driven by a keeper circuit (M9–M12 in Fig. 7). When R = 1 the pull-down transistor of the output stage, M7 is ON and the pull up network of the keeper through M11, is OFF. Similarly, if S=0 the pull-up transistor of the output stage, M8 is ON and the pull-down network of the keeper through M10, is OFF.

The pulse generator in CP^{3}L comprises a clock phase generator, a pseudo-NAND for the fall path (M15-M19) and a pseudo-NOR gate for the rise path (M20–M24). The pseudo- NOR/NAND is gated by delayed version of Q, Q_D, generated by delay stage (consisting of two inverters M13–M14 and M25–M26) in feedback path. If Q_D =1(0) and D=0(1), CP^{3}L will change its state, and doesn't not change its state if D=1(0). By delaying the previous output, power dissipation is reduced due to the elimination of undesired transitions on CP_f and CP_r.

IV(B). CSP^{3}L : Conditional Shareable Push-Pull Pulsed Latch

The Conditional shareable push-pull pulsed latch (CSP^{3}L) is depicted in Fig. 8.In CP^{3}L, the pulse generator cannot be shared among different latches since pseudo-NOR/NAND are driven by Q_D , which is unique for each latch. In CSP^{3}L, by integrating the conditional logic in the latch, the pulse generator can be shared among several flip-flops within the chip.

In CSP3L, static NAND/NOR gates are used in the shareable pulse generator to generate the pulses CPf, ext and CPr,ext which can be distributed to different latches requiring the same role as CP f and CPr in CP3L. For this purpose two transmission gates and few keeper circuits have to be added at the pulsed nodes. Two more inverters are added in the delay stage in feedback path than in CP3L, as the transmission gates in static NOR/NAND needs complementary control signals.

V. LOW POWER TECHNIQUES

Power gating technique is one of the most advanced lower power technique. Power gating is the complete shut off of supply nets to different areas of a design when they are not needed (also known as MTCMOS or power shutdown). Since the power has been completely removed from these shutdown areas, the power for these areas is reduced essentially to zero. The most effective way of implementing power gating technique is Dual stack approach method [2].

Dual Stack Method

In dual stack approach, in Fig. 9, two pMOS transistors are used in the pull-down network and two nMOS transistors are used in the pull up network. In sleep mode, the sleep transistors are off., by making Sel=0 and hence Sel'=1. The other four transistors in the method, namely, P2, P3 and N2, N3 connect the main circuit with the power rails, supply and ground. The advantage is that The nMOS transistors in pull-up network degrades the high logic level while pMOS transistors in the pull-down network degrades the low logic level. Since power dissipation is proportional

to the voltage applied, with the reduced voltage the power decreases and also the previous state can be retained. During active mode, when Sel=1 and Sel'=0, both the sleep transistors (N1 and P1) and the parallel transistors (N2, N3 and P2, P3) are on, and connects the circuit to the power supply rails.

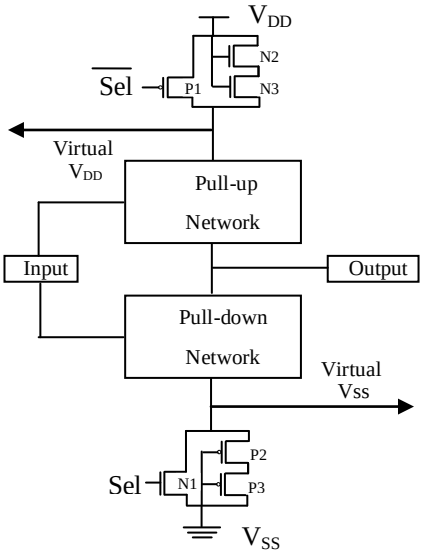

Fig. 9.Dual Stack approach

VI.CONDITIONAL PUSH-PULL PULSED LATCHES WITH DUAL STACK

The high speed energy efficient ɪditiona' 'atches with dual stack gating approach are ɑepicted ɪn Fig. 10, Conditional push-pull pulsed latch (CP^3L) and Conditional shareable push-pull pulsed latch (CSP^3L) in Fig. 11. Digital Schematic drawing tool is used for schematic diagrams. An extra inverter at the output in CP^3L is used to reduce the current contention at the output stage.

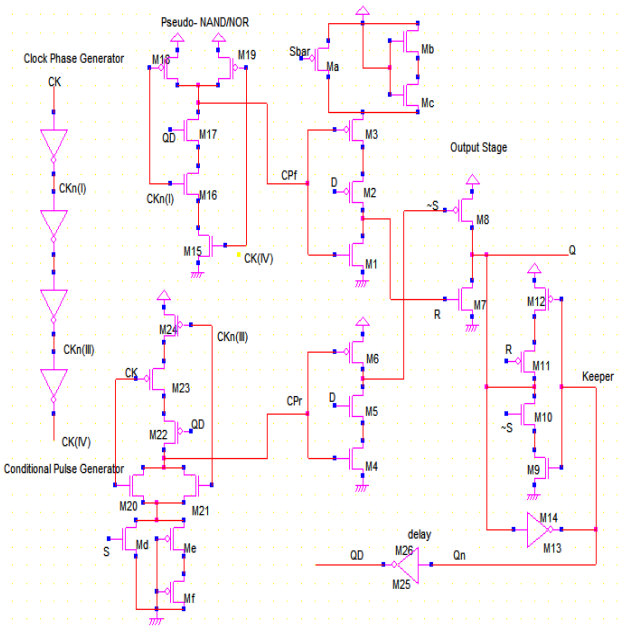

Fig. 10. CP^3L schematic with dual stack and output inverter

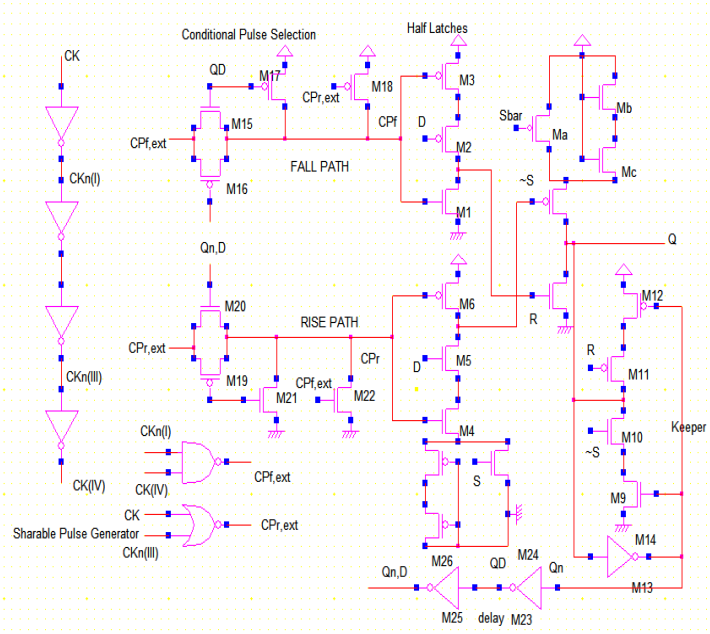

Fig. 11. CSP^3L with dual stack schematic

VII. SIMULATION RESULTS

All the above circuits are simulated using HSPICE tool, developed by Synopsis. TSPICE is a low end simulator used for schematics and layouts.

A.Comparision of State-of-art-topologies

The below are the tabulated results of the existing state-of-art-topologies, Transmission gate pulsed latch (TGPL), Trans-mission gate FF (TGFF), Adaptive coupling FF (ACFF), Skew - tolerant FF(STFF).

Flip-flop Topologies	Average Power (Watts)	Clk- Q Delay (seconds)	Energy (Joules)
STFF	83.32µ	108.56p	9.04f
TGPL	29.86 µ	115.19p	3.43f
TGFF	28.54 µ	123.82p	3.53f
ACFF	11.13 µ	164.71p	1.83f

* $\mu = 10^{-6}$, $p = 10^{-9}$, $f = 10^{-15}$

B. CP^3L and CSP^3L along with their dual stack implementation

The two versions of conditional pulsed latches are simulated and their results are compared with the reference flip-flop.

Flip-flop Topologies	Average Power (µ Watts)	Clk- Q Delay (p seconds)	Energy (f Joules)
TGPL	29.86	115.19	3.43
CP^3L	37.04	57.14	2.11
CSP^3L	45.22	96.44	4.36

* $\mu = 10^{-6}$, $p = 10^{-9}$, $f = 10^{-15}$

From the above table, it can be inferred that, despite certain increment in power dissipation, *CP^3L and CSP^3L* circuits

exhibits superior energy efficiency compared with TGPL, in terms of delay. 50% to 60% delay improvements are achieved compared to the reference flip-flop, TGPL. This energy dissipation is further reduced by employing dual stack method.

Flip-flop Topologies	Average Power (μ Watts)
CP^3L	37.04
CP^3L with Dual Stack	21.94
CSP^3L	45.22
CSP^3L with Dual Stack	32.71

The incremented power in *CP^3L and CSP^3L* is greatly reduced by the adaptation of dual stack low power technique.

VIII. CONCLUSION

In this paper, a dual stack gating technique is employed in an energy efficient pulsed latch. This adaptation has reduced the leakage power, thus reducing the overall power consumption making it power efficient circuits. The implemented latches, CP^3L (CSP^3L) achieves a 2.01X(1.19X) speed improvement compared to TGPL, which makes them faster and energy efficient flip-flops. Since CP^3L (CSP^3L) are almost equal in terms of energy and performance, both are equally worth considering while considering highly energy efficient systems.

IX. REFERENCES

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