Designing of DS CDMA-CI Transmitter through CORDIC and QPSK Modulator

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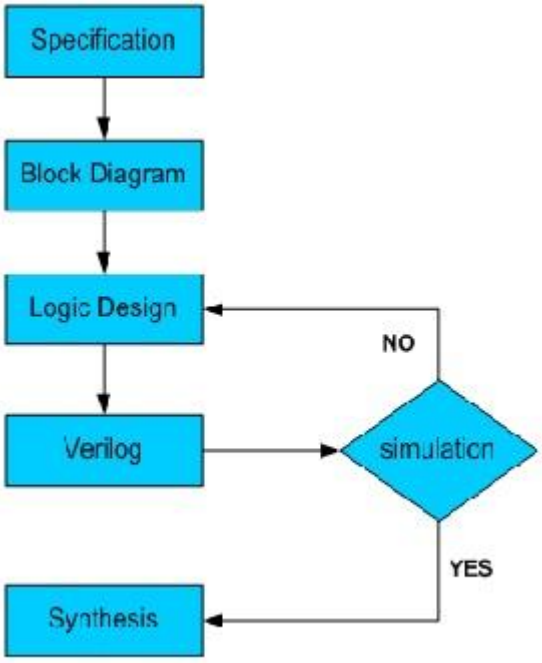
***Abstract*— DS CDMA-CI transmitter is Direct Sequence Code Division Multiple Access- Carrier Interferometry Transmitter. The present existing transmitter model of DS-CDMA is not capable enough when spreading codes are made complex since complex multiplications needed for spreading would consume more power, require more area for implementation and contribute more delays. In this paper, a designing of DS-CDMA/CI transmitter is proposed which uses CORDIC algorithm and QPSK Modulator (for 2 bits calculation) to generate carrier wave whose phase offset value is controlled by Carrier Interferometry (CI) codes. The architecture is based on the principle that product of two exponential is essentially an exponential with angle equal to sum of angle of product components. Furthermore, the architecture is reconfigurable in the sense that the spreading codes can be dynamically assigned during transmission and therefore can be used for designing communication systems for cognitive radio applications. The proposed design is simulated in modelsim 6.3f.**

***Index Terms*— QPSK modulator, Convolutional Encoder, CORDIC, PN Sequence, DS CDMA-CI, Angle Generator**

I. INTRODUCTION

Direct Sequence Code Division Multiple Access (DSCDMA) is a technique based on the orthogonal codes this gives the user more space (bandwidth) at the same time and same frequency domain. Here we mean with the same frequency is the single wireless channel available for serving the users at same time through same channel by sending the individual information to each of these users separately, this concept is stand for multiple access. Although this CDMA is very important aspect of 3rd generation mobile system and is the base of WCDMA (Wide band code division multiple access) technique. The CDMA is multiple access technology, In DS-CDMA the information needs to send to the users or need to get from the users is denoted in different symbols and these symbols are the different sequence of codes. Once the base station sends the different symbols to the users hence it is essential for the base station to recover back the information which it got from the users in acknowledgement. The technique of this sending the symbols are spreading and the recovering the symbols is de-spreading. If the codes selected are such that de-spreading of a user's spread signal by another user's code gives zero output, the codes are said to be orthogonal. If the output is non-zero for two types of codes, the metric for comparison of performance is the cross-correlation property. Orthogonal codes have zero cross correlation. In simple terms, lower the cross correlation better is the performance of codes and resistance against multiple access interference.

II. PROPOSED METHODOLOGY



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Above flow graph shows the method or procedure of the project, and each block present in the flow graph is briefly explained below:

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1. **Specification: Xilinx ISE 13.4, version 0.87 xd** tool is used for simulation and also used the simulation software **ModelSim6.3c.**
2. **Block Diagram**: Design of DS CDMA-CI transmitter is proposed through CORDIC algorithm with QPSK Modulator.
3. **Logic Design:** Logic design will be done to Design of convolutional encoder, CI Code selector, cordic block, QPSK Modulation, LFSR and phase generator.
4. **Verilog:** To work on this project Verilog language will use for the implementation of Design for DS CDMA-CI transmitter with cordic block in Xilinx ISE 13.4.
5. **Simulation:** The all the different module of this design will be simulated separately for check of their individual working and hence the simulation done for them separately and if it is found okay then combination of all the module needs to be done.
6. **Synthesis:** After combining, testing has to be done, i.e whether the program is working properly or not, if yes it will continue else it has to rewrite or correct. After correction again test the program, if it's successfully working then it will be simulated.

III. Objective and Scope of Project

1. The main objective of the project is to develop and design for DS CDMA CI transmitter using Cordic operations and QPSK modulator.

2. To investigate the shortfalls of the different methods and the present technology and to find out the advancements of new system. Also to analyze the scope for performance enhancements with respect to present system.

3. New architecture will be simulated in Xilinx ISE design suite13.4 and tested to reduce the delay/power consumption and area on chip for the given system.

IV. Designing

For processing the data we need to have the sequence of randomly generated bits so the LFSR is used. LFSR is a shift register whose input bit is a linear function of its previous state. The output of the LFSR goes to the convolutional encoder. The code rate, k/n, is expressed as a ratio of the number of bits into the convolutional encoder (k) to the number of channel symbols output by the convolutional encoder (n) in a given encoder cycle. Phase Generator, Offset Generator and CI code selector all together work to generate the angle of the signal which sums up in adder and is adjusted by the angle adjuster. The signal from here goes to the CORDIC block and processed under the CORDIC algorithm, CORDIC is Coordinate Rotation Digital Computer (CORDIC) technique, which uses an iterative computation method to generate carrier frequency**,** the only operations it requires are addition, subtraction, bit shift and table lookup. The output from the Convolutional encoder and from the CORDIC block fed in to the QPSK (Quadrature Phase shift Keying) modulator under which the rotation of phase took place in different co-ordinates on local oscillator.

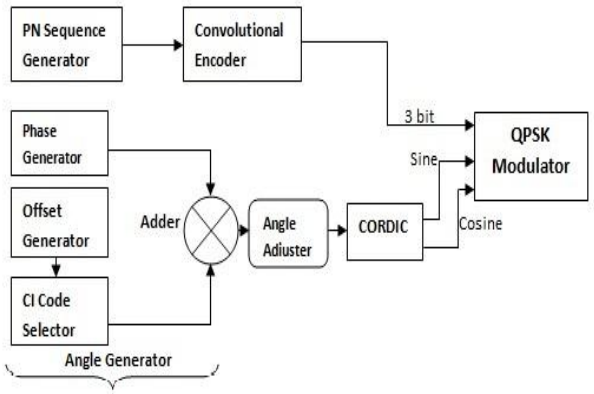

Figure 1: Block Diagram for design of DS CDMA-CI transmitter through CORDIC and QPSK modulator.

A. PN Sequence Generator: PN sequence generator or Linear-feedback shift register (LFSR) is a shift register whose input bit is a linear function of its previous state. The most commonly used linear function of single bits is exclusive-or (XOR). Thus, an LFSR is most often a shift register whose input bit is driven by the XOR of some bits of the overall shift register value. An LFSR is a class of devices known as state machine. It is a shift register whose input bit is a linear function of its previous state. The only linear functions of single bits are XOR and XNOR. Thus it is a shift register whose input bit is driven by XOR or XNOR of some bits of overall shift register value. Feedback around an LFSR's shift register comes from a selection of points (taps) in the register chain and constitutes XORing these taps to provide tap(s) back into the register. Register bits that do not need an input tap, operate as a standard shift register. It is this feedback that causes the register to loop through repetitive sequences of pseudo-random value. The choice of taps determines how many values there are in a given sequence before the sequence repeats. The implemented LFSR uses a one-to-many structure, rather

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than a many-to-one structure, since this structure always has the shortest clock-to-clock delay path.

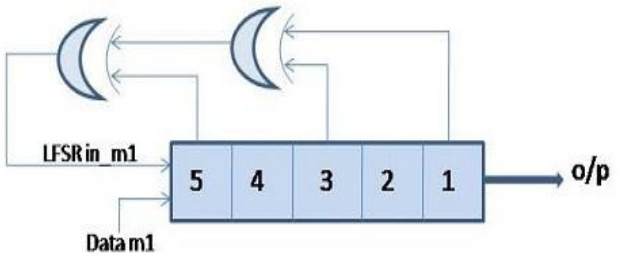

Figure 2: Circuit Dia. of LFSR with maximum length Feedback Polynomial $X^5 + X^3 + 1$

Tap m1 and tap m3 are joined together for performing the Ex-or operation having the partial feedbacks from the respective tapes. The output of the first Ex-or is going in to the second Ex-or (as the diagram is for two tapes operation of LFSR) there it is joined with the tape m5 data and the Ex-or gate produces the partial feedback which is again looping towards the stated process.

B. Convolutional Encoder: We have used 3 bit length of convolutional encoder. Convolutional codes are commonly described using two parameters: the code rate and the constraint length. The code rate, k/n, is expressed as a ratio of the number of bits into the convolutional encoder (k) to the number of channel symbols output by the convolutional encoder (n) in a given encoder cycle. The constraint length parameter, K, denotes the "length" of the convolutional encoder, i.e. how many k-bit stages are available to feed the combinatorial logic that produces the output symbols. Closely related to K is the parameter m, which indicates how many encoder cycles an input bit is retained and used for encoding after it first appears at the input to the convolutional encoder. The m parameter can be thought of as the memory length of the encoder.

C. Angle Generator: The all together the portion of phase generator, offset generator, CI code selector can be written as an angle generator. So the angle generator technique to store only $\pi / 2$ radians of sine information and to generate the sine look-up table samples for the full range of 2π quarter-wave symmetry of the sine function is used. As shown in Fig. 3. The two Most Significant Bit (MSB) s are used to decode the quadrant, remaining 10 bits are used to address a one-quadrant sine look-up table. MSB determines whether the amplitude is increasing or decreasing. The accumulator output is used “as is” for the first and the third quadrants. The bits must be complemented so that the slope of the saw-tooth is inverted for the second and fourth quadrant.

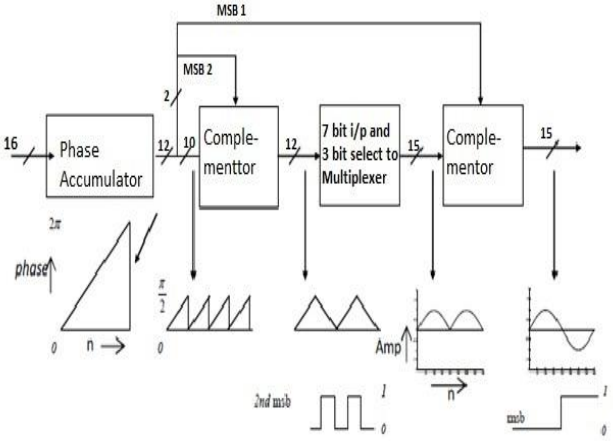

Figure 3: Angle Generator

D. Angle Adjustment: Fine tune or adjust the angle of generated wave.

E. CORDIC: Coordinate Rotation Digital Computer (CORDIC) technique, which uses an iterative computation method to generate carrier frequency**,** the only operations it requires are addition, subtraction, bit shift and table lookup. CORDIC is one such hardware-efficient algorithm that is used in DSP systems for calculating trigonometric, hyperbolic, logarithmic and other transcendental functions. This simplicity in operation has made CORDIC a competitive alternative for evaluating various trigonometric and hyperbolic functions required in many DSP applications. The original algorithm, developed by Jack Volder was limited to trigonometric calculations. John Walther extended the CORDIC theory and made it possible to calculate a large variety of trigonometric and other linear and hyperbolic functions.

FPGAs are often used as co-processors to perform all the high speed tasks that cannot be achieved using conventional processors. Historically, FPGAs have been slower, less energy efficient and generally achieved less functionality than their fixed ASIC counterparts. Advantages include the ability to re-program in the field to fix bugs, shorter time to market and lower non-recurring engineering cost.

F. QPSK Modulator: Digital phase modulation, or phase-shift keying (PSK), is very similar to frequency modulation. It involves changing the phase of the transmitted waveform instead of the frequency, and these finite phase changes represent digital data. For QPSK it can be assumed that the number of phase shifts is not limited to only two states. The transmitted "carrier" can

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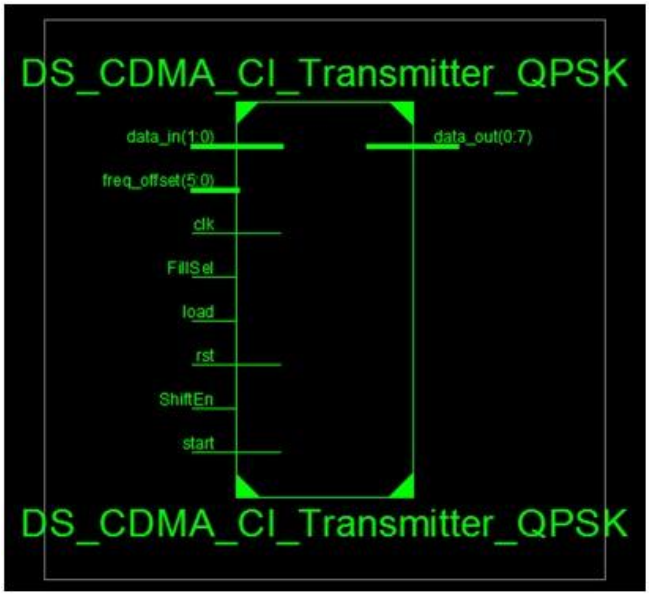
undergo any number of phase changes and, by multiplying the received signal by a sine wave of equal frequency, will demodulate the phase shifts into frequency-independent voltage levels. This is indeed the case in Quadrature phase-shift keying (QPSK). With QPSK, the carrier undergoes four changes in phase (four symbols) and can thus represent 2 binary bits of data per symbol. Although this may seem insignificant initially, a modulation scheme has now been supposed that enables a carrier to transmit 2 bits of information instead of 1, thus effectively doubling the bandwidth of the carrier.

QPSK is type of phase shift keying. Unlike BPSK which is a DSBCS modulation scheme with digital information for the message, QPSK is also a DSBCS modulation scheme but it sends two bits of digital information a time (without the use of another carrier frequency).

V. RESULTS

The top module of the DS CDMA-CI transmitter through CORDIC and QPSK modulator is



Following figure 4 is the QPSK waveform generated from the Simulation Tool- Modelsim6.3c. It is showing the change of phase in 2 bit data of sine and cosine waves. As the input is 00 the wave is sine wave, once the input is changed to 01 the wave is changed to cosine wave, once the input is changed to 10 the wave is changed to the negation of sine wave and once the input is changed to 11 then the output is changed to the negation of the cosine wave.

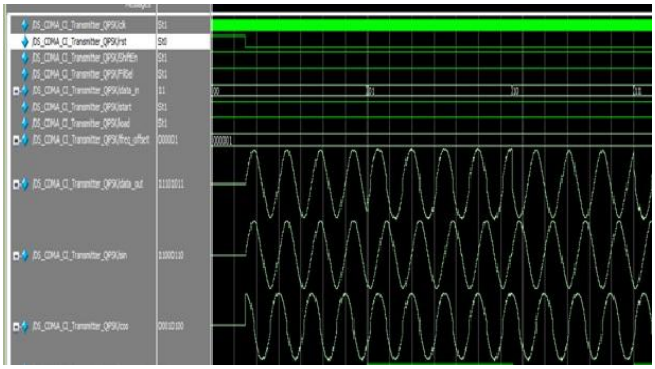


Figure 4: DS CDMA-CI transmitter through cordic and QPSK Modulator waveform.

Device Utilization Summary			
Logic Utilization	Used	Available	Utilization
Number of Slice Flip Flops	209	7,168	2%
Number of 4 input LUTs	624	7,168	8%
Number of occupied Slices	392	3,584	10%
Number of Slices containing only related logic	392	392	100%
Number of Slices containing unrelated logic	0	392	0%
Total Number of 4 input LUTs	758	7,168	10%
Number used as logic	624		
Number used as a route-thru	134		
Number of bonded IOBs	13	141	9%

Figure 5: DS CDMA-CI transmitter through cordic and QPSK Modulator Device utilization summary.

Power consumption contributes in the dissipated heat of the system and affects to the stability and long life of the system, if the consumption of power is less for an efficiently designed system then the stability and the life of the system will be increased.

Following are the figures of the power consumed by DS CDMA-CI transmitter through cordic and QPSK Modulator. As we can see that the power consumption is minimal for this is 60 mili Watts only.

	Total	Dynamic	Quiescent
Supply Power (W)	0.060	0.000	0.060

Figure 6: DS CDMA-CI transmitter through cordic and QPSK Modulator Power Consumption.

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VI. CONCLUSION

Designing of DS CDMA-CI Transmitter through cordic and QPSK Modulator gives the output of 2 bits data for sine and cosine waves. We get the same wave as sine wave when the input is 00, we get the same wave as cosine wave when the input is 01, we get the negation of sine wave when the input is 10 and We get the negation of cosine wave when the input is 11.So this implementation gives the less area requirement which provide the Compaq designing area, less complexity in architecture as the optimization is done for the logic gates and less power consumption which provide more stability and avoid unnecessary heating of system.

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