MULTILEVEL INVERTER WITH A STEP-UP SWITCHED-CAPACITOR & SELF VOLTAGE BALANCING

Fahmida Iqbal [1], Masarath Unnisa [2] Mohammed Abdul Rahman Uzair [3] and Ishrath Jahan [4]

[1]*Assistant Professor, Nawab Shah Alam Khan College of Engg & Tech, Hyderabad, INDIA.*

[2]*Assistant Professor, Nawab Shah Alam Khan College of Engg & Tech, Hyderabad, INDIA.*

[3]*Associate Professor, Nawab Shah Alam Khan College of Engg & Tech, Hyderabad, INDIA.*

[4]*Assistant Professor, Nawab Shah Alam Khan College of Engg & Tech, Hyderabad, INDIA.*

ABSTRACT: **The objective of this paper is to propose a new inverter topology for multilevel inverter technology has emerged recently as a very important alternative in the area of high-power medium-voltage energy control. This topology is designed based on switched-capacitor technique and the number of output levels is determined by the number of switched-capacitor cells. Only one DC voltage source is needed and the problem of capacitor voltage balancing is avoided as well. This structure is not only very simple and easy to be extended to higher level, its gate driver circuits are also simplified because the number of active switches is reduced. This paper also presents the most relevant control and modulation methods developed for this family of converters: multilevel sinusoidal pulse width modulation, multilevel selective harmonic elimination. The output is obtained by using MAT-LAB.**

Keywords: **Switched-capacitor, Multilevel voltage output, PWM, Capacitor voltage balancing, MATLAB.**

I. INTRODUCTION

Multilevel inverters have been introduced as an alternative in high power quality situations. For several attractive features such as near sinusoidal staircase output voltage waveforms, reduced d_v/d_t stresses and operating with lower switching frequency stress etc. multilevel inverters, as an alternative solution, have been receiving much attention. As results, many different topologies and wide variety of control strategies have been proposed.

The Inverter is an electrical device which converts direct current (DC) to alternate current (AC). The inverter is used for emergency backup power in a home. The inverter is used in some aircraft systems to convert a portion of the aircraft DC power to AC. The AC power is used mainly for electrical devices like lights, radar, radio, motor, and other devices.

Conventionally, multilevel inverter topologies can be divided into three categories: neutral-point-clamped flying capacitors and the H-bridge cascade. In many industrial applications, these inverters have been playing very important roles in the terms of high quality ac supplies and motor driver because of their good performance. However, their drawbacks are also apparent. For instance, multiple separated voltage sources are required for the H-bridge cascade topologies. And the problem of voltage balancing among DC link series capacitors exists in both neutral-point-clamped and capacitor-clamped inverters.

A simple topology is proposed but multiple separated DC voltage sources are still required. The structures are simplified but it is difficult to expand this technique to higher levels applications. Topologies based on switched-capacitor (SC) and boost techniques are presented but their numbers of output voltage levels are limited. In contrast, the multilevel topology introduced can be extended to higher levels. However, the use of a large number of active switches increases the cost and component counts in the terms of gate driver circuits and the overall system. Based on the SC technique which has been applied in many applications, a novel multilevel inverter topology connecting a multilevel DC-DC converter and a full bridge is presented in this paper.

II. DIODE CLAMPED MULTILEVEL INVERTER

The main concept of this inverter is to use diodes and provides the multiple voltage levels through the different phases to the capACitor banks which are in series. A diode transfers a limited amount of voltage, thereby reducing the stress on other electrical devices. The maximum output voltage is half of the input DC voltage.

It is the main drawback of the diode clamped multilevel inverter. This problem can be solved by increasing the switches, diodes, capacitors. Due to the capacitor balancing issues, these are limited to the three levels. This type of inverters provides the high efficiency because the fundamental frequency used for all the switching devices and it is a simple method of the back to back power transfer systems.

Ex: 5- Level diode clamped multilevel inverter, 9- level diode clamped multilevel inverter.

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The 5- level diode clamped multilevel inverter uses switches, diodes; a single capacitor is used, so output voltage is half of the input DC.

The 9-level diode clamped multilevel inverter uses switches, diodes; capacitors are two times more than the 5-level diode clamped inverters. So the output is more than the input.

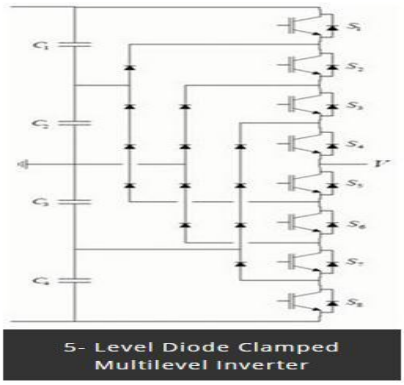

Figure1: The 5- level Diode Clamped Multilevel Inverter

III. FLYING CAPACITORS MULTILEVEL INVERTER

The main concept of this inverter is to use capacitors. It is of series connection of capacitor clamped switching cells. The capacitors transfer the limited amount of voltage to electrical devices. In this inverter switching states are like in the diode clamped inverter. Clamping diodes are not required in this type of multilevel inverters. The output is half of the input DC voltage.

Ex: 5-level flying capacitors multilevel inverter, 9-level flying capacitors multilevel inverter.

This inverter is same like that diode clamped multi inverter. In this inverter only switches and capacitors are used.

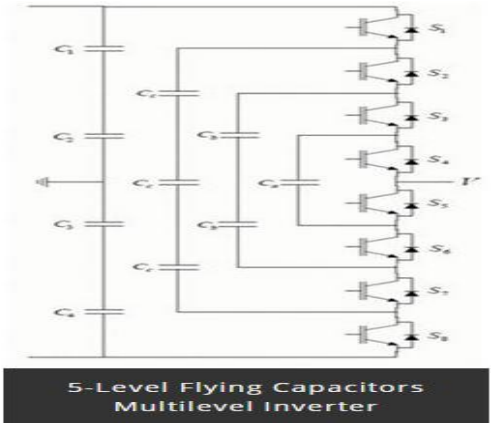

Figure2: (5) - Level Flying Capacitor Multilevel Inverter

In recent years, numerous new multilevel inverter topologies which cannot be attributed to the traditional classifications aforementioned have been reported. Specifically, multiple sub-multilevel converter units and full-bridge converters are employed in the new multilevel inverter topology.

IV. CASCADED H-BRIDGE

A single-phase structure of an m-level cascaded inverter is illustrated in Fig: 3. each separate DC source (SDCS) is connected to a single-phase full-bridge, or H-bridge, inverter. Each inverter level can generate three different voltage outputs, $+V_{DC}$, 0, and $-V_{DC}$ by connecting the DC source to the ac output by different combinations of the four switches, S_1, S_2, S_3, and S_4. To obtain $+V_{DC}$, switches S_1 and S_4 are turned on, whereas $-V_{DC}$ can be obtained by turning on switches S_2 and S_3. By turning on S_1 and S_2 or S_3 and S_4, the output voltage is 0. The AC outputs of each of the different full-bridge inverter levels are connected in series such that the synthesized voltage waveform is the sum of the inverter outputs. The number of output phase voltage levels m in a cascade inverter is defined by m = 2s+1, where s is the number of separate DC sources.

An example phase voltage waveform for an 11-level cascaded H-bridge inverter with 5 SDCSs and 5 full bridges is shown in Fig: 4. the phase voltage van = $va_1 + va_2 + va_3 + va_4 + va_5$.

For a stepped waveform such as the one depicted in Fig with s steps, the Fourier Transform for this waveform follows:

$$V(\omega t) = \frac{4V_{DC}}{\pi} \left[\cos(n_1\Theta) + \cos(n_2\Theta) + \ldots + \cos(n_s\Theta) \right] \frac{\sin(n\omega t)}{n}$$

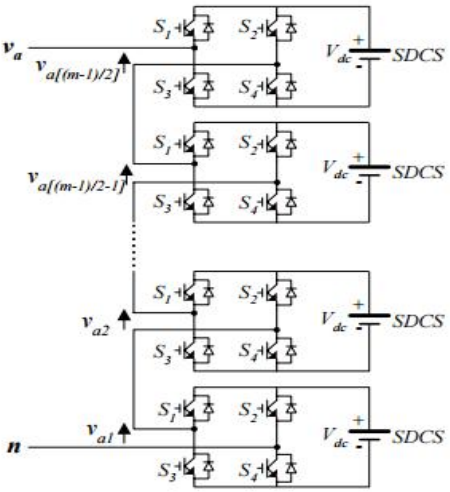

Figure3: Single phase structure of a multi level cascaded H-bridge inverter

Where n=1, 3, 5, 7 …

The magnitudes of the Fourier coefficients when normalized with respect to V_{DC} are as follows:

$$H(n) = \frac{4}{\pi n} \left[\cos(n\Theta_1) + \cos(n\Theta_2) + \ldots + \cos(n\Theta_s) \right]$$

Where n=1, 3, 5, 7..

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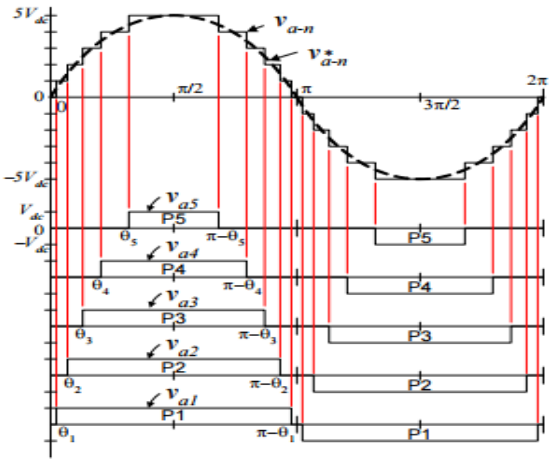

Output phase voltage waveform of an 11-level cascade inverter with 5 separate dc sources.

Figure4: Output voltage waveform of 11-level cascaded inverter with 5 separate DC source

The conducting angles, θ_1, θ_2... θ_s, can be chosen such that the voltage total harmonic distortion is a minimum. Generally, these angles are chosen so that predominant lower frequency harmonics, 5th, 7th, 11th, and 13th, harmonics are eliminated. Multilevel cascaded inverters have been proposed for such applications as static var generation, an interface with renewable energy sources, and for battery-based applications.

The number of possible output voltage levels is more than twice the number of DC sources (m = 2s + 1). The series of H-bridges makes for modularized layout and packaging. This will enable the manufacturing process to be done more quickly and cheaply.

V. CIRCUIT DESIGN DESCRIPTION

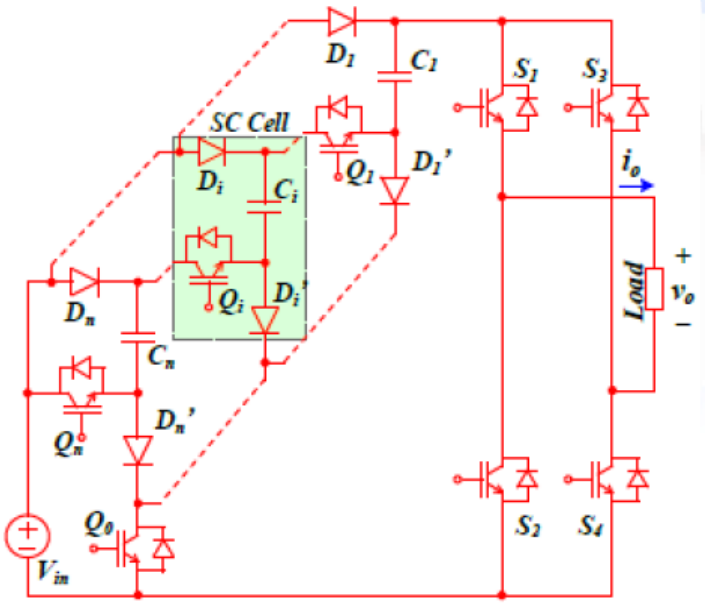

Figure5: Circuit Diagram

VI. MODULATION AND CONTROL STRATERGIES

The modulation methods used in multilevel inverters can be classified according to switching frequency, Methods that work with high switching frequencies.

There are two types of frequency modulating techniques:

For HFM methods, there are many commutations for the power switches in one period of the fundamental output voltage.

The HFM can be further divided into several specific modulation methods, of which a very popular one is the multilevel carrier-based sinusoidal PWM (SPWM). Therefore, this method will be introduced to control the proposed inverter.

For FFM methods, a staircase voltage waveform is generated by connecting different number of capacitor sources to the output terminal and with only one or two commutations of active switches during one cycle of fundamental output voltage. A representative of this family is the selective harmonic elimination (SHE) method. It also been introduced to modulate the proposed inverter to output a staircase voltage.

Fundamental switching frequency:

The selective harmonic elimination method is also called fundamental switching frequency method based on the harmonic elimination theory. A typical11-level multilevel converter output with fundamental frequency switching scheme is shown in Figure4.

The conducting angles Θ_1 Θ_2 Θ_3, can be chosen such that the voltage total harmonic distortion is a minimum. Normally, these angles are chosen so as to cancel the predominant lower frequency harmonics. For the 11-level case, the 5th, 7th, 11th, and 13th harmonics can be eliminated with the appropriate choice of the conducting angles.

One degree of freedom is used so that the magnitude of the fundamental waveform corresponds to the reference waveform's amplitude or modulation index ,*ma*, which is defined as V_L/V_{LMax} of the inverter for a sine wave output phase voltage,. V_L* is the amplitude command, V_{LMax} *is* the maximum attainable amplitude of the converter, i.e.,

$$V_{LMax} = S.V_{DC}$$

$$\text{Cos}(5\Theta_1) + \text{Cos}(5\Theta_2) + \text{Cos}(5\Theta_3) + \text{Cos}(5\Theta_4) + \text{Cos}(5\Theta_5) = 0$$

$$\text{Cos}(7\Theta_1) + \text{Cos}(7\Theta_2) + \text{Cos}(7\Theta_3) + \text{Cos}(7\Theta_4) + \text{Cos}(7\Theta_5) = 0$$

$$\text{Cos}(11\Theta_1) + \text{Cos}(11\Theta_2) + \text{Cos}(11\Theta_3) + \text{Cos}(11\Theta_4) + \text{Cos}(11\Theta_5) = 0$$

$$\text{Cos}(13\Theta_1) + \text{Cos}(13\Theta_2) + \text{Cos}(13\Theta_3) + \text{Cos}(13\Theta_4) + \text{Cos}(13\Theta_5) = 0$$

$$\text{Cos}(\Theta_1) + \text{Cos}(\Theta_2) + \text{Cos}(\Theta_3) + \text{Cos}(\Theta_4) + \text{Cos}(\Theta_5) = 5m_a$$

These above equations are nonlinear transcendental equations that can be solved by an Iterative method such as the Newton-Raphson method.

Thus, if the inverter output is symmetrically switched during the positive half cycle of the fundamental voltage to $+V_{DC}$ at 6.57°, $+2V_{DC}$ *at* 18.94°, $+3V_{DC}$ at 27.18°, $+4V_{DC}$ at 45.14°, and $+5V_{DC}$ at 62.24°, and similarly in the negative half cycle to V_{DC} at 186.57°, $-2V_{DC}$ at 198.94°, $-3V_{DC}$ at 207.18°, $-4V_{DC}$ at 225.14°, $-5V_{DC}$ at 242.24°, the output voltage of

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the 11-level inverter will not contain the 5th, 7th, 11th, and 13th harmonic components.

Selective harmonic elimination PWM:

A Pulse Width Modulation (PWM) Signal is a method for generating an analog signal using a digital source. A PWM signal consists of two main components that define its behavior: a duty cycle and a frequency.

The duty cycle describes the amount of time the signal is in a high (on) state as a percentage of the total time of it takes to complete one cycle. The frequency determines how fast the PWM completes a cycle (i.e. 1000 Hz would be 1000 cycles per second), and therefore how fast it switches between high and low states.

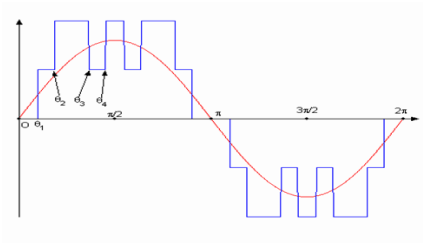
PWM signals are used for a wide variety of control applications. Their main use is for controlling DC motors but it can also be used to control valves, pumps, hydraulics, and other mechanical parts. The frequency that the PWM signal needs to be set at will be dependent on the application and the response time of the system that is being powered. Below are a few applications and some typical minimum PWM frequencies that are required:

Heating elements or systems with slow response times: 10-100 Hz or higher

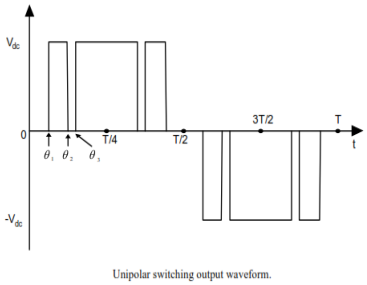
DC electric motors: 5-10 kHz or higher

Power supplies or audio amplifiers: 20-200 kHz or higher

In order to achieve a wide range of modulation indexes with minimized THD for the synthesized waveforms, a generalized selective harmonic modulation method was proposed, which is called virtual stage PWM. An output waveform is shown in Figure 6. The Virtual Stage PWM is a combination of Unipolar Programmed PWM and the Fundamental frequency switching scheme. The output waveform of Uni-polar Programmed PWM is shown in Figure 7. When Uni-polar Programmed PWM is employed on a multilevel converter, typically one DC voltage is involved, where the switches connected to the DC voltage are switched "on" and "off" several times per fundamental cycle. The switching pattern decides what the output voltage waveform looks like.



Output waveform of virtual stage PWM control.



Unipolar switching output waveform.

Figure6: Uni-polar Programmed PWM

For fundamental switching frequency method, the number of switching angles is equal to the number of DC sources. However, for the Virtual Stage PWM method, the number of switching angles is not equal to the number of DC voltages. For example, in Figure 5, only two DC voltages are used, whereas there are four switching angles.

Bipolar Programmed PWM and Unipolar Programmed PWM could be used for modulation indices too low for the applicability of the multilevel fundamental frequency switching method. Virtual Stage PWM can also be used for low modulation indices. Virtual Stage PWM will produce output waveforms with a lower THD most of the time. Therefore, Virtual Stage PWM provides another alternative to Bipolar Programmed PWM and Unipolar Programmed PWM for low modulation index control.

VII. VOLTAGE BALANCING OF CAPACITORS

The switched-capacitor part plays a role in balancing the voltages of capacitors by alternative conduction of the clamping switches Sc_1 - Sc_6. When the switching devices of Group A are ON and those of Group B are OFF, C_1 and C_3, C_2 and C_4 are in parallel, respectively, so $V_{C1} = V_{C3}$ and $V_{C2} = V_{C4}$.

When the switching devices of Group B are ON and those of Group A are OFF, C_1 and C_4, C_2 and C_5 are in parallel, respectively, so $V_{C1} = V_{C4}$ and $V_{C2} = V_{C5}$. If the switching devices of Group A are turned from ON to OFF, and from OFF to ON over and over again, then $V_{C1} = V_{C2} = V_{C3} = V_{C4} = V_{C5}$. That is to say, each capacitor can keep voltage balance through the capacitor C_4.

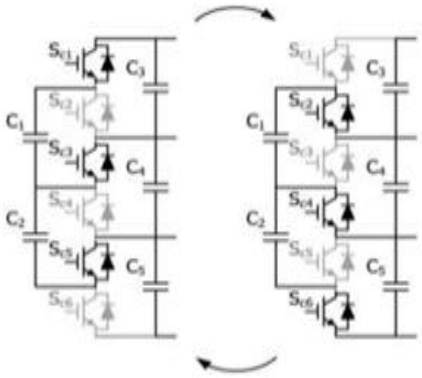


Figure7: Switched Capacitors

Actually, the capacitor C_4 acts as the second spiker, which is in parallel with different DC link capacitors in different

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switching states. So long as Group A or Group B can switch once in one period, the voltages of the capacitors can keep balance. As seen from Table-1, the switching devices of Group B or Group A are ON for one working state and OFF for the other working state.

Table-1: Working states and group distribution

No. of Working States	Output Level V_s	S_1	S_2	S_3	S_4	S_5	S_6	Group A	Group B
1	$+2V_{DC}$	1	1	1	0	0	0	0	1
2	$+1V_{DC}$	1	1	1	0	0	0	1	0
4	$0V_{DC}$	0	1	1	1	0	0	1	0
6	$-1V_{DC}$	0	0	1	1	1	0	1	0
8	$-2V_{DC}$	0	0	0	1	1	1	1	0

It can be seen from Table-1 that for the first working states combination, the switching devices of Group B are turned on only when the highest output level ($+2V_{DC}$) appears and turned off when other four output levels appear. The pulse width modulation (PWM) carrier's arrangement of this working states combination is shown in Fig.9 (a). As seen from Fig.9 (a), every carrier band from top down corresponds to Group B, S_1, S_2, and S_3 in turn.

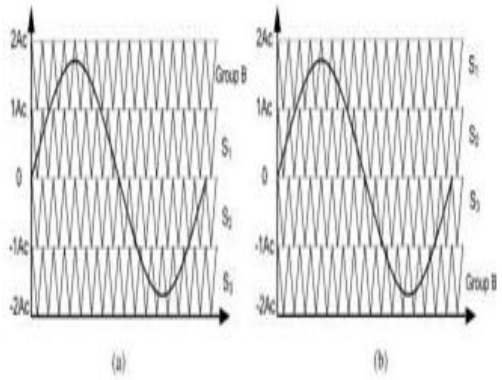

Figure8: PWM carriers arrangement

The capacitor voltage balancing can be realized only when the switching devices of Group B are turned on and off alternately; otherwise, the voltage balancing in capacitors will be broken under the condition of a lower modulation ratio. So these two kinds of working states combination must be considered together to ensure the normal operation within the wider range of modulation degree (even less than 0.5). As a result, the switching devices of Group B are turned ON over one switching period and turned off over the next switching period, and so on.

Table-2: Working states and group distribution

No. of Working States	Output Level V_s	S_1	S_2	S_3	S_4	S_5	S_6	Group A	GroupB
1	$+2V_{DC}$	1	1	1	0	0	0	0	1
3		0	1	1	1	0	0	0	1
5		0	0	1	1	1	0	0	1
7		0	0	0	1	1	1	0	1
8	$-2V_{DC}$	0	0	0		1	1	1	0

VIII. LOSSES

The key power losses are the conduction and switching losses in the inverter devices. Occurrence of the conduction losses is due to the declining voltage across the device as well as the current flow through the device. Switching losses are sustained by the concurrent occurrence of voltage and current on the device while switching.

A. *Conduction Losses:*

To evaluate conduction loss, the device is simplified as a constant voltage drop in series with a linear resistor. For both IGBTs and diodes, this simplified model is appropriate. The expression for the on-state voltage of an IGBT and a diode is shown in Equations, respectively.

$$V_{ce} = V_q + I_q .R_q$$
$$V_{ak} = V_d + I_d .R_d$$

I_q and I_d denotes the current flowing through the IGBT and diode, respectively. V_{ce} and V_{ak} denote the voltage across the IGBT and Diode. The parameters, V_q, R_q, V_d, and R_d can be extracted from data sheets. Powers dissipated in a component with a constant voltage drop correspond to the average current times the voltage drop. The r.m.s current squared times the resistance signifies the power dissipated in a resistor. To ease the calculation of the IGBT and diode currents, the load current is assumed to be sinusoidal. Calculating the average and rms currents of the IGBT and diode in an inverter (given sinusoidal pulse width modulation), using Equations below:

$$I_q(avg) = I_0(pk)\left[\frac{1}{2\pi} + \frac{m_a \cos \phi}{8}\right]$$
$$I_q(r.m.s) = I_0(pk)\sqrt{\left[\frac{1}{8} + \frac{m_a \cos \phi}{3\pi}\right]}$$
$$I_d(avg) = I_0(pk)\left[\frac{1}{2\pi} - \frac{m_a \cos \phi}{8}\right]$$
$$I_d(r.m.s) = I_0(pk)\sqrt{\left[\frac{1}{8} - \frac{m_a \cos \phi}{3\pi}\right]}$$

Where I_0 (pk) denotes the peak load current, **ø** denotes the power factor angle, and ma denotes the modulation index. With the simplified models, the conduction losses in the IGBT, $P_{q\text{-}con}$ diode, $P_{d\text{-}con}$, are obtained using Equations below:

$$P_{q\text{-}con} = V_q.I_q(avg) + R_q.\, I_q(r.m.s)^2$$

$$P_{d\text{-}con} = V_d.I_d(avg) + R_d.\, I_d(r.m.s)^2$$

The total conduction losses, $P_{tot\text{-}con}$ of 4 IGBTs and diodes are given by Eqn:

$$P_{tot\text{-}con} = 4[\, P_{q\text{-}con} + P_{d\text{-}con}]$$

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Evidently, considering device characteristics, the conduction losses are only reliant on load conditions.

B. Switching Losses:

Three components of the switching losses in the inverter can be identified; IGBT turn on losses, IGBT turn off losses, and the losses due to diode reverse recovery. Evaluation of the switching losses in the inverter can be done using the measured values of switching energy from the data sheets.

Generally, data sheets provide the calculated values of turn-on and turn-off energy (E_{on} and E_{0ff}) for a conventional test voltage and current (V_{test} and I_{test}). The calculated values of turn-on energy comprise the losses due to diode reverse recovery. These standards should be leveled suitably for a specific application using Equation:

$$E_{tot} = K_g \,.\, (E_{on} + E_{0ff}) \,.\, \frac{V_s}{V_{test}} \,.\, \frac{I_0(pk)}{I_{test}}$$

Equation represents V_s as the bus voltage, I_0 (pk) as the peak load current, and K_g as the correction factor to account for the gate drive impedance. Calculation for the total switching losses, $P_{tot\text{-}sw}$, switching inverter can be done using:

$$P_{tot\text{-}sw} = 4f_s \,.\, \frac{E_{tot}}{\pi}$$

Where, f_s denotes the PWM switching frequency.

IX. SIMULATION

A simulation design open loop system as shown is implemented in MATLAB SIMULINK with the help of switches and voltage sources we get desired output voltage level. **MATLAB** (**mat**rix **lab**oratory) is a numerical computing environment and fourth-generation programming language]. Developed by Math Works,

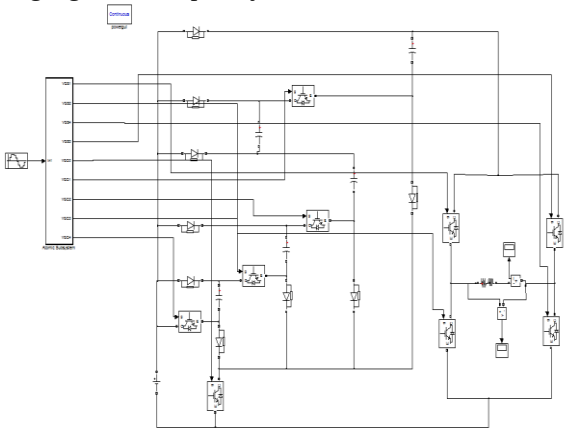

Figure9: Proposed Circuit Design

X. OUTPUT VOLTAGE WAVE FORM

The output waveform can be of two types:

- Sine wave
- Modified sine wave

While converting from DC voltage to AC voltage, there are two methods or modes:

Either we convert the DC signal into Higher-Power DC signal and then convert it into AC,OR we convert DC to AC at the lower level and then using line frequency we get the required output voltage.

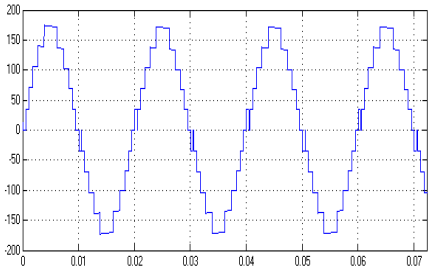

Figure10: 11-Level Output

XI. CONCLUSION

It has demonstrated the state of the art of multilevel power converter technology. Fundamental multilevel converter structures and modulation paradigms including the pros and cons of each technique have been discussed. It enables the simple structure and low cost of the circuits. And the voltage ripples across capacitors and power losses are analyzed in detail as well. Finally, the operation and performance of the proposed inverter are verified with experiments on an eleven-level inverter.

Good performance could be obtained in both high switching frequency and fundamental switching frequency modes. Therefore, the proposed inverter is more suitable for high frequency applications. The intention of the authors was simply to provide groundwork to readers interested in looking back on the evolution of multilevel inverter technologies, and to consider where to go from here.

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Fahmida Iqbal was born in Hyderabad, India. She completed her BTech in Electrical and Electronics Engineering from JNTU Hyderabad in 2013. She completed her MTech in Power Electronics from JNTU Hyderabad in the year 2015. Currently, she is working as Assistant Professor in the Department of EEE at Nawab Shah Alam Khan College of Engg & Tech, Hyderabad. Her fields of interest are Power Systems and Power Electronics.

Masarath Unnisa was born in Hyderabad, India. She completed her BE in Electrical and Electronics Engineering from OU, Hyderabad in 2012. She completed her MTech in Power Electronics from JNTU Hyderabad in the year 2015. Currently, she is working as Assistant Professor in the Department of EEE at Nawab Shah Alam Khan College of Engg & Tech, Hyderabad. Her fields of interest are Power Systems, Electrical Machines and Power Electronics.

Mohammed Abdul Rahman Uzair was born in Nalgonda, a district headquarter nearly 100kms from Hyderabad, India. He completed his BTech in Electrical and Electronics Engineering from JNTU Hyderabad. He completed his MTech in Electrical Power Engineering from JNTU Hyderabad in the year 2012. Currently, he is pursuing PhD from GITAM University, Hyderabad campus on the topic 'Failure Analysis of Power Transformers'. He is working as Associate Professor in the Department of EEE at Nawab Shah Alam Khan College of Engg & Tech, Hyderabad. His fields of interest are Power Systems and Power Electronics. He has published one paper in a National Journal (2011) and thirteen papers in International Journals apart from an IEEE paper (2015).

Ishrath Jahan was born at Hyderabad, India. She completed her BE in Electrical and Electronics Engineering in 2006 from OU Hyderabad. She completed her MTech in Power Electronics from JNTU Hyderabad in the year 2014. Currently, she is working as Assistant Professor in the Department of EEE at Nawab Shah Alam Khan College of Engg & Tech, Hyderabad. Her field of interest is Power Electronics.

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