LOW POWER AND HIGH PERFORMANCES FLIP-FLOPS

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***Abstract*— The power consumption is very important in modern VLSI circuits especially for low-power applications. Optimization of power at the logic level is an important task to minimize the power. Latches and flip-flops are critical to the performance of digital systems among logic components. This paper presents a detailed analysis of transmission gate master slave flip-flop, hybrid latch flip-flop and Conditional Pulse Enhancement flip-flop which is a type of pulse triggered flip-flop for 90nm and 45nm. This paper consists of a comparison of three flip-flop classes in terms of timing parameter and power dissipation. The analysis shows the best performance of CPEFF design for timing parameters and transmission gate master slave flip-flop for power consumption.**

***Index Terms*— CMOS, Flip-flop, High performances, Low power.**

I. INTRODUCTION

The performance of VLSI integrated circuits is strongly influenced by the clock network design and appropriate choice of flip flops (FFs). Flip Flops are extremely important circuit elements in all synchronous VLSI circuits. They are responsible for correct timing, functionality and performance of the chip, but they and other clock distribution networks consume a large part of the total power of the circuit. In particular, flip-flops are widely used for memory design and test application. Here, comes the need of low power flip flop and latches.

Storage elements such as flip-flops and latches must be as simple as possible and satisfy various requirements of synchronous systems such as rigid timing constraints and low power dissipation. Timing parameters such as data-to-output delay and setup and hold times are important because the timing budget is getting tighter as the clock frequency increases. Power requirement is also becoming equally important, because the power consumption increases with an increase in clock frequency while the power budget of high-performance portable digital systems is severely limited.

In this paper, we present a detailed analysis of the average power, and timing metrics like setup in two different styles of flip-flops designed using different technology node in CMOS process. The designs evaluated encompass two widely used design styles: Transmission gate master-slave, pulse-triggered.

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II. HIGH PERFORMANCE AND LOW POWER NEED

Today, there is a large demand of high performance devices with low power application. However, this type of design implementation produces a trade-off condition in VLSI design technique. A high performance flip-flop works with a greater frequency which increase the power consumption. Therefore, a greater insight is needed to produce an optimized design for use. The major advantage of using CMOS is its extremely low static power dissipation, but trends have shown that the power dissipation of VLSI circuit is increasing fourfold in every three years. The major research in this area is to find the contribution of input and clock in total power dissipation. Therefore, techniques like dual edge triggering swing are used to reduce clock power dissipation. Various high performances flip-flops are Hybrid Latch flip-flop (HLFF) and Semi dynamic flip flop. These flip-flops are crucial in high speed SOC design, having best timing parameters like small data to Q delay, negative setup time and logic embedding with small penalty. Transmission gate flip-flops are best low power implementing device having small clock to Q delay and large setup time making large data to Q delay. All these parameters are further discussed in next section with different designing scope like timing metrics.

III. TIMING METRICS

DATA and CLOCK inputs of clocked storage needs to satisfy basic timing restriction to ensure correct operation of flip-flop. Fundamental timing metrics of flip-flops are setup time and hold time. Setup time and hold time defines time interval during which input has to be stable for the correct operation of flip flop. The sum of setup time and hold time defines the sampling window.

All the hard edge triggered flip flop like master-slave flip-flop and sense amplifier flip-flop have positive setup time and causes large input to output delay. On the other hand pulse triggered flip flops are soft edge triggered flip flop having low logic complexity due o reduction of two stage into one leading to small input to output delay. These types of flip-flop shows negative setup time property. Hybrid latch flip-flop (HLFF) and sense amplifier flip-flop are pulse triggered flip-flop having negative setup time property.

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IV.TRANSMISSION GATE LATCH BASED MASTER-SLAVE FLIP-FLOP

Fig. 1 shows the schematic diagram of CMOS edge triggered master-slave D flip-flop using Transmission Gate. This flip-flop is implemented by using two transmission gate based latches operating on complementary clocks.

Transmission Gate flip-flop (TGFFs) have a fully static master–slave structure, built by cascading two identical pass-gates latches and provides a short clock-to-output delay.

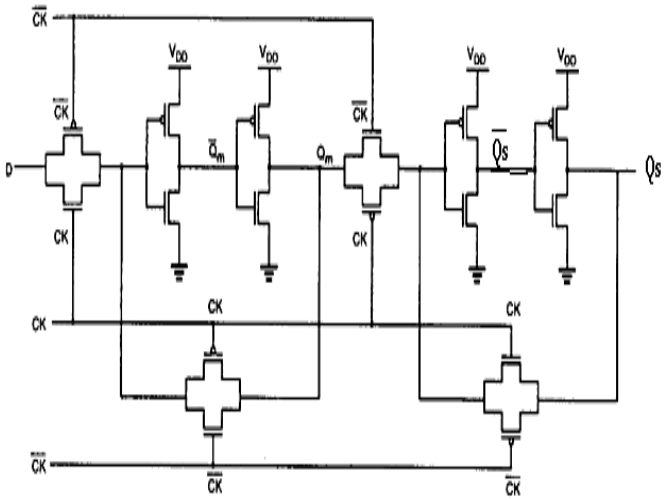

Fig.1 CMOS negative edge triggered master-slave D flip-flop using transmission gate

However, it has poor data-to-output latency because of positive setup time. It also requires two phases of clock that can cause a problem with data feed through when there is a skew between them and it has a relatively large clock load.

The first stage called master is driven by the clock signal, while the second stage is driven inverted clock signal. Transmission gate flip-flop is considered as low power flip-flop.

IV. MODIFIED HYBRID LATCH FLIP-FLOP (MHLFF)

The structure of modified hybrid latch flip flop is shown below in fig.2. This flip-flop consists of static latch structure. A static latch can store the data as long as power is supplied. It uses feedback to store the data, rather using a charge of capacitor. This flip-flop avoids the unnecessary node transition by allowing only different logic to make transition in two successive clock cycles.

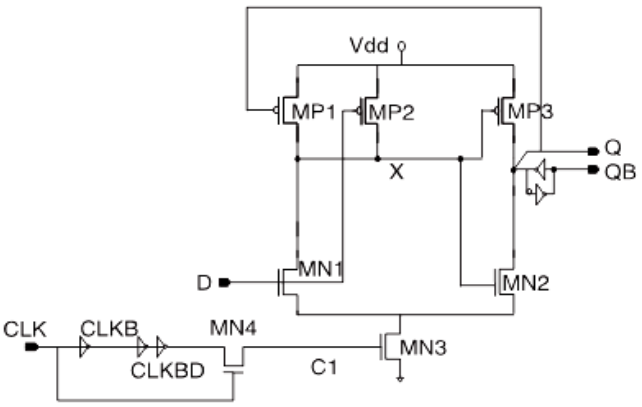

Fig.2 Modified Hybrid Latch Flip-flop

The working of this flip-flop is explained here. When CLK makes a transition from low to high, CLKBD remains high for a period of three inverters delay, creating a transparency window during which time period, C1 becomes high turning on MN3. Also, in this window, if D is low and Q is high, MP2 becomes on turning on MN2 and forcing output to become low. If both D and Q are low, MP1 and MP2 become on before the beginning of transparency window making the delay zero. If D is high and Q is low node X becomes low turning on MP3 and making output high. If D is high and Q is high, node X remain same, avoiding the redundant transition.

V. CONDITIONAL PULSE ENHANCEMENT FLIP-FLOP (CPEFF)

Master-slave flip-flops are characterized by having a hard edge and a positive setup time, causing large data to output (*D-Q*) delay whereas Hybrid flip-flop has a drawback of large clock delay due to 3 delay inverter and also this increases area of the circuit design. Reduction of two stage into one and soft edge property with negative setup time are some of the important characteristics of pulse-triggered flip-flops , that results in small D-Q delay, which reduces the delay penalty and also helps in absorbing the clock skew. Pulse -triggered flip flops also have small clock delay and smaller area. The structure of conditional pulse enhancement flip flop is shown below in fig.3. This flip-flop is based on the technique of clock gating which makes change in the input when there is a change in output reducing the power consumption.

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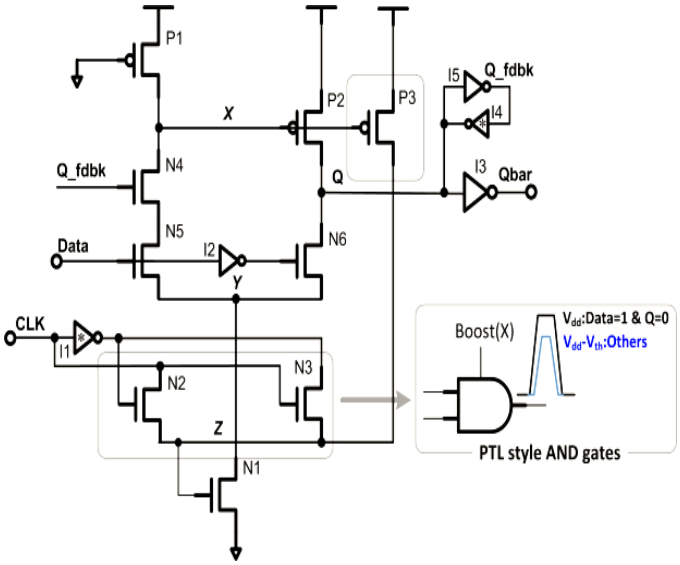

Fig.3 Conditional pulse enhancement flip-flop

This flip-flop consists of pulse generator comprising of delay inverter I1 and two nmos transistor N2 and N3. A simple PTL AND gate is used to boost the voltage, reduce circuit complexity and faster discharge operation. These types of flip-flop are used in high speed operation and features negative or zero setup time.

VI. RESULTS AND SIMULATION

The performance comparison of all the flip-flops for 90nm and 45nm is done using the above schematic diagram. The operating condition used in simulation is 500MHz/1.4v for 90nm technology and 500MHz/1.2v for 45nm technology. All the transistors are designed to function properly with l=90nm and 45nm respectively. The simulation results consist of output waveform to check the proper functionality, average power consumption, setup time, hold time and data to output delay. Fig.4 represents the output waveform for 90nm master slave D-flip-flop according to standard input parameter explained before.

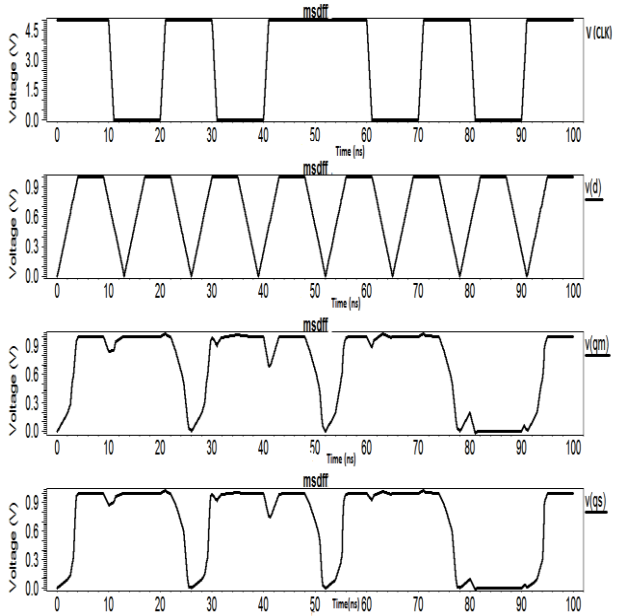

Fig.4 Simulated waveform for 90nm master slave D-flip-flop design

Fig.5 represents the output simulation of MHLFF for 90nm technology. Pulse-triggered flip-flops generate pulses during the active clock edge, which results in a transition at the output. This technique makes the flip-flop switch faster. This is the case especially with the hybrid latch flip-flop (HLFF), which has very low propagation delay, setup and hold time.

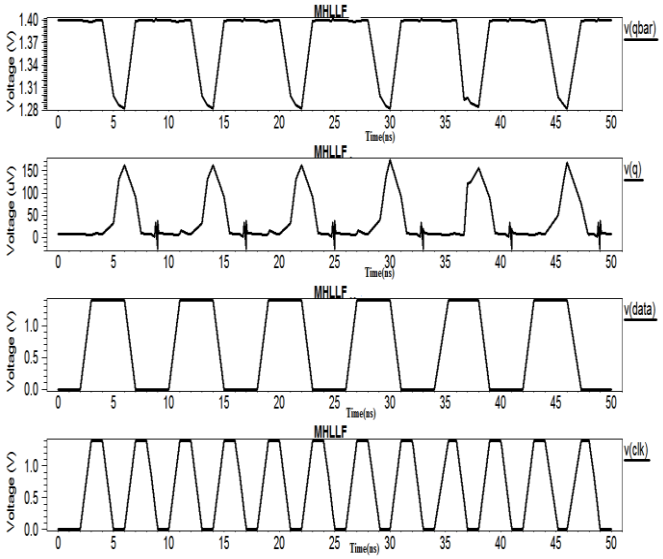

Fig.5 Simulated waveform for 90nm MHLFF design

Fig.6 shows the simulated waveform for 90nm CPEFF design.

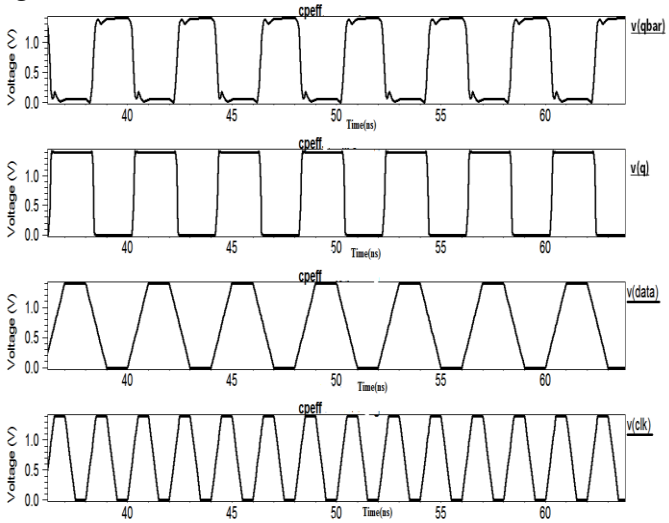

Fig.6 Simulated waveform for 90nm CPEFF design

Table I represents the output results of three flip-flops for 90nm and 45nm technology and provides a comparative study for the designs.

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Table. I Simulated output results of D- FF, MHLFF, and CPEFF

Flip-Flop (Name)		Master slave D-ff		MHLFF		CPEFF	
Technology used (nm)		90	45	90	45	90	45
Output	Setup Time(ns)	14	10.2	-4	-4.97	-2.25	-6.37
	Avg.Power (µw)	16.3	2.43	54	44	95	37

VII. CONCLUSION

In this paper, three different high performances and low power flip-flop designs are discussed for 90nm and 45nm technology. According to the performances of the flip-flops in terms of timing metrics and average power consumption, CPEFF design is proved best among the three.

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