Razor Based Modified Booth Multiplier

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***Abstract*—Multipliers perform the most frequently encountered arithmetic operations in DSP applications. The Razor based multi precision (MP) multiplier that incorporates various precision, parallel processing (PP) and dedicated MP operands scheduling to provide optimum performance for a various operating conditions. This reconfigurable multiplier can either work as independent smaller-precision multipliers or it also works parallel to form higher-precision multipliers. To reduce area of Razor based modified booth multiplier which incorporates variable precision, parallel processing (PP) and Razor based dynamic voltage scaling to provide optimum performance for a variety of operating conditions. The Razor based modified booth multiplier enables voltage scaling for low power operation, while still maintaining full throughput. A dynamic voltage scaling circuit can autonomously configure the multiplier to operate with the lowest possible voltage to achieve the lowest power consumption. Razor flip-flops help to reduce voltage safety margins and overhead typically associate to dynamic voltage scaling to the lowest level. Finally, the experimental result shows that the proposed MP Razor based multiplier features a reduction in circuit area and power.**

Keywords— dynamic voltage scaling, multi-precision (MP), parallel processing (PP), Razor flip-flop

I. INTRODUCTION

The demand for low power, high performance portable devices has been greatly increased. The growing market of portable electronic systems demands microelectronic circuits design with low power dissipation. Power dissipation is due to internal components [1]. In Digital Signal Processing applications, most frequently used arithmetic operation is multiplication. So Multipliers play an important role in today's digital signal processing and various other applications. With advances in technology, many researchers have tried and are trying to design multipliers which offer either of the following design targets – high speed, low power consumption and hence less area or even combination of them in one multiplier thus making them suitable for various high speed, low power VLSI implementation. Since Multiplication is a fundamental operation in most signal processing applications, Multipliers used in these applications have large area and consume considerable power. Therefore design of low-power multiplier has been an important part in low- power VLSI system design .Fast multipliers are essential parts of digital signal processing systems. The basic multiplication principle is two parts i.e., evaluation of partial products and accumulation of partial products. Many DSP systems is frequently truncated output due to the fixed register size and bus width inside the hardware and also disconnect the unused sections of multiplier to reduce dynamic power reduction can be achieved. Because of this significant power saving can be achieved by removing some adder cells. But in case of computing Least Significant (LSB) bits of product, this will cause large truncation errors. Various error compensation approaches and circuits can be used for the estimated compensation carries to the carry inputs of the retained adder cells to reduce the truncation error.

II. BACKGROUND

Due to the complex structure and interconnections, multipliers have large amount of unbalanced path which causes unwanted signal generation and propagation. This can be avoided by proper internal balancing through architectural and transistor level optimization. In most cases of multipliers, maximum word length is provided. Hence small multiplications are done in large multipliers, this causes unwanted switching activity and also power consumption. So word length optimization is the best method in which 8-bit multiplier is reused for 16-bit and 32-bit multiplication [2], [3]. Here it is possible to incorporate the pipelining for increasing the speed of the multiplier. Design of MP multiplier using operands scheduler and also storing min voltages for multiplication in LUT provide dramatic power reduction and also reduce delay. A predictable decrease in area overhead also can be achieved. In conventional DVS technique; LUT tunes to supply voltages which are stored as predefined voltage and frequency relationship by considering all worst case conditions. It will consume more time and area. In razor based DVS technique, minimum voltage required for multiplication using razor based feedback and also many voltage transitions occurred during the calculation of particular product [1]. Due to this voltage transitions power consumptions and delay for product calculation is also increases. Because of dynamic voltage scaling unit, increased number of preemptions and frequency switching occurs which leads to worst case power consumption and delay and did not get optimum performance at various operating conditions.

The concept of this paper includes: the Razor based MP multiplier reduces power consumption and delay and also reduce the additional area overhead than conventional 32 x 32 bit fixed width multiplier. This multiplier is also consists of operand scheduler which rearranges the input operands and hence reduce voltage transition, thus provide low power consumption.

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I. PROPOSED METHODOLOGY

Figure 1 show over all multiplier system architecture. The overall multiplier system mainly consists mainly 3 units.1) MP multiplier is one which performs multiplication with variable precision and parallel processing. 2) Voltage scaling unit gives the required voltage for multiplication. 3) voltage management unit (VMU) which is receives user requirement and control the VSU by giving suitable voltage.

All the three building blocks are working together to perform multiplication with variable precision. This multiplier initially works at standard supply voltage of 3.3v. Since LUT stores the minimum voltage for each combinations, depending on the incoming operands precision adjust the input voltage suitable for that particular combination. LUT stores 1.3v for 8-bit multiplication, 1.7v for 16-b, and 2.2v for 32-b multiplication.

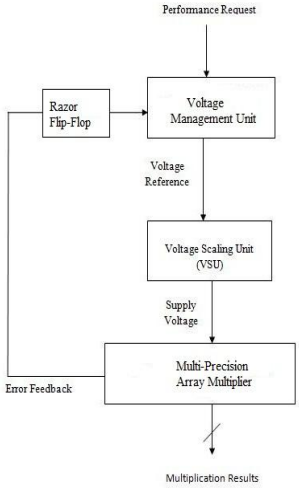

Fig 1. Overall Multiplier System Architecture

Figure 2 shows the multiplier which consist nine 8 x 8 bit multipliers. All these multipliers perform individual 8x8 bit operation and also can perform parallel multiplication for 16-bit and 32-bit multiplication. The processing elements of multiplier can either work as 9 independent multipliers or work in parallel to form one, two, or three 16 x 16 bit multiplier or a single 32- bit multiplication operation. The pipelining method reduces delay and also gets fast multiplication result without error.

Parallel processing is the ability of a device to simultaneously process incoming different inputs. Pipelining increases instruction throughput by performing multiple operations at the same time (concurrently), but does not reduce instruction latency (the time to complete a single instruction from start to finish) as it still must go through all steps.

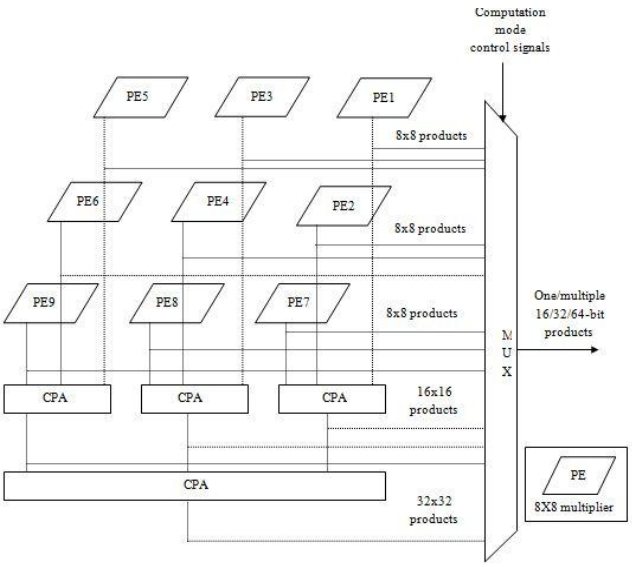

Fig 2. Possible Configuration Modes of MP Multiplier

II. DYNAMIC VOLTAGE MANAGEMENT UNIT

In this implementation DVS unit shows a dynamic power supply and a VCO are employed to achieve real-time dynamic voltage and scaling can be achieved when using voltage dithering, which exhibits faster response time than conventional voltage regulator. Voltage dithering uses power switches to connect different supply voltage to the load, depending on the time slots. Therefore, an intermediate average voltage is achieved.

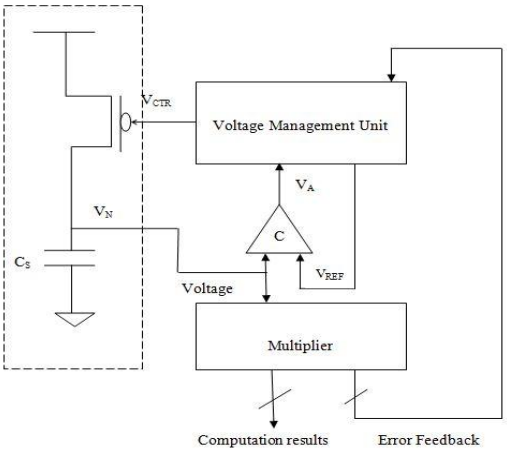

Fig 3. DVS using single switch

III. RAZOR FLIP-FLOP

Although the worst case paths are very rarely exercised, traditional DVS approaches still maintain relatively large safety margins to ensure reliable circuit operation, result in excessive power dissipated. The razor technology is breakthrough work, which eliminates the safety margin by achieving variable tolerance through in-situ error detection and correction ability. This approach is based on a razor flip-flops, which detects and correct the delay error by double sampling.

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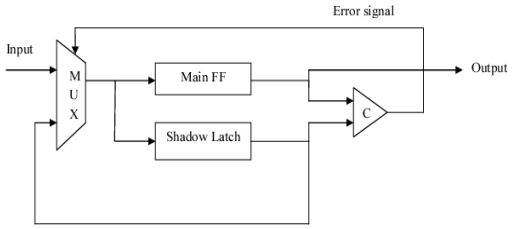

Fig 4. Razor flip-flop

The razor flip-flops are constructed out of a standard positive Edge triggered flip-flops (DFF) augmented with a shadow latch which samples at the negative clock edge. Thus, the input data is given additional time, equal to the duration of the positive clock phase, to settle down to its correct state before being sampled by the shadow latch. In order to ensure the shadow latch always capture the correct data, the minimum allowable supply voltage needs to be constrained during design time such that step-up time at the shadow latch. A comparator flags a timing error when it detects a discrepancy between the speculative sampled at the main flip-flops and the correct data sampled at the shadow latch.

IV. MODIFIED BOOTH MULTIPLIER

Booth multiplication is a technique that allows for smaller, faster multiplication circuits, by recoding the numbers that are multiplied. It is possible to reduce the number of partial products by half, by using the technique of radix-4 Booth recoding. The basic idea is that, instead of shifting and adding for every column of the multiplier term and multiplying by 1 or 0, we only take every second column, and multiply by ±1, ±2, or 0, to obtain the same results. The advantage of this method is the halving of the number of partial products. To Booth recode the multiplier term, we consider the bits in blocks of three, such that each block overlaps the previous block by one bit. Grouping starts from the LSB, and the first block only uses two bits of the multiplier. Figure 3 shows the grouping of bits from the multiplier term for use in modified booth encoding.

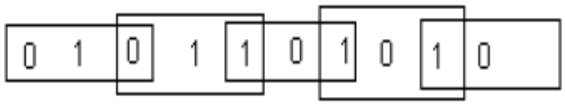

Fig.5. Grouping of bits from the multiplier term

Each block is decoded to generate the correct partial product. The encoding of the multiplier Y, using the modified booth algorithm, generates the following five signed digits, -2, -1, 0, +1, +2. Each encoded digit in the multiplier performs a certain operation on the multiplicand, X, as illustrated.

For the partial product generation, we adopt Radix-4 Modified Booth algorithm to reduce the number of partial products for roughly one half. For multiplication of 2's complement numbers, the two-bit encoding using this algorithm scans a triplet of bits. When the multiplier B is divided into groups of two bits, the algorithm is applied to this group of divided bits.

TABLE 1
MBM Operation

Block	Re - coded digit	Operation on X
000	0	0 X
001	+1	+1 X
010	+1	+1 X
011	+2	+2 X
100	-2	-2 X
101	-1	-1 X
110	-1	-1 X
111	0	0 X

A. *Multi-Precision and Reconfigurability Property*

The input interface unit of MP multiplier is shown in which forms the sub module of multiplier. Its function is to provide data to nine independent processing elements shown in fig 2 of the MP multiplier, depending on the selected operating mode. A 2-bit mode control is used to indicate whether the inputs are of 8-bit operands (1/4/9 pairs), or 16-bit operands (1/2/3 pairs) or a single 32-bit operand. This unit uses an extra MSB sign bit for signed and unsigned multiplication of incoming operands. The Processing Elements (PE) performs computation depending on the selected operating modes, that is 8-bit, 16-bit, or 32-bit operation will be performed.

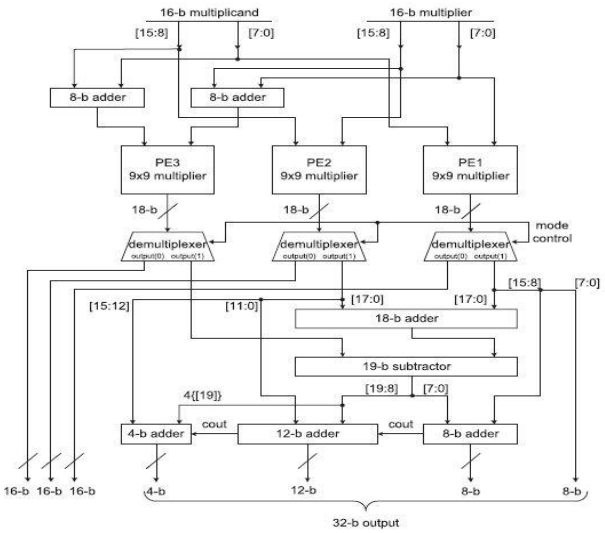

Fig 6.Three PEs combined to form 16x16 Multiplier

Figure 6 shows how 3 processing elements of 8x 8 bit can combine to form a 16 x 16 bit multiplier and perform 16-bit multiplier operation. Also 32-bit multiplier can be formed

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by similar methods but it requires 3 x3 PE of 8 x 8 bit. The 2-bit select mode signal is used as control signal which is used to determine which PEs become active and which are inactive. Based on this 2-bit signal proper precision will be selected and perform the multiplication. If complete precision (32 x32 bit) is not exercised, the corresponding supply voltage and frequency may be scaled down depending on the work load of MP multiplier.

Consider X and Y are 2n-bits wide multiplicand and multiplier; these are defined to evaluate the associated overhead to MP and configurability. X_H and Y_H are respective n MSBs and X_L and Y_L are respective n LSBs.
$X_L\ Y_L$,$X_H\ Y_L$, $X_L\ Y_H$, $X_H\ Y_H$ is corresponding cross products. This can be also represented as follows:

$$P=(\ XH\ YH)2^{2n} + (XH\ YL+\ XL\ YH)2^{n}+\ XL\ YL \qquad (1)$$

Where XLYL, XH YL, XL YH, and XH YH can be computed using 4, n x n bit multipliers, 2n bit reconfigurable multiplier can be constructed using adders. If,

$$X' = XH + XL \qquad (2)$$

$$Y' = YH + YL \qquad (3)$$

Then equation (1) will be

$$P=X_H\ Y_H\ 2^{2n} + (X_1\ Y_1 - X_H\ Y_H - X_L\ Y_L)\ 2^{n} + X_L\ Y_L \qquad (4)$$

Compare the equations (1) & (4),one n x n bit multiplier for calculation of $X_H\ Y_L$ or $X_L\ Y_H$ and one 2n bit adder for calculation of $X_H\ Y_L + X_L\ Y_H$ can be removed. Also two n-bit adders and two (2n+2)-bit subtractions are provided for calculation of $X_H + X_L$,$Y_H + Y_L$ and $X_1Y_1 - X_H\ Y_H - X_L\ Y_L$ resp. Evaluation of the Razor based MP multiplier can be done by comparing it with 32bit fixed width multiplier and four sub-block MP multipliers which are designed using Booth Radix-4 Wallace tree structure [4],[5]. This is done similar to proposed MP multiplier that consists of 3 sub-block multipliers. The power simulations are performed at clock frequency of 50 MHz and power supply voltage at 3.3v. From the evaluation, the Razor based MP 3 sub-block multiplier architecture achieved reduction in power and area compared to fixed width multiplier design. The large size of fixed width multiplier provides an irregular and complex interconnects. This causes increase in area and also additional power consumption. The MP multiplier with three sub-block architecture can achieve 16% reduction in power and 28% reduction in area as compared with the conventional 32 × 32 bit fixed-width multiplier design. This limitation of tree multipliers can be addressed by this MP 32 × 32 bit multiplier, which uses a more regular design to partition, regroup, and sum partial products. The Razor based multiplier is easy to implement and more suitable for DSP applications.

V. COMPARISION OF TWO MULTIPLIERS

This shows that the conventional MP multiplier occupies the area almost 52 times more than that of Razor based modified booth multiplier. So the power required for conventional MP multiplier will also be more than that of Razor based modified booth multiplier since the number of partial products are reduced in the Razor based modified booth multiplier.

Table II
Comparison of MP Array multiplier and MP Booth multiplier

Logic Utilization	Razor Based Array Multiplier	Razor Based MBM Multiplier
Number of slices	330	69
Number of slice flip flops	207	79
Number of 4 input LUTs	586	126

VI. CONCLUSION

The proposed novel MP Razor based multiplier featuring with variable precision and parallel processing provides the multiplication up to 32-bit without much area and power consumption than the any other fixed width multiplier. This architecture replaced the razor flip-flop and VSU and thus reduced area and power consumption with considerable amount. The MP multiplier benefits from operands scheduler that re-arranges the input to reduce the number of transitions of the supply voltage and thus minimized the overall power consumption of the multiplier. Finally, MP multiplier based on Razor and DVM provided a solution to achieve reduced area.

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