Design and Synthesis of AXI Slave Interface Memory Controller

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Abstract – The Advanced Extensible interface (AXI) memory controller is developed for the efficient communication between the IP (Intellectual Property) blocks and external memory comprising system-on-chips(SOC).An important feature of the AXI4 protocol supports high performance, high frequency system designs. It is suitable for high bandwidth and low latency designs and provides high frequency operation without using complex bridges. Now a days the speed of fetching data from memories is unable to match the speed of processors in the view of this issue an AXI4 interfacing memory controller is designed to increase the memory efficiency. In the subject paper, Advanced Extensible slave interface memory controller is designed in verilog and verified using Synopsys VCS tools.

Keywords – Advanced Extensible Interface (AXI), FIFO (First-in-First-out), memory controller (MC), system-on-chips (SOCs).

I. INTRODUCTION

A system-on-a-chip (SOC) consists of large number of intellectual property(IP) blocks a microchip with all the necessary electronic circuits and parts for a given system, such as Smartphone or wearable computer, on a single integrated circuit (IC). An SoC for a sound-detecting device, for example, might include an audio receiver, an analog-to-digital converter
(ADC),a microprocessor, memory,andthe input/ output logic control for a user - all on a single chip.

System-on-a-chip technology is used in small, increasingly complex consumer electronic

devices. Some such devices have more processing power and memory than a typical 10 year old desktop computer. In the future, SOC-equipped nanorobots might act as programmable antibodies to fend off previously incurable diseases. SOC video devices might be embedded in the brains of blind people, allowing them to see and SOC audio devices might allow deaf people to hear. Handheld computers with small whip antennas might someday be capable of browsing the Internet at megabit-per-second speeds from any point on the surface of the earth.SOC is evolving along with other technologies such as silicon-on-insulator (SOI), which can provide increased clock speeds while reducing the power consumed by a microchip.

II. ADVANCED MICROCONTROLLER BUS ARCHITECTURE (AMBA)

The first AMBA buses were Advanced System Bus (ASB) and Advanced Peripheral Bus (APB). In its second version, AMBA2, ARM added AMBA High-performance Bus (AHB) that is a single clock-edge protocol . In 2003, ARM introduced the third generation, AMBA 3 , including AXI to reach even higher performance interconnects and the Advanced Trace Bus (ATB) as part of the Core Sight on chip debugs and trace solution. In 2010 the AMBA 4 specifications were introduced starting with AMBA 4 AXI4, then in 2011 extending system wide coherency with AMBA 4 ACE with a re-designed high-speed transport layer and features designed to reduce congestion . Advanced microcontroller bus

architecture (AMBA) protocol family provides metric-driven verification of protocol compliance, enabling comprehensive testing of interface intellectual property (IP) blocks and system-on chip (SoC) designs. The AMBA advanced extensible interface 4 (AXI4) update to AMBA AXI3 includes the following: support for burst lengths up to 256 beats, updated write response requirements, removal of locked transactions and AXI4 also includes information on the interoperability of components. AMBA AXI4 protocol system supports 16 masters and 16 slaves interfacing.

The performance of microprocessors has been improving rapidly over the years. In contrast, the memory latencies and bandwidths have progressed relatively little. As a consequence, the memory access has been a real bottleneck in the context of improving the system performance. The External Memory controller should be efficiently combined with the interconnections. The Memory controller is designed as a master that operates on different protocols and interacts with the memory by sending or receiving data with the help of its slave. The biggest challenge in an SOC design is the integration of processors and memory modules. An increasing numbers of companies have adopted the advanced microcontroller bus architecture (AMBA) system, which has rapidly evolved as the de facto standard for the SOC interconnections and IP library development. The AMBA enhances a reusable design methodology by defining a common backbone for the SOC modules . Figure 1 shows the AXI interconnect.

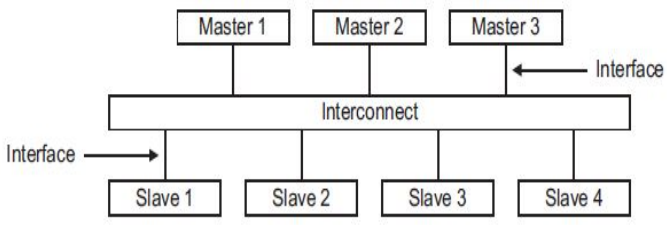

Figure1: AXI interconnect with interfaces

The AMBA-AXI does not require any bridge like AMBA-AHB. This AMBA-AXI compliant memory controller can be used with the latest ARM processors as well. This memory controller is mainly designed for interfacing the memories like SRAM and ROM and matches well with the memory latencies. Here the Memory controller is designed to improve the system performance. As the Memory Controller is On-chip, the memory accessing time is decreased so that performance is increased.

III. ARCHITECTURE OF AMBA AXI MEMORY CONTROLLER (MC)

The AMBA-AXI memory controller is mainly divided into three parts like: AXI Slave interface, FIFO, External Memory Interface. Figure 2 shows the architecture of AXI-MC.

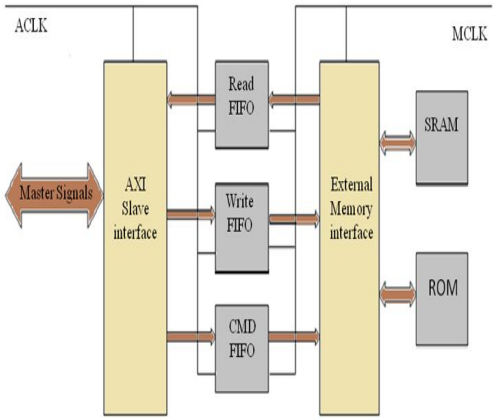

Figure 2 : AXI Slave interface Memory controller

A. AXI Slave Interface

The AXI Slave interface plays a vital role in AXI Memory controller. It is used for converting the incoming AXI transfers to the protocol used by the AXI. In AHB, there are no control signals like valid, Awready etc. In AXI Slave Interface there are various control signals like Awready, Awid, and Awresp etc. As AXI is full duplex, read and write can be performed at a time that is due to channels like :

a. Write Channel-Address, data, Response

b. Read channel-Address, Response and Data.

Here 2 clocks are used Hclk and Mclk. As AXI slave interface operates at high frequency clock and external memory interface operates at low frequency clock. To get the synchronization between two clocks FIFO is used.

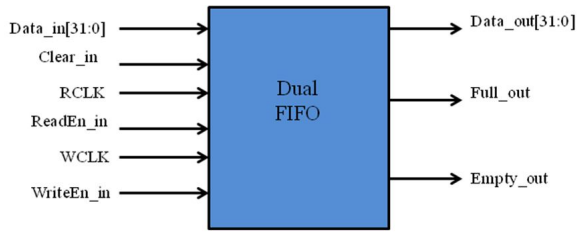

Figure 4: Dual FIFO

B. External Memory Interface

When clock signals arrive, the depending upon the instruction, its operation is decided on by command (CMD) control state. Based on the instruction, it moves to RAM read, RAM write and ROM read operations.

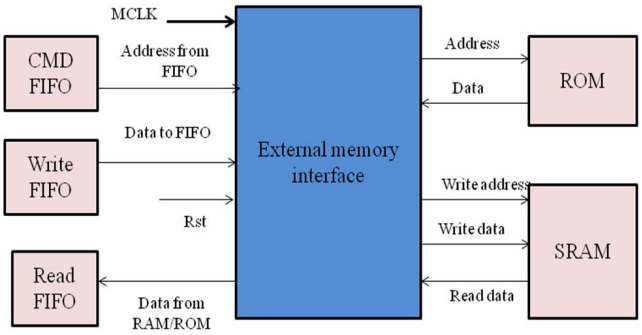

Figure 3: Block diagram of External Memory interface

C. First-In First-Out (FIFO)

The FIFO is a method of processing and retrieving data. In a FIFO system, the first items entered are the first ones to be removed. In Figure three signals are shown data, FIFO full and FIFO empty. The FIFO full and FIFO empty are known as handshaking signals, which allow the source and sink to communicate when it is time to pass the data. The FIFO full signal indicates that the FIFO is full and puts valid data on the data line. FIFO full is what is called a state signal – it is high only when data are valid. If data are not valid on the data line during a particular cycle, valid should be low during that cycle.

IV. SIMULATION RESULTS

The simulation results of the AXI-MC operations: signals high or low, depending on the read or write control signals are shown in Figure 5. There are three outputs: read-write latency , read address and write data.The read or write operations are forwarded to the Memory Controller by the slave interface.the design optimised latency of 300ns.

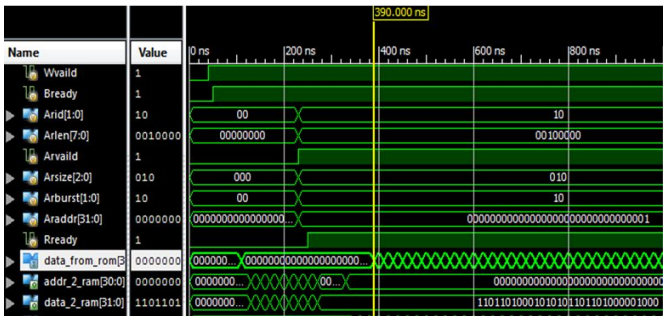

Figure 5: AXI Read-Write Latency

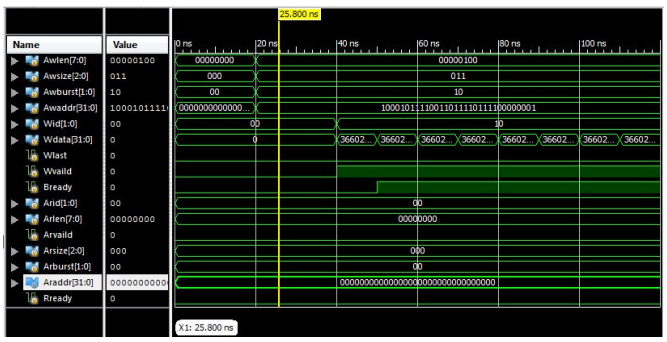

Figure 6: AXI Memory controller Write operation

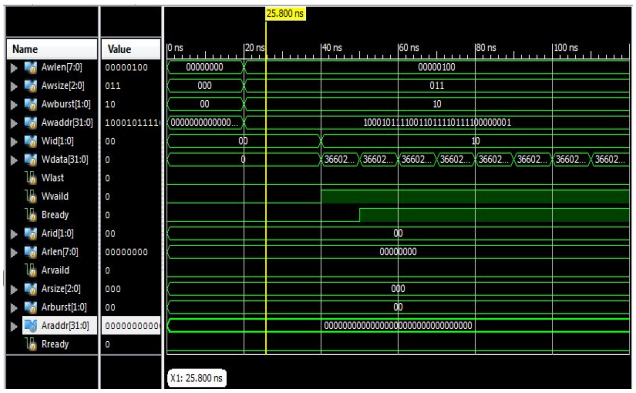

Figure 7: AXI Memoery Controller Read operation

V. SYNTHESIS RESULTS

The process of transferring RTL design to gate-level netlist is called synthesis.The RTL design is synthesized using Synopsys DC compiler tool.

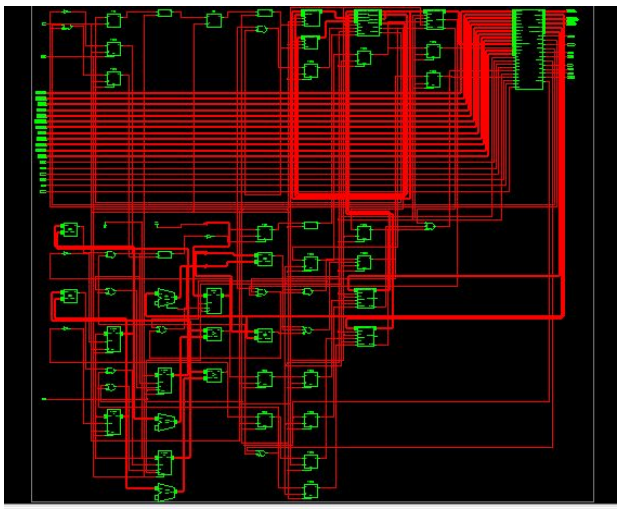

Figure 8: AXI Synthesized result

VI. CONCLUSION

The Advanced Extensible interface memory controller is designed and improves the performance and it removes the bridges like in AHB bus architecture. This decreases the latency and increases throughput it makes design simple and free of bottleneck. The design was obtained a frequency of 295MHZ.

VII. FUTURE SCOPE

Future improvements in the Advanced Extensible interface memory controller designed with more features like QOS (Quality of Service) specification recommends that AxQOS is used as a priority indicator for the associated write or read transaction. Write strobes specification WSTRB[n:0] signals when HIGH, specify the byte lanes of the data bus that contain valid information.

VIII . ACKNOWLEDGMENT

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IX. REFERENCES

[1] Shashisekhar RamagundamVoicu Groza, Sunil R.Das, Mansour H. Assaf, Scott Morton, Satyendra N. Biswas, and Emil M. Petriu ,proceedings of the IEEE Design and Implementation of High-PerformanceMaster/Slave Memory Controller with Microcontroller Bus Architecture

[2] Y. Hu and B. Yang, “Building an AMBA AHB compliant memory controller”, Proceedings of the Third International Conference on Measuring Technology and Mechatronics Automation , Vol. 01, 2011, pp. 658–661.

[3] S. Rao and A. S. Phadke, “Implementation of AMBA compliant memory controller on a FPGA”, International Journal of Emerging Trends in Electrical and Electronics, Vol. 2, April 2013, pp. 20–23.

[4] AMBA Specification (Rev 2.0), ARM Inc., 1999.

[5] AMBA® AXI Protocol, v1.0 Specification, ARM IHI 0022B, 2003.

