Power Analysis for CMOS based Dual Mode Logic Gates using Power Gating Techniques

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Abstract*:* Low power technology was major consideration in present generation circuits. In order to achieve low power Sub-threshold circuit design is one of the leading methods for low power to ultra-low power applications. The Dual Mode logic gates are designed to operate in the sub threshold region. In this paper we discuss about the design of the dual mode logic gates with which we designed different styles of design of dual mode logic using various Power gating Techniques. This paper proposes to design the dual mode logic gate for inverter and NAND using Power Gating techniques. These circuits are designed and they are simulated with the Tanner Tools13.0 with TSMC0.18 Technology.

Introduction:

In the present generation, the major concerns of the VLSI designer was the power consideration were area, performance, cost and reliability was mostly became secondary importance. In present years, however, this has begun to change and, power is being given comparable weight to area and speed considerations. Several factors have obtained to this trend. Infect the primary driving factor has been the remarkable success and growth of the class of portable devices (desktops, audio-video devices) and wireless communications systems (personal digital assistants and personal communicators) which demand high-speed computation and complex functionality with low power consumption.

Sources of Power Dissipation:

Power Dissipation majorly occurs due to the two factors called dynamic losses and static losses. These dynamic losses are occurred due to the increasing operating frequency of the devices. These losses occur due to switching activity of the transistors. Static losses not depend upon the frequency of operation it depends on the technology with which the scaling of transistors are designed with high scaling factor has high static losses.

In order to operate the circuit at low power consumption sub threshold plays a major role. Circuits which operate in the sub-threshold region use a supply voltage that is close to or less than the threshold voltages of the transistors, so that there is a significant reduction in both dynamic and static power consumption. The low-power dual mode logic (DML) family is a logic family designed to operate in the sub-threshold region. The proposed logic family can be switched between static and dynamic modes of operation according to system requirements. The ability of DML circuits to operate in both the static and dynamic modes gives the opportunity to create efficient logic circuits which balance power consumption and operating frequency (speed of the circuit) requirements. In the static mode of operation, the dual mode logic gates has very low-power dissipation with moderate performance, and in the dynamic mode of operation they have higher performance, at the price of increased power dissipation.

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Existing Logic Families

Dual Mode Logic gates:

These approaches utilize low supply voltages for digital circuit operation, decreasing the dynamic power quadratic ally and sufficiently reducing leakage currents; albeit, at the expense of loss in performance. The DML family, which is fully compatible with any standard logic process, was demonstrated to be fully functional at all operational regions, and up to nominal supply voltages
.
The basic DML emerges from the both static and dynamic logic gates. DML gets acts as both as static gates and as dynamic gates. An additional footer /header transistor (connected in series to an evaluation path) is optional to ensure a correct interface with other gates.

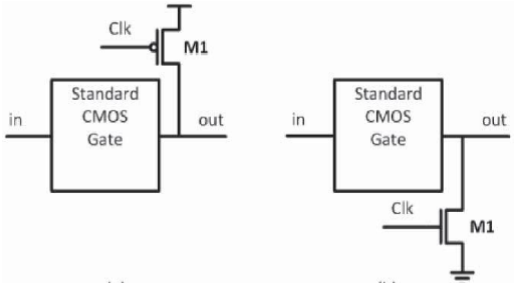

Figure 1: Type- A and Type –B of DML Logics

The clk is fed with an asymmetric clock, in dynamic mode operation, clk allows two distinct operations one dynamic phase and static phase. The output is charged to high/low. Based on the DML topology of the gate, the output is charged to high/low throughout the pre charge phase. The output is analyzed and evaluated based on the values obtained at the gate inputs during evaluation phase of operation.
Here two DML topologies are shown. Type A and Type B logics as shown in above figure.

Type A is characterized by an addition of p-MOS transistor connected to output and the VDD, on pre charge phase, the PMOS will be in ON state and pre charges the output to a logical "1".
Implementation of dynamic logic gates makes use of a footer, which needs an extra transistor than the DML gates. During the evolution phase i.e., clk=1 it acts like normal static CMOS gate.

Type B DML gate was designed by adding additional transistor to output and the ground during the pre-charge phase i.e., clk=1 the output was pre-charged to the logic "0" and during the evolution phase clk= 0 its acts like normal static gate.

DML nodes which operate in dynamic mode possess many merits over traditional dynamic nodes which inherited from DML topology. It has distinct potential to shift between various operations modes. The DML genetically characterizes an active keeper made from the CMOS complementary logic. It is acquired from the node structure which consists of fully functional CMOS part, and also supports in retaining the output level. This vital constraint to the immunity to temperature fluctuations, process variations and resolving domino's popular disadvantages such as crosstalk noise, charge sharing and susceptibility to glitches, which escalates with voltage and process scaling.

Footed A is similar to the Type A logic design but here we adds a additional NMOS transistor in series to the NMOS logic. NMOS logic was grounded by using this additional nmos with clk signal. During Pre-charge phase PMOS will be in the ON state and pre-charges the output node at the same time NMOS will be in OFF state which will disconnects the ground from circuit in-order to reduce the static loss in pre-charge node.

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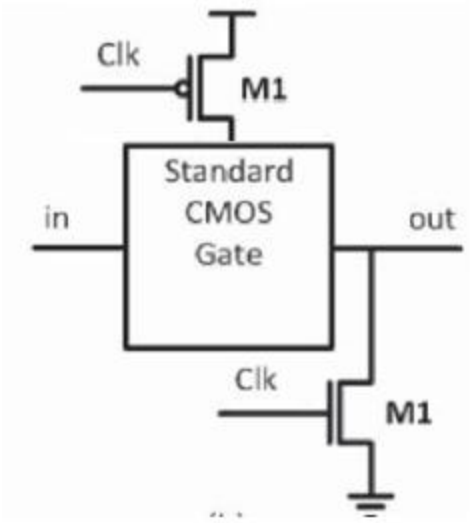

Figure 2: Standard CMOS logic

Footed B is similar to the Type B logic design but here an additional PMOS transistor is added in series to the PMOS logic. PMOS logic was connected to VDD by using this additional PMOS with clk signal. During Pre-charge phase NMOS will be in the ON state and pre-charges the output node at the same time PMOS will be in OFF state which will disconnects the VDD from circuit in-order to reduce the static loss in pre-charge node.

Existing System Disadvantages:

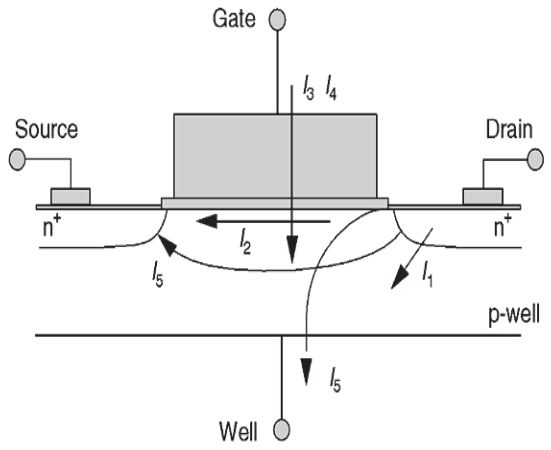

Figure 3: Leakage Currents.

Here I2, I5, I6 are off state leakage currents which consumes more power.

To eradicate these Problems We implement Power Gating Techniques which reduces Power in off state and improves Performance.

Proposed System:

To reduce power in circuits two power gating techniques, namely Sleep and Stack Sleep technique are implemented and the results of best technique are observed.

1. **Sleep Technique**:

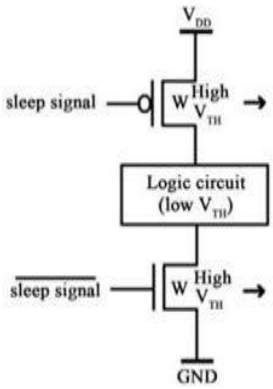

Figure 4: Sleep Technique

- This technique uses the sleep transistor between both VDD and the pull up network and between GND and pull down network.

2. **Stack Sleep Technique**

- The forced stack and the sleep transistor techniques are combined to get the sleepy stack structure.

- The function of sleep transistors in sleepy stack is same as of the sleep transistor in sleep transistor technique

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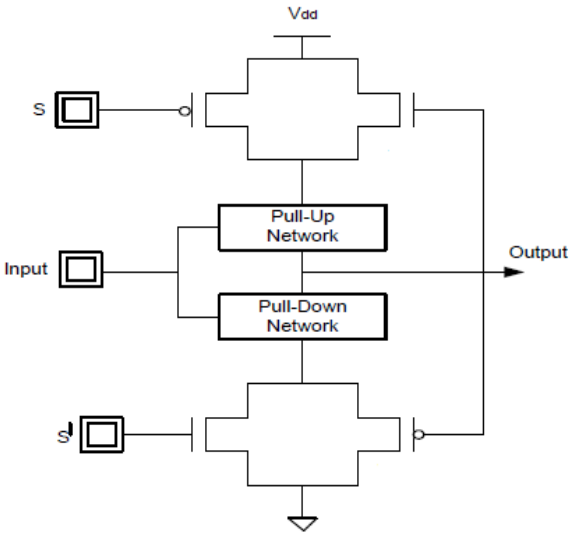

Figure 5:Stack Sleep Technique

Simulation and Results:

These circuits are designed and simulated using the Tanner Tools.

The DML logic style along with power gating techniques is applied on various gates and their power dissipations are compared in the below table

Type A:

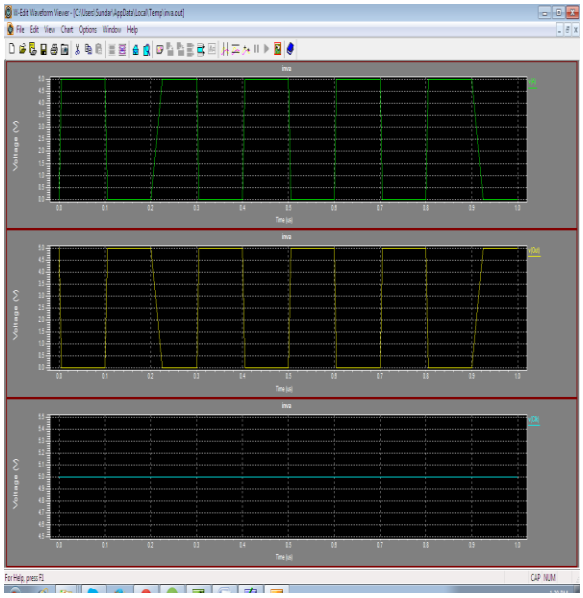

Figure 6: waveform for inverter Type A

Sleep Technique:

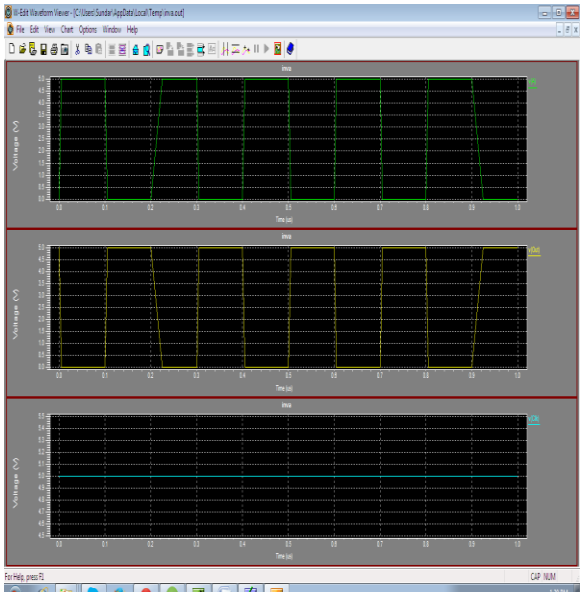

Figure 7: Waveform for Sleep Technique.

Sleep Stack Technique:

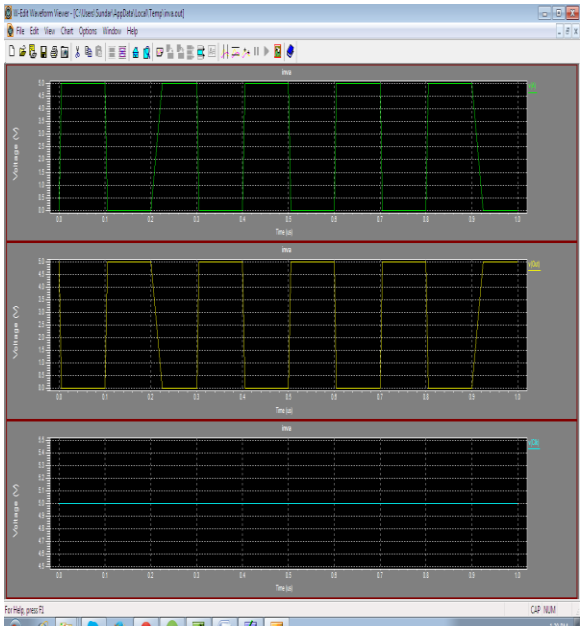

Figure8: waveform for Sleep Stack Technique

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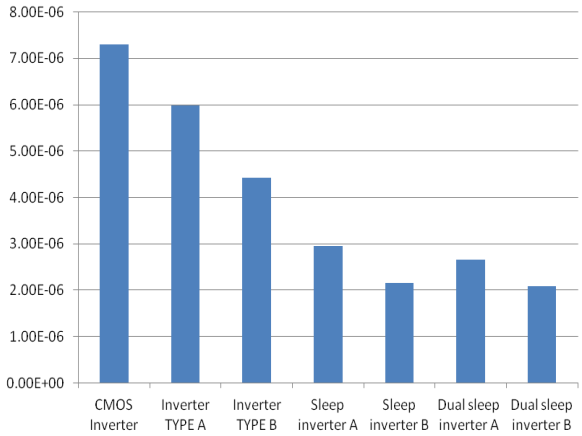
The values of power dissipation for inverter are noted and graphical representation is given

Table1:power value for Inverter

Inverter	Power consumption
CMOS Inverter	7.30e-006 watts
Inverter TYPE A	5.98e-006 watts
Inverter TYPE B	4.41e-006 watts
Sleep inverter A	2.95e-006 watts
Sleep inverter B	2.16e-006 watts
Dual sleep inverter A	2.65e-006 watts
Dual sleep inverter B	2.08e-006 watts

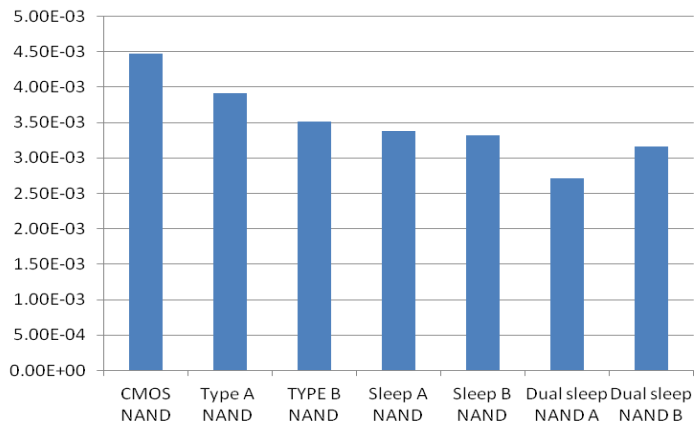


Observation: Here for inverter dual sleep technique is best among the compared techniques.

The values of power dissipation are noted in the same way for NAND gate and graphical representation is taken

Table 2:Power value for NAND

Nand gate	**Power consumption**
CMOS NAND	4.47e-03
Type A NAND	3.91e-03
TYPE B NAND	3.51e-03
Sleep A NAND	3.38e-03
Sleep B NAND	3.32e-03
Dual sleep NAND A	2.72e-03
Dual sleep NAND B	3.17e-03



Observation: Here for the NAND gate dual sleep type A is best among the techniques.

Conclusion:

The novel Dual Mode Logic (DML) family of logic gates along with power gating techniques was considered as an energy efficient alternative to standard CMOS logic. On the fly tradeoff between High performance of dynamic mode and energy efficiency of static mode is enabled using DML and its following design

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methodologies. The various techniques are implemented and best among them is observed.

Future Scope:
In the future the same techniques can be applied to complex circuits and sequential circuits and can also to the memory elements.

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References:
[1]Itamar Levi, Alexander Belenky, Alenxader Fish, Logical Effort for CMOS Based Dual Mode Logic Gates , IEEE Transactions On Very Large Scale Integration(vol-22), May 2014.

[2] Itamar Levi, Ori Bass, Asaf Kaizerman, Alexander Belenky , High Speed Dual Mode Logic Carry Look Ahead Adder , IEEE Trans. Very Large Scale Integration, May 2012.

[3] Levi, A. Kaizerman, and A. Fish, "Low voltage dual mode logic: Model analysis and parameter extraction," Excepted Elsevier, Micro electron. J., vol. 12, no. 1, Jan. 2012.

[4]A. Kaizerman, S. Fisher, and A. Fish, "Sub threshold dual mode logic," IEEE Trans. Very Large Scale Integration. (VLSI) Syst., vol. 21, no. 5, pp. 979–983, May 2013.

[5]M. Alioto, "Ultra low power VLSI circuit design demystified and explained: A tutorial," *IEEE Trans. Circuits Syst. I*, vol. 59, no. 1, pp.3–29, Jan. 2012

[6] W.M.Pensey and L. Lau, *MOS Integrated Circuits*. New York: Van No strand, 1972, pp. 260–282.

[7] B. Zhai, S. Hanson, D. Blaauw, and D. Sylvester, "Analysis and mitigation of variability in sub threshold design," in *Proc. Int. Symp.Low Power Electron. Design*, Aug. 2005, pp. 20–25

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