Design of Programmable Arbiter based On-Chip Permutation Network for Multiprocessor System-On-Chip

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Abstract:In this paper the design of a network on chip to support a guaranteed throughput is explained. The clos network topology is used with the three stages of switches of 4ports of inputs and outputs. This network is designed to support a guaranteed traffic permutation in multiprocessor system-on-chip applications. The network employs a pipelined circuit-switching approach combined with a dynamic path-setup scheme enables runtime path arrangement for arbitrary traffic permutations. Network on chip (NoC) is a communication subsystem on integrated circuit, typically between IP cores in a system on a chip (SoC). NoCs are an attempt to scale down the concepts of large scale networks, and apply them to the embedded system on chip domain. The fundamental unit of building a network on chip is the router, it directs the packets according to a routing algorithm to the desired host. In Programmable Arbiter based priority logic contains F-Priority, RR-Priority, D-Priority logics. This circuit-switching approach offers a guarantee of permuted data and its compact overhead enables the benefit of stacking multiple networks. The Programmable Arbiter improves the delay efficiency and improves the data efficiency.

***Index Terms*—backtracking, circuit-switched, dynamic Path-setup, guaranteed throughput, network-on-chip (NoC), on-chip switch, source synchronous, wave-pipeline.**

INTRODUCTION

Multiprocessor systems-on-chips (MPSoCs) have emerged in the past decade as an important class of very large scale integration (VLSI) systems. An MPSoC is a system on-chip a VLSI system that incorporates most or all the components necessary for an application that uses multiple programmable processors as system components. MPSoCs are widely used in networking, communications, signal processing, and multimedia among other applications.A trend of multiprocessor system-on-chip (MPSoC) design being interconnected with on-chip networks is currently emerging for applications of parallel processing, scientific computing, and so on. New architectures are and must be continuously conceived. It is clear now that Moore's law for the last two decades has enabled three main revolutions.

The first revolution in the mid-eighties was the way to embed more and more electronic devices in the same silicon die; it was the era of System on Chip. One main challenge was the way to interconnect all these devices efficiently. For this purpose, the Bus interconnect structure was used for long time. Anyway, in the mid-nineties the industrial and academic communities faced a new challenge when the number of processing cores became two numerous for sharing a single communication medium.

In Multistage switching network, Permutation traffic, a traffic pattern in which each input sends traffic to exactly one output and each output receives traffic from exactly one input, is one of the important traffic classes exhibited from on-chip multiprocessing applications. Standard permutations of traffic occur in general-purpose. In addition, many of the MPSoC applications compute in real-time, therefore, guaranteeing throughput (i.e., data lossless, predictable latency, guaranteed bandwidth, and in-order delivery) is critical for such permutation traffics.

Most on-chip networks in practice are general-purpose and use routing algorithms such as dimension-ordered routing and minimal adaptive routing. To support permutation traffic patterns, on-chip permutation networks using application-aware routings are needed to achieve better performance compared to the general-purpose networks. These application-aware routings are configured before running the applications and can be implemented as source routing or distributed routing.

ISSN: 2278 – 7798

To overcome the drawback of packet switching and fixed arbitrary scheme for arbiter in switch circuit, a new design is proposed with configurable and programmable Arbiter for runtime traffic permutation. The main drawback previous system is with the Arbitration schemes. To overcome these problems we are using run time programmable arbiter in each switch. The Arbiter is programmed with new Arbitration schemes by overcoming drawbacks of previous schemes. The efficiency is improved. The proposed system re-routes data on erroneous links to a set of spare wires without interrupting the data flow. The main advantage of Circuit Switching is manual establishment of dedicated channel, with a fixed delay for data transaction.

PROPOSED ON-CHIP NETWORK DESIGN

The design of multistage switching on chip network topology with pipelined circuit switching with dynamic path, the dynamic path-setup scheme enables runtime path arrangement for arbitrary traffic permutations. The circuit-switching approach offers a guarantee of permuted data. The proposed design involves configuration and programming of Arbiter in switch circuit.

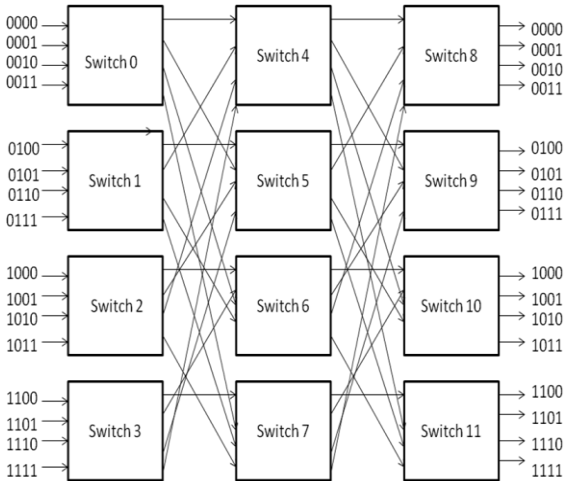


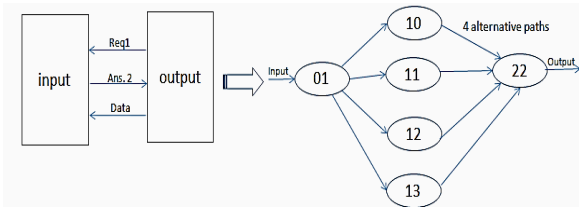
Fig. 1. Proposed on-chip network topology with port addressing scheme.

On-Chip Network Topology

Clos network, a family of multistage networks, is applied to build scalable commercial multiprocessors with thousands of nodes in macro systems. A typical three-stage Clos network is defined as *c(n,m,p)*, where n represents the number of inputs in each of p first-stage switches and m is the number of second-stage switches. Inorder to support a parallelism degree of 16 as in most practical MPSoCs, we proposed to use*c(n,m,p)* as a topology for the designednetwork (see Fig. 1). This network has a rearrange able property that can realize all possible permutations between its input and outputs.The choice of the three-stage Clos network with a modest number ofmiddle-stage switches is to minimize implementation cost, whereas itstill enables a rearrange able property for the network.

A pipelined circuit-switching scheme is designed for use with the proposed network. This scheme has three phases: the setup, the transfer, and the release. A dynamic path-setup scheme supporting the runtime path arrangement occurs in the setup phase. In order to support this circuit-switching scheme, a switch-by-switch interconnection with its handshake signals is proposed, as shown in figure 2.

Figure 2: Switch-by-switch interconnection and path-diversity capacity



Each switch has four bidirectional ports: four ports are connected to corresponding neighboring switches, and the remaining port is connected to the on-chip IP through a wrapper.According to this handshake scheme, one bit is used for the Request (Req.) signal to denote the on-probing state (circuit request) and the circuit idling state. Two bits are used for the Answer (Ans.) signal. This has one of three statuses to direct the backpressure flow-control to upstream switch. An Ans. status of "01" denotes that the receiver is ready to accept data from the sender, whereas a status of "10" denotes that the intended path is blocked in the network, forcing the probe header to backtrack to discover possible alternative paths. An Ans. status of "11" denotes that the receiver is not ready to receive data (e.g., due to being busy, or having an overflow at the receiving buffer).

Request signals: (req.) 1-bit length. If req=1 (Data transfer along setup path). If req=0 (switch releases the occupied link).

ISSN: 2278 – 7798

Answer signals: (Ans.) 2 bit length. If Ans =01 Acknowledgement (Ack) – Destination is ready to receive data from source. Ans =11 negative Acknowledgement (nAck) – Reserved for end-to- end flow control. Ans =10 (Back) – Link is blocked. Ans =00 (Ideal).

COMMON SWITCH ARCHITECTURE AND PROGRAMMABLE ARBITER

The proposed switch architecture has the following main components that can be divided into two function groups. The data path includes CROSBAR with internal transceivers to support a direct-forwarding (wave-pipelining) of the source-synchronous data. The control part includes IC's, OC's, and ARBITER. Each pair of Ctrl In and Ctrl Out performs handshaking activity.

The IC's are in charge of processing the incoming probe headers from upstream switches. When an incoming probe header arrives at an input (with Req= "1"), the corresponding IC's monitors the output status through Monitor bus and requests ARBITER to grant it access to the desired OC's through the internal Request bus. Based on output status or the feedback from ARBITER placed in Grant & Answer bus, the IC's operates appropriately and replies to the upstream switch through its Ans_In.

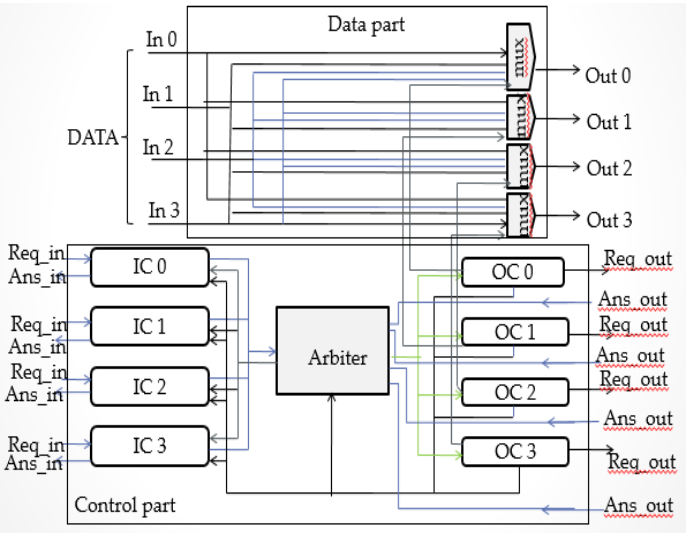


Figure 3: Common Switch Architecture

The ARBITER has two roles:

First, for cross-connecting Ans_Out signals back to IC's, and second, as a referee for requests from IC. If a requesting IC is accepted, the first role of ARBITER keeps Ans _signal from the requested Ans_Out being connected back to the requesting IC through the Grant & Answer bus. By this way, in case of backtracking, the ARBITER can direct the probe header to backtrack to the corresponding input from which it arrived (reserved) previously. Contention resolution is required when several IC's, upon observing the Monitor bus, request the same idling output in the same probing clock cycle.

The second role of ARBITER (based on a static priority rule) allows only one request to be accepted, while the remainders are answered with "Network Blocked". By receiving this answer, the requesting IC's continues probing other outputs or returns a "Busy Dest." to its corresponding upstream switch, depending on which probed port is the direction port. The OC's, based on the command from the ARBITER placed in the Control bus, make requests to the downstream switches and control the CROSSBAR. When locked with a specific selecting value, the OC's handles the CROSSBAR to establish a direct connection from the Data In to the target Data out.

Programmable Arbitration schemes:

In the previous design of the switching circuit consists of Arbiter as shown in above figure, can be programmed and configurable with different arbitration schemes to overcome drawback in the previous system with arbitration schemes, new design has proposed with new arbitration scheme for better efficiency. i. Round Robin ii. Fixed Priority.

In proposed Dynamic Priority scheme, all tasks or devices will get access those who put request for grant to communicate with other device. By overcoming drawbacks of above two schemes, means inefficiency in round robin, starvation problem in fixed priority, and this scheme provides better results so that the efficiency is increased.

For example, if four devices are trying for accessing or communicate with other device. All devices has kept request for grant. we first initially assign priorities. Initially the highest priority device gets access. What about other devices? Now the highest priority will get decreased by one value in next clock cycle or after getting first access. This process will continue until to the next highest priority value. Now the second highest priority device will get

ISSN: 2278 – 7798

access. This process will continue to the next highest priority value and so on. In this all the devices will get access those devices put request for grant. So all the drawbacks are overcome and efficiency is increased.

BACK TRACK PROBING PATH-SETUP SCHEME

The path-setup scheme is essential and directly affects the overall performance of the circuit-switching approach. An analysis at the network-level, performed in previous work, confirmed the good performance of the backtracked routing circuit-switched NoC with the clos topology under certain communication patterns. In particular, in communications with larger packets, the data transmission duration can be long. This overwhelms the setup delay overhead, hence, improving the overall network performance.

SIMULATION RESULTS

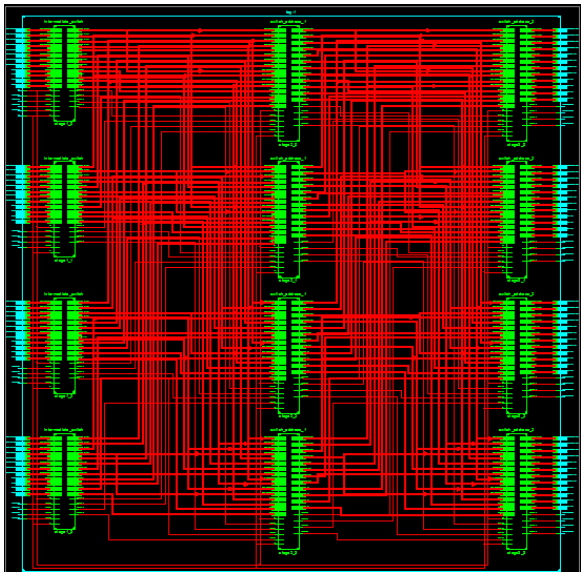


Figure 4: Top module 3 stage switching circuit

The arbiter has the inputs of master_number (1:0), Priority_scheme(1:0), priority_value(3:0), request_vector(3:0), clk and reset signals of one bit each and it has one ouput signal as grant(3:0).

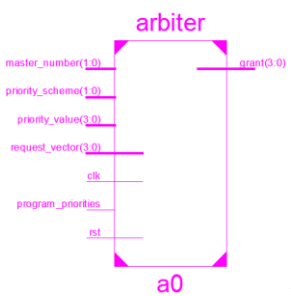
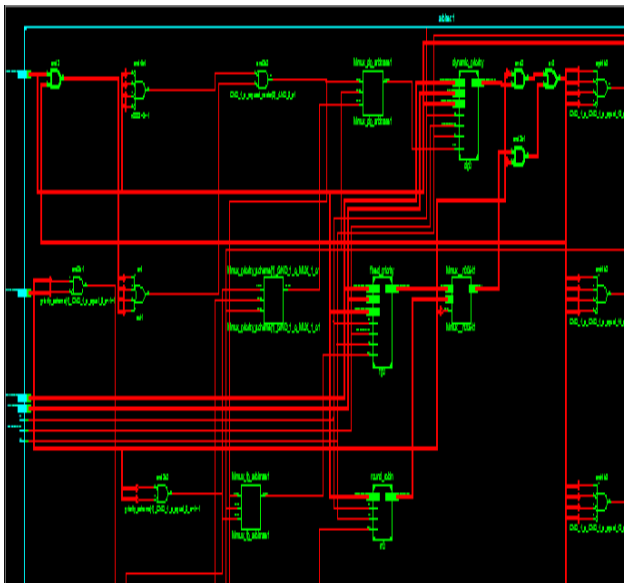


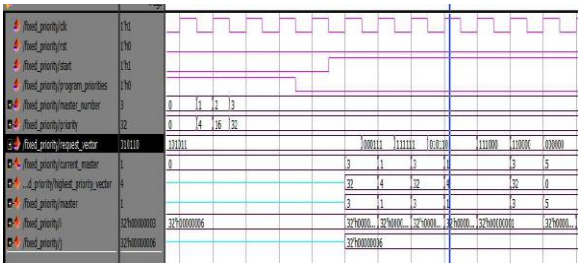
Figure 5: Top level schematic of Arbiter

The following figure 6 shows the internal schematic representation of arbiter with full routing connection with the other 3 arbitration schemes.

Figure 6: Internal RTL schematic of Arbiter with 3 schemes.



The Dynamic Priority is one the arbitration schemes which has the inputs master_number(1:0), Priority(3:0), request_vector(3:0),program priorities, clk and reset signals of one bit each and it has one ouput signal as current_master(3:0).



Simulation waveform is shown is for the example Which has master(4:0) and it has 4 high request signals for all inputs, it performs in the following manner.

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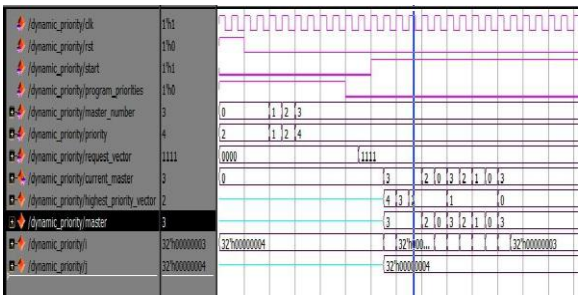

Figure 7:Simulation results for Dynamic Priority

The Round Robin scheme has request_vectors (3:0), start ,clk and reset signals of one bit each and it has one output as Current _master (3:0).

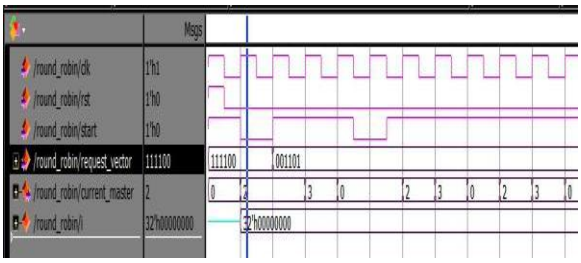

Figure 8: Simulation results for Round Robin

In this Round Robin technique all the devices will be given equal priorities. The request vector is 1111 so all the devices D0, D2, D3 and D4 will get the access in round fashion.

The Fixed Priority arbitration scheme has mainly master_number(1:0), priority(3:0),request vector(3:0) and program priorities ,clk, rst, and start signals of one bit each and current_master (3:0) as the output.

The simulations results for fixed priority are shown in figure 9. In Fixed priority only the device with highest priority will get the access. In the above figure device D3 having the highest priority will get the access.

Figure 9: Simulation results for fixed priority.

CONCLUSION

On-Chip network designed supporting traffic permutations in MPSoC applications. By using a circuit-switching approach combined with dynamic path-setup scheme under a Clos network topology, the proposed design offers arbitrary traffic permutation in runtime with compact implementation overhead. By using Circuit Switching technique we can have a dedicated path delay from source Node to Destination Node. Link once established is serviced till all amount transactions is carried out. EPB: Exhaustive profitable Backtracking is the routing technique used in setting up the link for data communication. Dynamic path setup plays a major role in probing, for setting link.

ACKNOWLEDGEMENT

I highly indebted to Dr. P Vinay Kumar, Assistant Professor in JNTU Kakinada for guiding me as well as for providing necessary information regarding the project and also support in completing project.

REFERANCES

[1] Phi-Hung Pham, Junyoung Song, Jongsun Park, and Chulwoo Kim, "Design and Implementation of an On Chip Permutation Network for Multiprocessor System-On-Chip," *IEEE Transactions On Very Large Scale Integration (VLSI) Systems, Vol. 21, No. 1, Jan. 2013, pp. 173-177.*

[2] Phi-Hung Pham, Jongsun Park, Phuong Mau, and Chulwoo Kim, "Design and Implementation of Backtracking Wave-Pipeline Switch to Support Guaranteed Throughput in Network-on-Chip," *IEEE Transactions On Very Large Scale Integration (Vlsi) Systems, Vol. 20, No. 2, Feb. 2012, pp. 270-283.*

[3] S. Borkar, "Thousand core chips—A technology perspective," in *Proc. ACM/IEEE Design Autom. Conf.(DAC), 2007, pp. 746–749.*

[4] P.-H. Pham, P. Mau, and C. Kim, "A 64-PE folded-torus intra-chip communication fabric for guaranteed throughput in network-on-chip based applications," in *Proc. IEEE Custom Integr. Circuits Conf. (CICC), 2009, pp. 645–648.*

[5] N. Michael, M. Nikolov, A. Tang, G. E. Suh, and C. Batten, "Analysis of application-aware on-chip routing under traffic uncertainty," in *Proc.IEEE/ACM Int. Symp. Netw. Chip (NoCS),* 2011, *pp. 9–16.*

[6] L. Benini and G. De Micheli, "Networks on chips: A new SoC paradigm," IEEE

ISSN: 2278 – 7798

Computer, vol. 35, no. 1, pp. 70–78, Jan. 2002.

[7] K. Goossens, J. Dielissen, and A. Radulescu, "Æthereal network on chip: Concepts, architectures, and implementations," IEEE Des. Test. Comput., vol. 22, no. 5, pp. 414–421, 2005.

[8] C. Neeb, M. J. Thul, and N. Wehn, "Network-on-chip-centric approach to interleaving in high throughput channel decoders," in Proc. IEEE Int. Symp. Circuits Syst. (ISCAS), 2005, pp. 1766–1769.

[9] H. Moussa, O. Muller, A. Baghdadi, and M. Jezequel, "Butterfly and Benes-based on-chip communication networks for multiprocessor turbo decoding," in Proc. Design, Autom. Test in Euro. (DATE), 2007, pp. 654–659.

ISSN: 2278 – 7798