Mitigation of Fault Current using Parallel-Resonance Type FCL

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Abstract- Fault Current Limiter (FCL) provides low cost solutions to replace conventional protection devices. This protects other equipment on the system from getting damaged by excessive fault currents. FCL became best option to reduce ratings of circuit breakers and may limit the electromagnetic stress in associated equipments. The considered structure prevents voltage sag and phase-angle jump at Point of Common Coupling (PCC) after occurrence of fault. This project considers a new parallel-LC-resonance type fault current limiter (FCL) that uses a resistor in series with a capacitor. The considered FCL is capable of limiting the fault current magnitude near to the pre-fault magnitude of distribution feeder current by placing the resistor in the structure of the FCL. In this way, the voltage of the point of common coupling does not experience considerable sag during the fault. In addition, the considered FCL does not use a superconducting inductor which has high manufacturing cost. The performance of implemented FCL is evaluated in the presence of several faults. The simulation results reveal the applicability of FCL. The simulation results are obtained using MATLAB/Simulink software.

Keywords: Parallel-Resonance type Fault current limiter (FCL), point of common coupling (PCC), power quality (PQ), semiconductor switch, total harmonic distortion (THD), voltage sag.

I. INTRODUCTION

In today circumstances, rapid development of power network cause the fault current of the system increased greatly. The levels of fault current in many places have often exceeded the withstand capacity of existing power system equipment. As implication to this matter; security, stability and reliability of power system will be negatively affected [1]. The short circuit current can’t remain unnoticed as it causes a heavy inrush of currents in a short time and as a consequence heating of the equipment’s and ultimately leading to power failure. The fault current in many places has often exceeded the withstand capacity of existing power system equipment’s. Thus limiting the fault current of the power system to a safe level can greatly reduce the risk of failure of the power system equipment’s due to high fault current flowing through the system. Since, this technology may limit the fault current to a lower level; it has grabbed a concern of research in recent past [3]. From the design point of view of the power system, limiting the fault current to a safe level can reduce the design capacity of some electrical equipment in the power system. This one will led to the reduction in the investment cost of high capacity circuit breakers and construction of new transmission line.

Consequently, from both technical and economical point of view, fault current limiting Technology for reducing short circuit current to a lower level is needed [4,5]. For a highly reliable power supply, the fault current limiter (FCL) is becoming an essential part in modern power systems. The current-limiting device is required to be introduced into the power system to prevent the fault current from rising to its full prospective value. This can also be attributed to the concern over power quality (PQ) as FCLs can be used to mitigate voltage sags caused by faults. These will avoid upgrading switchgears during system expansion and improve the PQ delivered to customers. FCLs are needed to provide a limited and sustained short-circuit current through the fault for a sufficient time (e.g., 1 s) to enable proper coordination of protective relays in the overall protection scheme.

Fault current limiters (FCLs) are developed to overcome the aforementioned problems. An ideal FCL should have the following characteristics [5], [6]:
1) Zero impedance in the normal operation;
2) No power loss in the normal operation;
3) Large impedance in the fault conditions;
4) Quick appearance of impedance when a fault occurs;
5) Fast recovery after fault removal.

The implementation of FCLs in electric power systems is not restricted to suppressing the amplitudes of short-circuit currents. Resonance-type FCLs limit the fault current by using various topologies of series or parallel LC resonant circuits [18]–[23]. Series-resonance-type FCLs are composed of a series connection of a capacitor and a superconducting inductor. They do not allow the short-circuit current to increase instantaneously as the fault occurs. However, these FCLs cannot limit the fault current level if the fault continues. Thus, the fault current will increase continually [18], [19]. Because of the use of a superconducting inductor, some of these structures need high construction cost. Therefore, they are not commercially available, particularly for third-world countries. On the other hand, resonance-type FCLs, which do not use a superconducting inductor and replace it with an ordinary copper coil, make power losses in their structures [20], [21].

As Fig.1 representation of basic FCL systems.

In this paper, a new structure for a parallel-LC-resonance type FCL is introduced. The proposed FCL uses a resistor in series with a capacitor, and therefore, it can simulate load impedance during fault. By this way, it can limit the fault current level near to pre-fault condition. From
the power quality point of view, by equating fault current and before-fault line current, the voltage of the point of common coupling (PCC) will not experience considerable change during fault condition, and power quality will improve. In comparison with the previously introduced resonance-type FCLs, this FCL does not use a superconducting inductor in the resonant circuit, and as a result, it is simpler to manufacture and has lower cost. Analysis and design considerations for this FCL are presented, and matrix laboratory (MATLAB) software [24] is used to solve the resulted formulas. The circuit operation in the normal and fault conditions is simulated by using Matlab/Simulink software [25].

Fig. 2 shows the single-phase power circuit topology of the proposed FCL. It is necessary to use a similar circuit for each phase in a three-phase distribution system. This structure is composed of two main parts which are as follows.

1) Bridge part: This part consists of a rectifier bridge containing \( D1-D4 \) diodes, a small dc-limiting reactor (\( L_{dc} \)), a self-turnoff semiconductor switch (such as a gate turnoff thyristor and an insulated-gate bipolar transistor) and its snubber circuit, and a freewheeling diode (\( D_f \)).

2) Resonance part: This part consists of a parallel \( LC \) resonance circuit (\( L_{sh} \) and \( C_{sh} \)) (its resonant frequency is equal to power system frequency) and a resistor \( R_{sh} \) in series with the capacitor. The bridge part of the proposed FCL operates as a high-speed switch that changes the fault current path to the resonance part when the fault occurs. Obviously, it is possible to substitute this part with an antiparallel connection of two self-turnoff semiconductor switches [22], [23]. Using a diode rectifier bridge has two advantages compared to two antiparallel switches as follows.

1) This structure uses only one controllable semiconductor switch which operates in the dc side instead of two switches that operate in the ac side. The control circuit is simpler because of no need for ON/OFF switching in the normal operation case.

2) It is possible to use a small reactor in series with the semiconductor switch at the dc side. This reactor plays two roles as follows.

a) It is snubber for a semiconductor switch.

b) It is as a current limiter at first moments of fault occurrence. However, placing the dc reactor inside the bridge makes the voltage drop on it because of dc current ripple. However, the current ripple is low, and consequently, the voltage drop caused by it is not considerable in comparison with the feeder’s voltage. Current ripple and voltage drop equations are studied completely in [6] and [26]. It is important to note that high-rating semiconductor switches are commercially available with current rating up
to 24 kA and voltage rating up to 4 kV [27]. Also, it is possible to use some series and/or parallel self-turnoff switches considering high current and voltage levels. The semiconductor switch needs a suitable snubber circuit for its protection, which is not shown in Fig. 2 for simplicity. Also, high-rating semiconductor switches, their protection procedure, and minimization of their power losses are discussed in [28]–[32]. From the power loss point of view, in the normal condition, the proposed FCL has the losses on the rectifier bridge diodes, the semiconductor switch, and the small resistance of the dc reactor. Each diode of the rectifier bridge is ON in half a cycle, while the semiconductor switch is always ON. Therefore, the power losses of this FCL in the normal operation can be calculated as

$$P_{loss} = P_R + P_D + P_{SW} = R_{dc} I_{dc}^2 + 4V_{DF} I_{ave} + V_{SWF} I_{dc}$$  \(1\)

Where

- \(I_{dc}\) dc-side current which is equal to the peak of the line current (\(I_{peak}\));
- \(R_{dc}\) resistance of the dc reactor;
- \(V_{DF}\) forward voltage drop on each diode;
- \(V_{SWF}\) forward voltage drop on the semiconductor switch;
- \(I_{ave}\) average current of the diodes in each cycle that is equal to \(I_{peak}/\pi\).

Considering (1) and the small value of the dc reactor in this structure, the total power losses of the proposed structure become a very small percentage of the feeder’s transmitted power.

![Fault occurrence](image1)

![Switch state](image2)

![Fault removal](image3)

Fig. 3. Control circuit of the proposed FCL.

Fig. 3 shows the control circuit of the proposed FCL. In the normal operation of the power system, the semiconductor switch is ON. Therefore, \(I_{dc}\) is charged to the peak of the line current and behaves as a short circuit. Using the semiconductor devices (the diodes and semiconductor switch) and the small dc reactor causes a negligible voltage drop on the FCL. When a fault occurs, the dc current becomes greater than the maximum permissible current \(I_0\), and the control circuit detects it and turns the semiconductor switch off. Therefore, the bridge retreats from utility. At this moment, the freewheeling diode \(I_f\) turns on and provides free path for discharging the dc reactor. When the bridge turns off, the fault current passes through the parallel resonance part of the FCL. Consequently, large impedance enters to the circuit and prevents the fault current from rising. In the fault condition, the parallel \(LC\) circuit starts to resonate. In this case, because of resonance, the line current oscillates with large magnitude [22], [23]. These oscillations may lead to damaging system equipment or putting them in stress. However, by placing a resistor \((R_{sh})\) in series with the capacitor, current transients damp quickly. In addition, by using \(R_{sh}\), the voltage drop on \(R_{sh}\) causes that the voltage across the capacitor is decreased during fault.

![Single-line diagram](image4)

Fig. 4. Single-line diagram of the power system.

When the fault disappeared, while the semiconductor switch is OFF, the parallel part of the FCL will be connected in series with the load impedance. Therefore, the line current will be decreased instantaneously. To detect this instantaneous reduction of the line current, \(I_L\) is compared with \(I_f\) that can be calculated from

$$I_f = \frac{|V_{PCC}|}{|Z_{eq}|}$$

Where \(Z_{eq}\) is the equivalent impedance of the resonance part. When the difference of \(I_L\) and \(I_f\) becomes greater than \(k\) as the fault removal sign, the control circuit turns the semiconductor switch on. Therefore, the power system returns to the normal state. The value of \(k\) can be calculated from

$$k = \frac{|V_{PCC}|}{|Z_{eq}|} - \frac{|V_{PCC}|}{|Z_{eq} + Z_{L\min}|}$$

Where \(Z_{L\min}\) is the minimum impedance of the load on the protected feeder. As pointed, some of previously proposed FCL structures have ac power losses at the resonant circuit in the normal condition, because of placing a large inductor in the line current path [20], [21]. However, the proposed structure in this paper has very low losses in the normal condition, because the inductor is bypassed by the bridge part. Also, by choosing proper values for the resonant circuit, the proposed FCL limits the fault current in a way that the power system is not affected by the fault. In such
condition, there will not be any considerable voltage sag on the PCC voltage.

III. PERFORMANCE ANALYSIS

Fig. 4 shows the single-line diagram of the power system including the proposed FCL. This figure is composed of a power source, a transformer, a circuit breaker (C.B.), an FCL, line impedance, and a load. The circuit breaker (C.B.) which is rated for the full system short-circuit current is placed to ensure the adequate protection of the power system during permanent faults. The utility voltage is a three-phase sinusoidal waveform. The utility-side impedance is modeled by a series connection of a resistor $R_s$ and an inductor $L_s$. The analytical analysis is discussed in two modes as follows:

Mode 1) Perrault steady-state operation (until $T_f$ in Fig. 5);
Mode 2) between fault occurrence and fault removal (from $T_f$ to fault removal time in Fig. 5).

![Fig. 5. Enlarged view of the line current before and after a fault.](image)

A. Mode 1:

In the normal operation of the power system, the bridge part by-passes the resonant circuit. In this condition, the line current ($i_L$) can be expressed by the following differential equation:

$$V_s \sin(\omega t) = R_i L + \omega L \left( \frac{d}{dt} i_L \right)$$

Where

- $V_s$: peak of the utility voltage;
- $\omega$: angular frequency of the utility voltage;
- $R = R_s + R_L + R_D$: resistance of the source side, load, and distribution feeder;
- $L = L_s + L_L + L_D$: inductance of the source side, load, and distribution feeder.

Therefore, the line current equation can be derived as follows:

$$i_L(\omega t) = \left( \frac{V_s}{\sqrt{R^2 + \omega^2 L^2}} \right) \left[ \left( \frac{L \omega}{\sqrt{R^2 + \omega^2 L^2}} \right) e^{-\left( \frac{R L}{2} \right) \omega t} \right.$$\nsin($\omega t - \varphi$)\n
$$= \left( \frac{V_s}{\sqrt{R^2 + \omega^2 L^2}} \right) \left[ \left( \frac{L \omega}{\sqrt{R^2 + \omega^2 L^2}} \right) e^{-\left( \frac{R L}{2} \right) \omega t} \right.$$\nsin($\omega t - \arctan \left( \frac{\omega L}{R} \right)$)$

B. Mode 2:

When a short circuit occurs, the dc-limiting reactor can limit the increasing rate of the fault current. The semiconductor switch does not operate until the line current reaches to a predefined value. By semiconductor switch operation in the $t_{sw}$ instant (Fig. 5), the bridge is switched off, and the fault current is suppressed by the resonant circuit. Therefore, the differential equation of the fault current can be expressed as follows:

$$L_s L_{sh} C_{sh} \left( \frac{d^3 i_L}{dt^3} \right) + (R_s L_{sh} C_{sh} + L_s R_{sh} C_{sh} + R_{sh} L_{sh} C_{sh}) \left( \frac{d^2 i_L}{dt^2} \right) + (L_s + R_{sh} C_{sh} R_s + L_{sh}) \frac{di_L}{dt} + R_s i_L$$

$$= (V_s - L_{sh} C_{sh} \omega^2) \sin(\omega t) + R_{sh} C_{sh} V_s \omega \cos(\omega t)$$

With initial values given in above eqn, shown at the bottom of the page, where $I_0$ is the predefined line current for semiconductor switch operation.

IV. SIMULATION RESULTS

Case 1: Three Phase Network without FCL.

Fig. 6. Shows the Matlab/Simulink circuit of PCC without FCL using Matlab/Simulink Software Package.

![Fig. 7. Three Phase Line Currents without FCL](image)
Fig. 7 shows the Three Phase Line Currents without FCL, due to sudden fault condition current goes to increases, limiting this current by using FCL.

Fig. 8 shows the Three Phase Line Voltages without FCL, due to sudden fault condition voltage may goes to decreases; maintain this voltage as constant by using FCL.

Case 2: Three Phase Network with FCL

Fig. 9. Shows the Matlab/Simulink circuit of PCC with FCL using Matlab/Simulink Software Package.

Fig. 10 shows the Three Phase Line Currents with FCL with No Rsh; due to that condition current value goes to increases & oscillated, limiting this current by using FCL with parallel resonance condition.

Fig. 11 shows the Three Phase Line Currents with Proposed FCL; due to this proposed FCL current value goes to limiting & less oscillated, limiting these oscillations in current by using FCL with parallel resonance condition.

Fig. 12 show the three phase voltage at PCC with the FCL. It is found to be undistorted voltage waveform even a fault has occurred.

Fig. 13 shows the three phase voltage drop on the FCL during the fault. This voltage drop does not allow the PCC voltage to change.
Fig. 14 (a) Line, dc reactor, and (b) shunt impedance currents. Fig. 14 shows the shunt impedance current for the three phase system.

Fig. 15 Total Power
Fig. 15 shows the Total Power with Proposed FCL.

C. Different Fault Condition:

Fig. 16. MATLAB/Simulink of the proposed circuit with different fault conditions
Fig. 16 shows the MATLAB/Simulink of the proposed circuit with different fault conditions, here we removed one of the phase fault condition.

Fig. 17 Three phase PCC voltage with the proposed FCL
Fig. 17 shows the three phase voltage at PCC with the FCL. It is found to be undistorted voltage waveform even a one of the phase at fault has occurred.

Fig. 18 Three-phase instantaneous power of the sensitive load with the proposed FCL during fault condition
Fig. 18 shows the three-phase instantaneous power of the sensitive load with the proposed FCL. It is seen that the power is remains unaltered during the fault condition.
Fig. 19 shows the three phases, in that one phase voltage drops rest of two maintained constant on the FCL during the one phase fault.

Fig. 20 shows the three phases, in that two phase voltage drops rest of one maintained constant on the FCL during the two phase fault.

V. CONCLUSIONS

The Fault Current Limiter is used to reduce the current stresses on the equipment at the time faults. FCL improves the transient stability of the power grid by reducing the voltage dips and sags. In this project, a recently developed topology of parallel-LC-resonance-type FCL with series resistor and capacitor has been implemented. For this scheme, analysis and design have been carried out. The operation of FCL in normal and fault conditions have been studied. The considered structure prevented voltage sag at PCC during the fault. This Project considered a new parallel-LC-resonance type fault current limiter (FCL) that uses a resistor in series with a capacitor. The considered FCL is capable of limiting the fault current to 400 A without shunt resistance. By placing the shunt resistor in the structure of the FCL the fault current is limited to 375 A. The voltage of the point of common coupling does not experience considerable sag during the fault. It is maintained at 11 kV. The performance of implemented FCL is evaluated in the presence of several faults. Future scope of the work can be extended with superconducting inductor included in FCL structure if cost is not a constraint.

REFERENCES


