A Higher Voltage Multilevel Inverter with Reduced Switches for Industrial Drive

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Abstract - Power electronic inverter become popular for various industrial drives applications. The multi-level inverter system is very promising in ac drives. Large electrical drives and utility application require advanced power electronics converter to meet the high power demands. As a result, multilevel power converter structure has been introduced as an alternative in high power and medium voltage situations. A multilevel converter not only achieves high power rating but also improves the performance of the whole system in terms of harmonics. The inverter output with more numbers of voltage levels with reduced number of switches as compared to cascade H-bridge inverter, which results in reduction of installation cost and have simplicity of control system. In this paper, a new configuration of a three-phase seven-level multilevel voltage source inverter is introduced. The proposed topology constitutes the conventional three-phase five-level bridge with three bidirectional switches.This three phase inverter is fed to induction motor and check the performance chtacteristicsby using matlab/Simulink platform.

IndexTerms—Bidirectional switch, fundamental frequency staircase modulation, multilevel inverter.

I. INTRODUCTION

Multilevel inverters are composed of a number of power electronic switches and DC voltage sources that produce a stepped voltage waveform in its output. Generally, multilevel inverters are divided into three categories as follows: neutral-point clamped inverter (NPC), flying capacitor inverter (FC), and cascaded H-bridge inverter (CHB). These inverters can surrender higher power with lower dv/dt and di/dt in output waveform which is to reduce EMI noise and Size of the output filter. Therefore, using theseinverters is very common nowadays. In recent years, several architectures have been proposed for cascade multilevel inverters. This kind of inverters can produce more voltage levels and also provide higher quality of power in its output. As a result, this kind of inverter is considered more than other kinds of inverters. Cascade inverters are made of series separate single phase inverters with separate dc voltage sources. On the other hand, this inverter consists of a number of basic blocks (sub multilevel inverter) that each of these blocks has similar control system. One of the major advantages of this type of inverters is the ability of its modulation. So, if an error occurs in one of the blocks, it can replace or fix by using a control system, but there are some disadvantages such as high number of dc voltage sources and power electronic switches. Increasing the number of power electronic switches leads to increase the number of driver circuits too. Both of these issues caused to increase in complexity, size, and cost of the circuit. Thus, reducing the number of power electronic switches is very vital and should be considered.

Some applications for these new converters include industrial drives, flexible ac transmission systems (FACTS), and vehicle propulsion. One area where multilevel converters are particularly suitable is that of renewable photovoltaic energy that efficiency and power quality are of great concerns for the researchers.Some new approaches have been recently suggested such as the topology utilizing lowswitching-frequency high-power devices . Although the topology has some modification to reduce output voltage distortion, the general disadvantage of this method is that it has significant low-order current harmonics.

The purpose of improving the performance of the conventional single- and three-phaseinverters, different topologies employing different types of bidirectional switches. Comparingto the unidirectional one, bidirectional switch is able to conduct the current and withstanding the voltage in both directions.Bidirectional switches with an appropriate control techniquecan improve the performance of multilevel inverters in terms of reducing the number of semiconductor components, minimizing the withstanding voltage and achieving the desired outputvoltage with higher levels. Based on this technical background, this paper suggests a novel topology for a threephase five-level multilevel inverter. The number of switching devices, insulated-gate driver circuits, and installation area and cost are significantly reduced. The magnitudes of the utilized dc voltage supplies have been selected in a way that brings the high number of voltage level with an effective application

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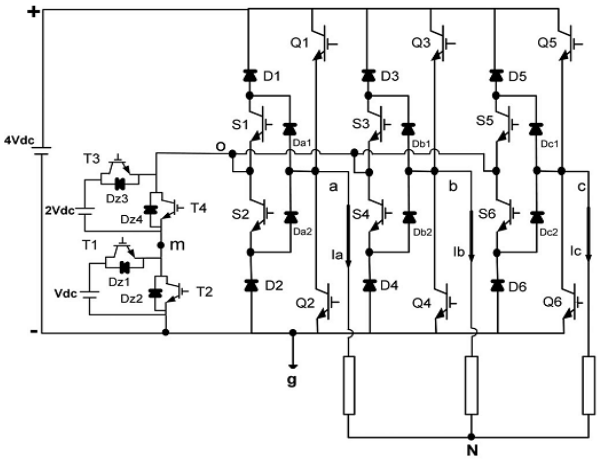
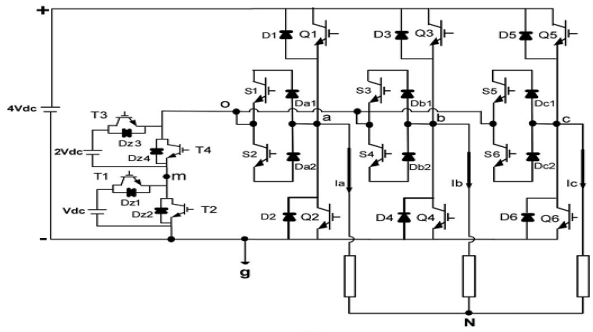
of a fundamental frequency staircase modulation technique. Extended structure forN-level is also presented and compared with the conventional well-known multilevel inverters. Simulation results are explained.

II. PROPOSED CONFIGERATION

Fig. 1(a) and (b) shows the typical configuration of the proposed three-phase five-level multilevel inverter. Three bidirectional switches (S1–S6, Da1–Dc2), two switches–two diodes type, are added to the conventional three-phase two-level bridge (Q1–Q6). The function of these bidirectional switches is to block the higher voltage and ease current flow to and from the midpoint (o). A multilevel dc link built by a single dc voltage supply with fixed magnitude of $4V_{dc}$ and CHB having two unequal dc voltage supplies of V_{dc} and 2Vdc are connected to (+,–,o) bridge terminals. Based on the desired number of output voltage levels, a number of CHB cells are used. Since the proposed inverter is designed to achieve five voltage levels, the power circuit of the CHB makes use of two series cells having two unequal dc voltage supplies. In each cell, the two switches are turned ON and OFF under inverted conditions to output two different voltage levels. The first cell dc voltage supply V_{dc} is added if switch T1 is turned ON leading to V_{mg} =+V_{dc} where V_{mg} is the voltage at node (m)with respect to inverter ground (g)or bypassed if switch T2 is turned ON leading to V_{mg} = 0. Likewise, the second cell dc voltage supply 2Vdc is added when switch T3 is turned ON resulting in V_{om}=+$2V_{dc}$ where $V_{om}$is the voltage at midpoint(o)with respect to node(m)or bypassed when switch T4 is turned ON resulting in V_{om}=0. The peak voltage rating of the switches of the conventional twolevel bridge (Q1–Q6) is 4Vdcwhereas the bidirectional switches (S1–S6) have a peak voltage rating of 3Vdc.InCHBcells,the peak voltage rating of second cell switches (T3 and T4) is $2V_{dc}$ while the peak voltage rating of T1 and T2 in the first cell is $V_{dc.}$



(a)



(b)

Fig. 1.Circuit diagram of the proposed three-phase five-level multilevel inverter.

TABLE I
Switching State S_a and Inverter Line-to-Ground Voltage V_{ag}

Sa	Q1	S1	S2	Q2	T1	T2	T3	T4	*Vag*
4	on	off	off	off	on	off	on	off	*+4Vdc*
3	off	on	on	off	on	off	on	off	*+3Vdc*
2	off	on	on	off	off	on	on	off	*+2Vdc*
1	off	on	on	off	on	off	off	on	*+Vdc*
0	off	off	off	on	on	off	off	on	0

It is easier to define the inverter line-to-ground voltages V_{ag}, V_{bg}, and V_{cg} in terms of switching states Sa, Sb, and Sc as

$$\begin{bmatrix} V_{ag} \\ V_{bg} \\ V_{cg} \end{bmatrix} = \frac{4V_{dc}}{N-1} * \begin{bmatrix} Sa \\ Sb \\ Sc \end{bmatrix} \quad (1)$$

Where N=5 is the maximum number of voltage levels.

The balanced load voltages can be achieved if the proposed inverter operates on the switching states depicted in Table II. The inverter may have 24 different modes within a cycle of the output waveform. According to Table II, it can be noticed that the bidirectional switches operate in 18 modes. For each mode, there is no more than one bidirectional switch in on state. As a result, the load current commutates over one switch and one diode (for instance: in (410), the load current I_b can flow in S3 and Db1 or S4 and Db2). Since some insulated gate bipolar transistors (IGBTs) share the same switching gate signals, the proposed configuration significantly contributed in reducing the utilized gate driver circuits and system complexity. The inverter line-to-line voltage waveforms V_{ab},V_{bc}, and $V_{ca}$with corresponding switching gate signals are depicted in Fig. 2 where V_{ab}, V_{bc}, and V_{ca} are related to V_{ag}, V_{bg}, and V_{cg} by

$$\begin{bmatrix} V_{ab} \\ V_{bc} \\ V_{ca} \end{bmatrix} = \begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ -1 & 0 & 1 \end{bmatrix} * \begin{bmatrix} V_{ag} \\ V_{bg} \\ V_{cg} \end{bmatrix} \quad (2)$$

The inverter line-to-neutral voltages V_{aN}, V_{bN}, and V_{cN} may be expressed as

$$\begin{bmatrix} V_{aN} \\ V_{bN} \\ V_{cN} \end{bmatrix} = \frac{1}{3} \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} * \begin{bmatrix} V_{ag} \\ V_{bg} \\ V_{cg} \end{bmatrix} \quad (3)$$

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It is useful to recognize that the inverter voltages at terminals a, b, and c with respect to the midpoint (o) are given by

$$\begin{bmatrix} V_{\mathrm{ao}} \\ V_{\mathrm{bo}} \\ V_{\mathrm{co}} \end{bmatrix} = \begin{bmatrix} V_{\mathrm{ag}} \\ V_{\mathrm{bg}} \\ V_{\mathrm{cg}} \end{bmatrix} - \begin{bmatrix} V_{\mathrm{og}} \\ V_{\mathrm{og}} \\ V_{\mathrm{og}} \end{bmatrix} \quad (4)$$

Where V_{og} is the voltage at midpoint(o)with respect to ground (g). V_{og} routinely fluctuates among three different voltage valuesVdc,2Vdc, and 3Vdcas follows:

$$V_{\mathrm{og}} = \begin{cases} V_{\mathrm{dc}}, & \text{if } Sa + Sb + Sc \le 5 \\ 2V_{\mathrm{dc}}, & \text{if } Sa + Sb + Sc = 6 \\ 3V_{\mathrm{dc}}, & \text{if } Sa + Sb + Sc \ge 7. \end{cases} \quad (5)$$

TABLE II
SWITCHINGSTATESSEQUENCE OF THEPROPOSEDINVERTERWITHINONECYCLE

Sa Sb Sc	Period T [s]	ON switches Leg *a*	ON switches Leg *b*	ON switches Leg *c*	ON switches cascaded half-bridge	*Vag* [V]	*Vbg* [V]	*Vcg* [V]
400	t1	Q1	Q4	Q6	T1,T4	*4Vdc*	0	0
410	t2	Q1	S3, S4	Q6	T1,T4	*4Vdc*	*Vdc*	0
420	t3	Q1	S3, S4	Q6	T2,T3	*4Vdc*	*2Vdc*	0
430	t4	Q1	S3, S4	Q6	T1,T3	*4Vdc*	*3Vdc*	0
440	t5	Q1	Q3	Q6	T1,T3	*4Vdc*	*4Vdc*	0
340	t6	S1, S2	Q3	Q6	T1,T3	*3Vdc*	*4Vdc*	0
240	t7	S1, S2	Q3	Q6	T2,T3	*2Vdc*	*4Vdc*	0
140	t8	S1, S2	Q3	Q6	T1,T4	*Vdc*	*4Vdc*	0
040	t9	Q2	Q3	Q6	T1,T4	0	*4Vdc*	0
041	t10	Q2	Q3	S5, S6	T1,T4	0	*4Vdc*	*Vdc*
042	t11	Q2	Q3	S5, S6	T2,T3	0	*4Vdc*	*2Vdc*
043	t12	Q2	Q3	S5, S6	T1,T3	0	*4Vdc*	*3Vdc*
044	t13	Q2	Q3	Q5	T1,T3	0	*4Vdc*	*4Vdc*
034	t14	Q2	S3, S4	Q5	T1,T3	0	*3Vdc*	*4Vdc*
024	t15	Q2	S3, S4	Q5	T2,T3	0	*2Vdc*	*4Vdc*
014	t16	Q2	S3, S4	Q5	T1,T4	0	*Vdc*	*4Vdc*
004	t17	Q2	Q4	Q5	T1,T4	0	0	*4Vdc*
104	t18	S1, S2	Q4	Q5	T1,T4	*Vdc*	0	*4Vdc*
204	t19	S1, S2	Q4	Q5	T2,T3	*2Vdc*	0	*4Vdc*
304	t20	S1, S2	Q4	Q5	T1,T3	*3Vdc*	0	*4Vdc*
404	t21	Q1	Q4	Q5	T1,T3	*4Vdc*	0	*4Vdc*
403	t22	Q1	Q4	S5, S6	T1,T3	*4Vdc*	0	*3Vdc*
402	t23	Q1	Q4	S5, S6	T2,T3	*4Vdc*	0	*2Vdc*
401	t24	Q1	Q4	S5, S6	T1,T4	*4Vdc*	0	*Vdc*

III.SWITCHING ALGORITHM

The staircase modulation can be simply implemented for the proposed inverter. Staircase modulation with selective harmonic is the most common modulation technique used to control the fundamental output voltage as well as to eliminate the undesirable harmonic components from the output waveforms. An iterative method such as the Newton–Raphson method is normally used to find the solutions to(N–1) nonlinear transcendental equations. The difficult calculations and the need of high performance controller for the real application are the main disadvantages of such method. Therefore, an alternative method is proposed to generate the inverter's switching gate signals. It is easier to control the proposed inverter and achieve the required output voltage waveforms in terms of Sa, Sb, and Sc. The operation of the proposed inverter, the switching states Sa, Sb, and Scare determined instantaneously.

The on-time calculations of Sa, Sb, and Sc directly depend on the instantaneous values of the inverter line-to-ground voltages. It is well known that the reference values of Vag, Vbg, and Vcg are normally given by

$$\begin{bmatrix} V_{\mathrm{ag\_ref}} \\ V_{\mathrm{bg\_ref}} \\ V_{\mathrm{cg\_ref}} \end{bmatrix} = \frac{M_a * 4V_{\mathrm{dc}}}{2} * \begin{bmatrix} \cos(wt) \\ \cos\left(wt - \frac{2\pi}{3}\right) \\ \cos\left(wt + \frac{2\pi}{3}\right) \end{bmatrix} + \frac{4V_{\mathrm{dc}}}{2} * \begin{bmatrix} 1 \\ 1 \\ 1 \end{bmatrix} \quad (6)$$

Where wt is the electrical angle. Or

$$\begin{bmatrix} V_{\mathrm{ag\_ref}} \\ V_{\mathrm{bg\_ref}} \\ V_{\mathrm{cg\_ref}} \end{bmatrix} = \frac{M_a * 4V_{\mathrm{dc}}}{2} * \begin{bmatrix} \cos(wt) \\ \cos\left(wt - \frac{2\pi}{3}\right) \\ \cos\left(wt + \frac{2\pi}{3}\right) \end{bmatrix} + \frac{4V_{\mathrm{dc}}}{2} * \left[1 - \frac{M_a}{6}\cos(3wt)\right] * \begin{bmatrix} 1 \\ 1 \\ 1 \end{bmatrix} \quad (7)$$

From (10), it can be noticed that the third harmonic component is added to the three-line-to-ground voltages. The third harmonic injection may increase the inverter fundamental voltage without causing over modulation. As a result, M_a can reach to 1.15 and Sa, Sb, and Sc can be simply determined by integerzing the reference line-to-ground voltages as

$$\begin{bmatrix} Sa \\ Sb \\ Sc \end{bmatrix} = \text{integer} \left(\frac{N-1}{4V_{\mathrm{dc}}} * \begin{bmatrix} V_{\mathrm{ag\_ref}} \\ V_{\mathrm{bg\_ref}} \\ V_{\mathrm{cg\_ref}} \end{bmatrix} \right) \quad (8)$$

Comparison of the proposed modulation method with the staircase modulation with the selective harmonic method shows that the proposed modulation features less time and needs simple calculations.

Table III
Switching State Sa1 and Inverter Line-To-Ground Voltage Vag at Ma <0.9 (Leg A)

Sa1	Q1	S1	S2	Q2	T1	T2	T3	T4	*Vag*
2	on	off	off	off	off	on	on	off	*+4Vdc*
1	off	on	on	off	off	on	on	off	*+2Vdc*
0	off	off	off	on	off	on	on	off	*0*

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Since the proposed inverter has been designed to achieve five voltage levels, the modulation index must be within range 0.9≤Ma ≤1.15. For modulation index Ma <0.9, only two dc voltage supplies 4Vdcand 2Vdcare utilized and the behavior of the proposed inverter becomes similar to the three-level multilevel inverter. Using (9)–(11) and substituting N=3, the inverter's operating switching states Sa, Sb, and Sc at Ma<0.9 can be defined. The operation principle of the proposed inverter at Ma<0.9 is illustrated in Table III.

V.INDUCTION MOTOR

Induction Motor (1M) An induction motor is an example of asynchronous AC machine, which consists of a stator and a rotor. This motor is widely used because of its strong features and reasonable cost. A sinusoidal voltage is applied to the stator, in the induction motor, which results in an induced electromagnetic field. A current in the rotor is induced due to this field, which creates another field that tries to align with the stator field, causing the rotor to spin. A slip is created between these fields, when a load is applied to the motor.

Compared to the synchronous speed, the rotor speed decreases, at higher slip values. The frequency of the stator voltage controls the synchronous speed [12]. The frequency of the voltage is applied to the stator through power electronic devices, which allows the control of the speed of the motor. The research is using techniques, which implement a constant voltage to frequency ratio. Finally, the torque begins to fall when the motor reaches the synchronous speed. Thus, induction motor synchronous speed is defined by following equation,

$$n_s = \frac{120f}{p}$$

Where f is the frequency of AC supply, n, is the speed of rotor; p is the number of poles per phase of the motor. By varying the frequency of control circuit through AC supply, the rotor speed will change.

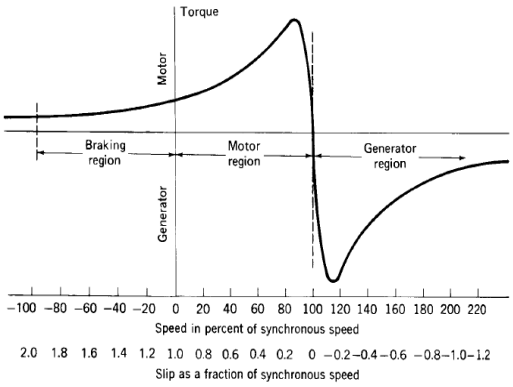

Fig.2.Speed torque characteristics of induction motor

V. MATLAB/SIMULINK RESULTS

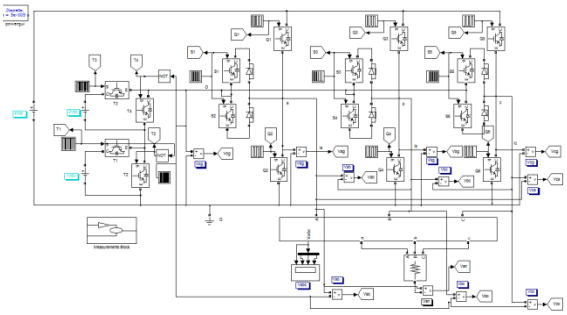

Fig .3.Simulink model of the proposed three-phase five-level multilevelinverter.

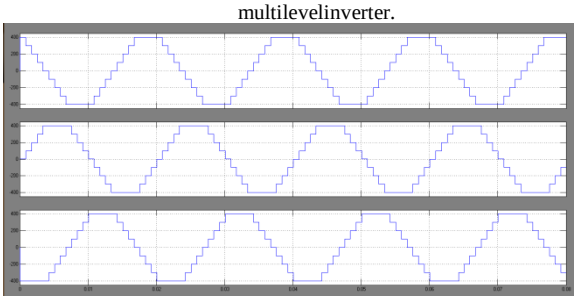

Fig .4. Simulation output Vab,Vbc and Vca of proposed five level inverter.

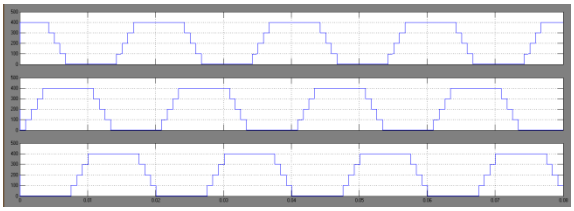

Fig .5. Simulation output Vag,Vbg and Vcg of proposed five level inverter.

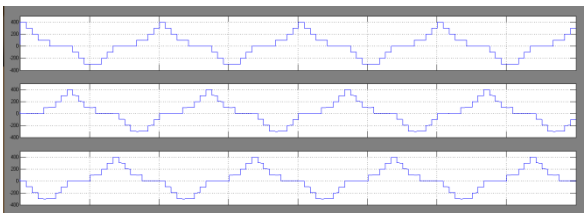

Fig .6. Simulation output Vao,Vbo and Vco of proposed five level inverter.

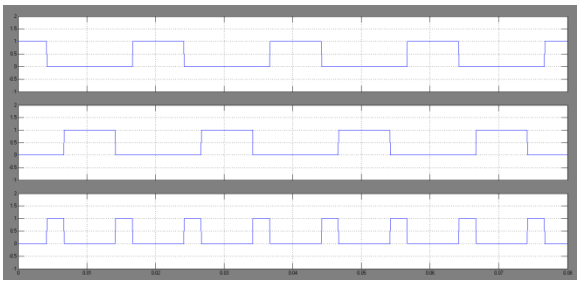

Fig .7. Simulated output wave forms of Q1, Q2 and S1.

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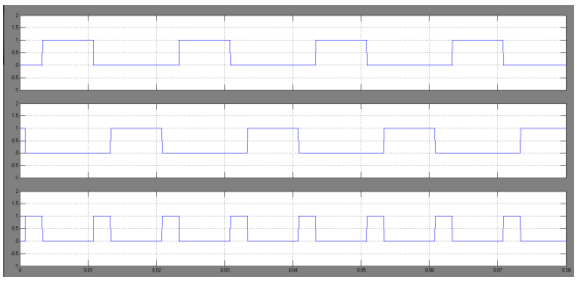

Fig .8. Simulated output wave forms of Q3, Q4 and S3.

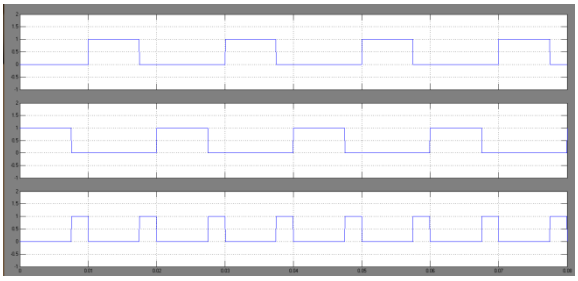

Fig .9.Simulated output wave forms of Q5, Q6 and S5.

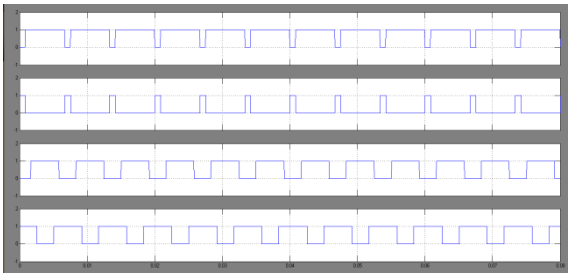

Fig .10. Simulated output wave forms of T1, T2, T3 and T4.

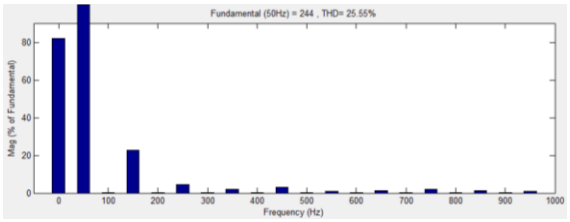

Fig .11. Total Harmonic Distortion of 5 level phase voltage shows 25.55%.

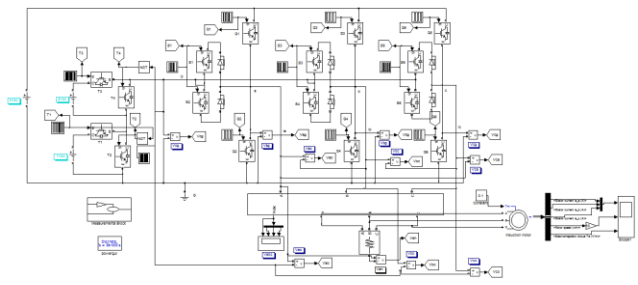

Fig .12. Simulink model of the proposed three-phase five-level multilevel inverter with induction motor

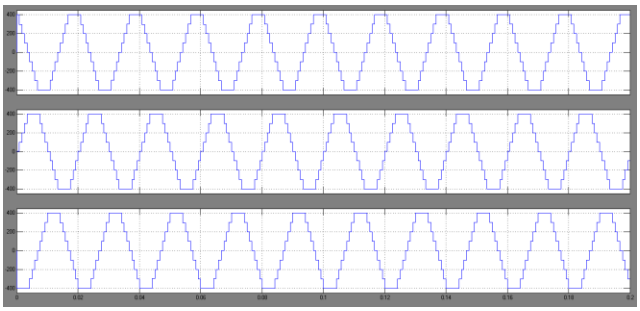

Fig.13.Simulation result for three phase voltages

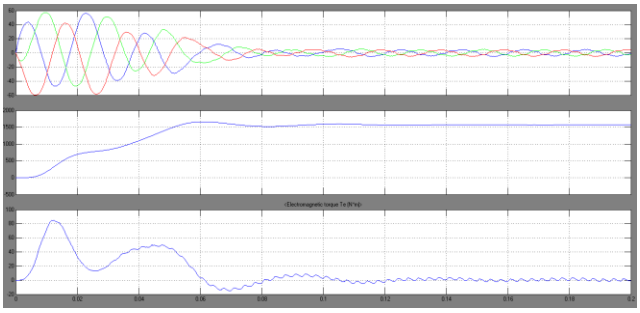

Fig.14.Simulation result for stator currents, speed and electromagnetic torque of induction motor

VI. CONCLUSION

A new topology of the three-phase seven-level multilevel inverter was introduced. The suggested configuration was obtained from reduced number of power electronic components. Therefore, the proposed topology results in reduction of installation area and cost. The fundamental frequency staircase modulation technique was comfortably employed and showed high flexibility and simplicity in control. Moreover, the proposed configuration was extended to N-level with different methods. Furthermore, the method employed to determine the magnitudes of the dc voltage supplies was well executed. In order to verify the performance of the proposed multilevel inverter, the proposed configuration was simulated and its prototype was manufactured. The obtained simulation results met the desired output. Hence, subsequent work in the future may include an extension to higher level with other suggested methods. For purpose of minimizing THD%, a selective harmonic elimination pulse width modulation technique can be also implemented.

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