Low leakage and high speed BCD adder using clock gating technique

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Abstract— **The growing market of mobile, battery powered electronic systems (e.g., cellular phones, personal digital assistants, etc.) demands the design of microelectronic circuits with low power dissipation. As density and complexity of the chips continue to increase, the difficulty in providing power dissipation might limit the functionality of the computing systems. Especially, at nanometer level the power dissipation consumes about 35% of the chip power. Power dissipation comes from two components: static dissipation and dynamic dissipation.**

The purpose of this project is to analyze the performance of one of the most trustful approaches to low power design called as "Power Gating". The focus is only on CMOS devices in nanometer scale, as this technology is being the most widely adopted in current VLSI systems. a transistor with high threshold voltage (Vth) is placed in series with a low Vth device. The high Vth transistor is called as the Sleep Transistor. In the power gating structure, a circuit operates in two different modes. In the active mode, the sleep transistors are turned ON and can be treated as the functional redundant resistances. In the sleep mode, the sleep transistors are turned OFF to reduce the leakage power.

Optimum sleep transistor design and implementation are seems to be critical to a successful power-gating design. The leakage and power consumed are analyzed at the sleep transistor by changing the input to either '0' or '1'.

A proposed technique for leakage power reduction is the stack approach, the total leakage power for cascading transistor chain will decrease with the increase in the number of stacked transistor. One Transistor is provided with sleep input and other two transistors connected in series to the sleep transistor is given stack input. The advantage of combining stacked sleep transistors is to form a cascading chain of transistors which reduces the burden on a single transistor.

Electric Tool is used to design the schematic and layout level diagrams of our project. The LT-SPICE Tool will be used for simulation of the Spice code which tests the functionality of our generated layout and schematic blocks.

Index Terms—**BCD adder, Clock gating , One bit full adder, stack gating**

I. INTRODUCTION

The scaling of process technologies to nanometer regime has resulted in a rapid increase in leakage power dissipation. Hence, it has become extremely important to develop design techniques to reduce static power dissipation during period's inactivity. The power reduction must be achieved without trading-off performance which make it harder to reduce leakage during normal (runtime) operation. On the other hand, there are several techniques for reducing leakage power in sleep or standby mode.

Power gating is one such well known technique where a sleep transistor is added between actual ground rail and circuit ground (called virtual ground). This device is turned-off in the sleep mode to cut-off the leakage path. It has been shown that this technique provides a substantial reduction in leakage at a minimal impact on performance. Power gating technique uses high Vt sleep transistors which cuts off VDD from a circuit block when the block is not switching. Power gating affects design architecture more than clock gating. It increases time delays as power gated modes have to be safely entered and exited. Architectural trade-offs exist between designing for the amount of leakage power saving in low power modes and the energy dissipation to enter and exit the low power modes. Shutting down the blocks can be accomplished either by software or hardware. Optimum sleep transistor design and implementation are critical to a successful power-gating design.

Leakage power has been increasing exponentially with the technology scaling[2][3]. In 90nm node, leakage power can be as much as 35% of chip power. Consequently, leakage power reduction becomes critical in low-power applications such as cell phone and handheld terminals. Power-gating is the most effective standby-leakage reduction method recently developed[4]-[7]. In the power gating, sleep transistors are used as switches to shut off power supplies to parts of a design in standby mode. Although the concept of the sleep transistor is simple, design of a correct and optimal sleep transistor is challenge because of many effects introduced by the sleep transistor on design performance, area and overall power dissipation.

Power dissipation is becoming widely recognized as a top-priority issue in VLSI circuit design. One of the most challenging problems faced by the VLSI designer in present scenario, is to find out new and effective circuit design techniques to reduce the overall power dissipation without compromising the performance of the device.

Currently, many of the effects have not been fully aware by designers. This could result in improper sleeper transistor design that would either fail to meet power reduction target when silicon is back or cause chip malfunction due to serious power integrity problems introduced. A number of critical considerations in the sleep transistor design and implementation including header or footer switch selection,

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sleep transistor distribution choices and sleep transistor gate length, leakage and efficiency have been considered.

A sleep transistor is referred to either a PMOS or NMOS high V_{th} transistor that connects permanent power supply to circuit power supply which is commonly called "virtual power supply".

II. LOW POWER DESIGN

The header switch is implemented to control Vdd supply. PMOS transistor is less leaky than NMOS transistor of a same size. The NBTI effect increases Vth over time and makes PMOS transistor even less leaky. Header switches turn off VDD and keep VSS on. As the result, it allows a simple design of a pull-down transistor to isolate power-off cells and clamp output signals in "0" state as shown in Fig 1. The "0" state isolation is complied with reset state requirement in most designs. The disadvantage of the header switch is that PMOS has lower drive current than NMOS of a same size, though difference is reduced by strained silicon technology. As a result, a header switch implementation usually consumes more area than a footer switch implementation.

The footer switch is implemented by NMOS transistor to control VSS supply. The advantage of footer switch is the high drive and hence smaller area. However, NMOS is leakier than PMOS and application designs become more sensitive to ground noise on the virtual ground (VVSS) coupled through the footer switch. The isolation on "0" state becomes complex due to loss of the virtual ground in sleep mode and necessity of bypassing footer switch to reach permanent VSS. In the following part of the paper, we shall focus on header switch design and implementations.

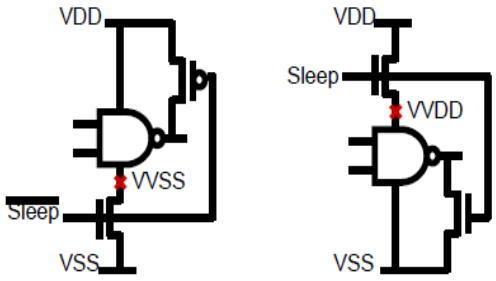

Fig:1 Header and Footer Sleep Transistor implementation of NAND gate.

A.Sleep Transistor Efficiency (I_{on}/I_{off}):

The sleep transistor efficiency is defined by a ratio of drain current in ON and OFF states, i.e. I_{on}/I_{off}. It is desirable to maximize the efficiency to achieve high drive in normal operation and low leakage in sleep mode. The sleep transistor efficiency can be analyzed by SPICE simulations where two high V_{th} transistors are configured for ON and OFF state respectively to measure Ion and I_{off}. A high temperature is set on ON sleep transistor to model high chip temperature in operating mode and a low temperature is set on OFF sleep transistor to reflect the cool situation when the design is in sleep mode. The sleep transistor efficiency varies with gate length, width and body bias. The curves were generated by SPICE simulation of a TSMC90G high V_{th} PMOS transistor with foundry provided BSIM4 v2.0 model. The junction temperature of the transistor is set 125C^o in Ion analysis and 25Co in I_{off} analysis. V_{ds} is set equal to V_{dd} in I_{off} analysis and 10mV in Ion analysis reflecting the IR-drop target on the sleep transistor.[8]

B. Sources of Power Dissipation

Power dissipation in VLSI circuits can be broadly divided into two categories: Dynamic or switching power, and Static or leakage power dissipations. Dynamic power dissipation results due to charging and discharging of internal capacitances in the circuit. Leakage power dissipation occurs during the static input state of the device. Leakage power dissipation is much more noticeable in low threshold voltage MOS transistors. This power dissipation arises because of the presence of subthreshold and gate oxide leakage currents. Gate oxide leakage current occurs because of the desire to increase the performance characteristics of MOS transistor by decreasing the thickness of the gate oxide layer while subthreshold leakage current occurs between the source and the drain region of a MOS transistor in weak inversion state. The subthreshold leakage current occurs even when the applied gate voltage, VGS, is less than the threshold voltage, V_{TH}, of the MOS transistor. A general formula for the total power dissipation in a VLSI circuit can be expressed as:

$$P_T = P_{dynamic} + P_{static} \quad (1)$$

$$P_T = \alpha C V_{DD} 2 f_{clk} + N(1-\alpha) V_{DD} I_S + N(1-\alpha) VDD\ I_{OX} \quad (2)$$

where α is the switching activity factor which represents the probability of the output switching, C is the sum of all load capacitance in the design, V_{DD} is the supply voltage, f_{clk} is the clock frequency, N is the number of gates, I_S is the average subthreshold leakage current of a gate, and I_{OX} is the average thin-oxide leakage current of a gate.

2.5 Leakage:

In electronics, leakage may refer to a gradual loss of energy from a charged capacitor. It is primarily caused by electronic devices attached to the capacitors, such as transistors or diodes, which conduct a small amount of current even when they are turned off. Even though this off current is an order of magnitude less than the current through the device when it is on, the current still slowly discharges the capacitor. Another contributor to leakage from a capacitor is from the undesired imperfection of some dielectric materials used in capacitors, also known as *dielectric leakage*. It is a result of the dielectric material not being a perfect insulator and having some non-zero conductivity, allowing a *leakage current* to flow, slowly discharging the capacitor.

Another type of leakage occurs when current leaks out of the intended circuit, instead flowing through some alternate path. This sort of leakage is undesirable because the current flowing through the alternate path can cause damage, fires, RF noise, or electrocution. Leakage of this type can be measured by observing that the current flow at some point in

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the circuit doesn't match the flow at another. Leakage in a high-voltage system can be fatal to a human in contact with the leak, as when a person accidentally grounds a high-voltage power line.

Leakage may also mean an unwanted transfer of energy from one circuit to another. For example, magnetic lines of flux will not be entirely confined within the core of a power transformer; another circuit may couple to the transformer and receive some leaked energy at the frequency of the electric mains, which will cause audible hum in an audio application.

Leakage current is also any current that flows when the ideal current is zero. Such is the case in electronic assemblies when they are in standby, disabled, or "sleep" mode. These devices can draw one or two microamperes while in their quiescent state compared to hundreds or thousands of milliamperes while in full operation. These leakage currents are becoming a significant factor to portable device manufacturers because of their undesirable effect on battery run time for the consumer.

C. Reduction Techniques

There are several VLSI techniques to reduce leakage power. Each technique provides an efficient way to reduce leakage power; but disadvantages of each technique limit the application of each technique. Static power consumption is a major concern in nanometre technologies. Along with technology scaling down and higher operating speeds of CMOS VLSI circuits, the leakage power is getting enhanced. As process geometries are becoming smaller, device density increases and threshold voltage as well as oxide thickness decrease to keep pace with performance.

D. Power-Gating

Power-gating (PG) is the most intuitive technique for reducing leakage currents. It introduces a power switch to temporarily power down unused parts of an ASIC design. In this state the difference in leakage currents I_{ACTIVE} - I_{SLEEP} is saved. The switch is typically made of a single transistor and is also referred to as sleep transistor. As simple as the idea of power-gating sounds, it is complicated to implement and to consider its impact during the design because of an immense range of implementation artifacts. Most important design parameters are the type and size of a sleep transistor, the interfacing to neighboring components, as well as the component size to which power-gating is applied. A major drawback of power-gating is the loss of the internal state during sleep.

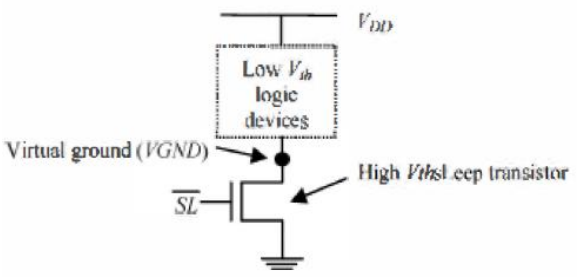

Fig:2 Power Gating Structure

Power-gating technique uses a high Vth sleep transistor in series with the pull-up and/or the pull-down of a low Vth logic block to reduce leakage power. The sleep transistor can be turned off when the low Vth logic block is inactive, thus resulting in a significant reduction of sub-threshold leakage current. Fig 1 shows a sleep transistor used for power gating. A sleep transistor can be a high Vth NMOS or PMOS transistor. A PMOS sleep transistor served as a header switch connects the power network to virtual VDD, Figure 2. An NMOS sleep transistor served as a footer switch connects the ground network to virtual GND. Normally, either a header switch or a footer switch is used to conserve area and reduce timing penalty caused by voltage drop across sleep transistors.

The header switch is implemented by PMOS to control Vdd supply. PMOS transistor is less leaky than NMOS transistor of the same size. The disadvantage of the header switch is that PMOS has lower drive current than NMOS of a same size. As a result, a header switch implementation usually consumes more area than a footer switch implementation. The footer switch is implemented by NMOS transistor to control VSS supply. The advantage of footer switch is the high drive and hence smaller area. However, NMOS is leakier than PMOS and sleep transistor become more sensitive to ground noise.

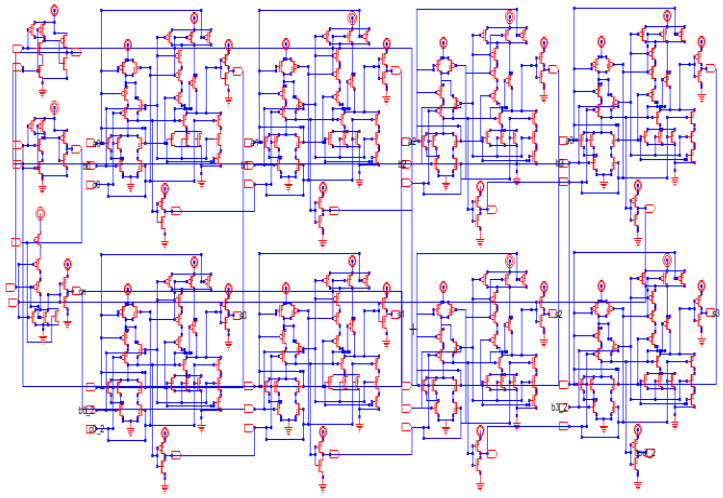

Fig:3 BCD adder Power Gating Structure with Header & Footer Switch

E. Power Gating Parameters

Power gating implementation has additional considerations for timing closure implementation. The following parameters need to be considered and their values carefully chosen for a successful implementation of this methodology.

***Power gate Size*:** The power gate Size must be selected to handle the amount of switching current at any given time. The gate must be bigger such that there is no measurable voltage (IR) drop due to the gate. As a rule of thumb, the gate Size is selected to be around 3 times the switching capacitance. Designers can also choose between header (P-MOS) or footer (N-MOS) gate. Usually footer gates tend to be smaller in area for the same switching current.

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Dynamic power analysis tools can accurately measure the switching current and predict the Size for the power gate.

***Gate control slew rate*:** In power gating, this an important parameter that determines the power gating efficiency. When the slew rate is large, it takes more time to switch off and switch-on the circuit and hence can affect the power gating efficiency. Slew rate is controlled through buffering the gate control Signal.

***Simultaneous switching capacitance*:** This important constraint refers to the amount of circuit that can be switched simultaneously without affecting the power network integrity. If a large amount of the circuit is switched simultaneously, the resulting "rush current" can compromise the power network integrity. The circuit needs to be switched in stage in order to prevent this.

***Power gate leakage*:** Since power gates are made of active transistors, leakage reduction is an important consideration to maximize power savings

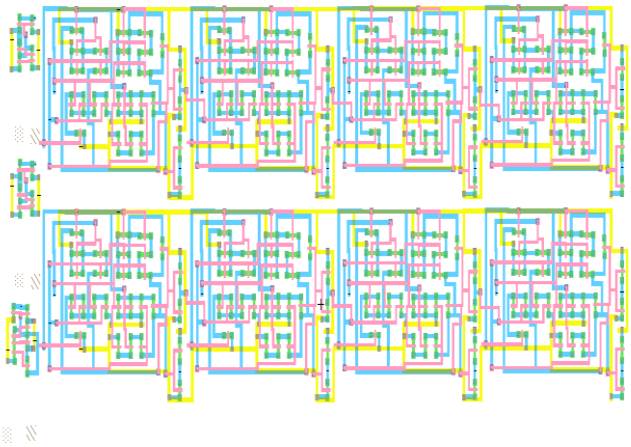

Fig :4 BCD adder Power Gating lay out .

III. DISTRIBUTED SLEEP TRANSISTOR NETWORK (DSTN)

Sleep transistors are effective to reduce dynamic and leakage power. The cluster-based design was proposed to reduce the sleep transistor area by clustering gates to minimize the simultaneous switching current per cluster and then inserting a sleep transistor per cluster.

We propose a novel distributed sleep transistor network, and show that DSTN is intrinsically better than the cluster-based design in terms of the sleep transistor area and circuit performance.

We reveal properties of optimal DSTN designs, and develop an efficient algorithm for gate level DSTN synthesis. The algorithm obtains DSTN designs with up to 70.7% sleep transistor area reduction compared to cluster-based designs. Furthermore, we present custom layout designs to verify the area reduction by DSTN.

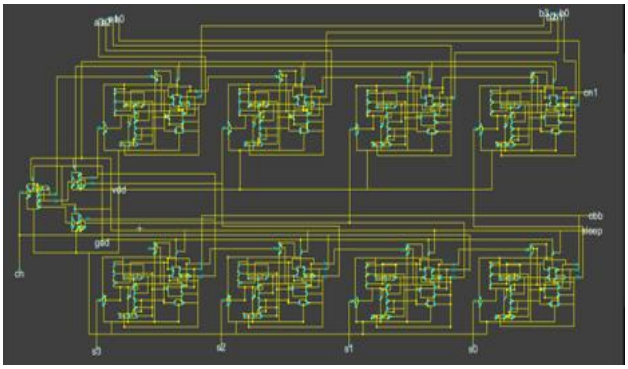

Fig:5 Distributed sleep transistor network

When discharging current flows over sleep transistors, the voltage drop in sleep transistor 2 tends to be larger than the voltage drop in sleep transistor 1 and 3, which causes a part of current from module 2 flowing to transistors 1 and 3. The total area of all the sleep transistors in DSTN ca n thus be significantly reduced with presence of such current discharging balance.

Distributed sleep transistor network is advantageous in area and performance compared to module-based and cluster-based sleep transistor designs.[9]

IV. BCD ADDER USING CLOCK GATING TECHNIQUE

Clock gating is one of the most effective and widely used techniques for saving clock power. The clock net is one of the nets with the highest switching density, resulting in high power dissipation in the adders. A promising technique to reduce the power dissipation of the clock net is selectively stopping the clock in parts of the circuit, called “clock gating”. It is very well integrated into semi-custom design flows nowadays.

By gating the clock, the switching activity of the adders clock signal is reduced. However, clock gating circuitry itself occupies chip area and consumes additional power; therefore a judicious selection of circuit. Figure 6

Clock-gating is a well-known technique to reduce clock power. In clock gating clock to an idle block is disabled. Thus significant amount of power consumption is reduced by employing clock gating.

By clock gating technique, clock to an idle portion is disabled, thus avoiding power dissipation due to unnecessary charging and discharging of the unused circuit. In clock gating clock is selectively stopped for a portion of circuit which is not performing any active computation. Local clocks that are conditionally enabled are called gated clocks, because a signal from the environment is used to gate the global clock signal.[10]

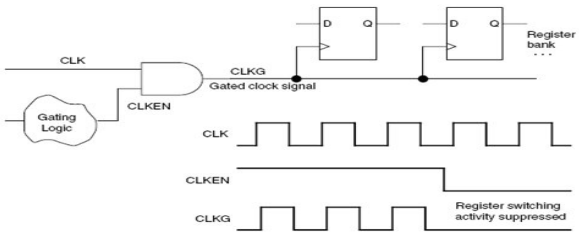

Fig:6 Clock Gating

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Figure shows reduction in switching activity when not needed controlling the logic circuit using a clock enable signal(CLKEN) resulting in a suppressed gated clock signal(CLKG).

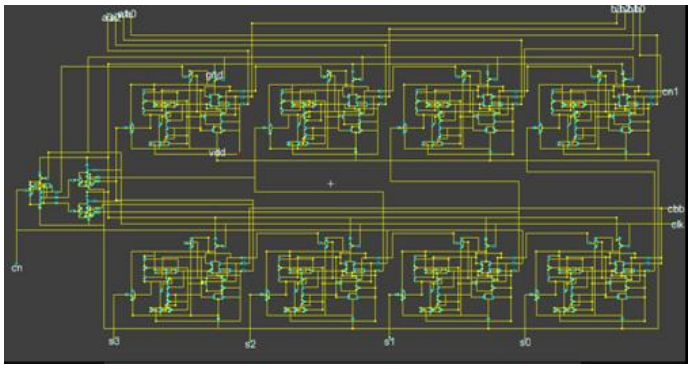

Fig:7 BCD adder with Clock Gating

V. SIMULATION RESULTS

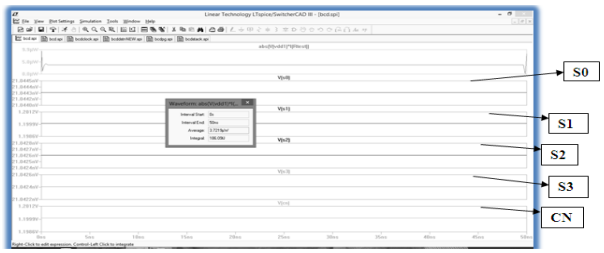

Fig:9 BCD adder simulation result

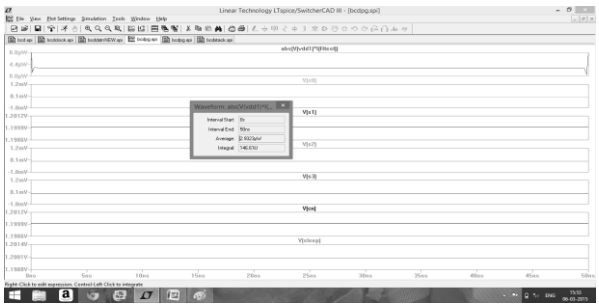

Fig:10 BCD adder with power gating

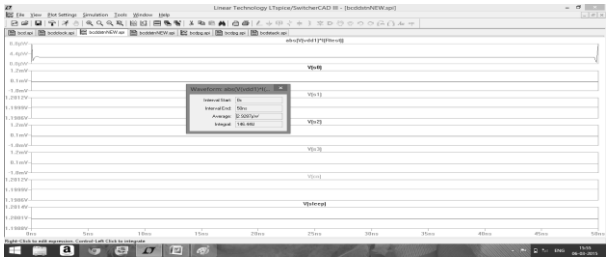

Fig:11 BCD adder with DSTN

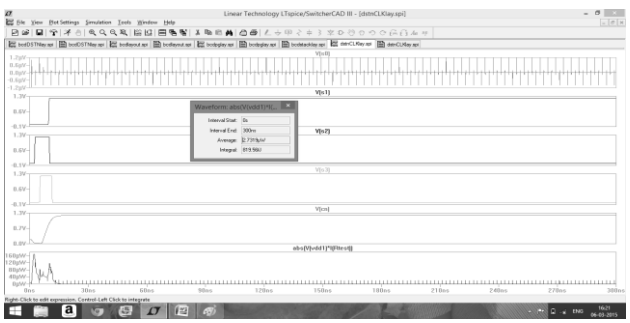

Fig:12 BCD adder with clock gating

A. Comparison of Power Analysis

S No:	Technique	Power Consumption(µW) Schematic	Layout
1	Conventional BCD Adder	3.7219	5.5132
2	BCD Adder(Power Gating)	2.9323	2.9364
3	BCD Adder(DSTN)	2.9287	3.1754
4	BCD Adder(Clock Gating)	1.1312	2.7319

Table No.1 Power Analysis Comparison

S.No:	Technique	Leakage Power (nW
1	BCD Adder(Power Gating)	4.389
2	BCD Adder(DSTN)	3.701
3	BCD Adder clock gating	2.331

Table No:2 Leakage Power Comparison

VI. CONCLUSION

In nanometer scale CMOS technology, sub threshold leakage power consumption is a great challenge. Although previous approaches are effective in some ways, no perfect solution for reducing leakage power consumption is yet known. Therefore, designers choose techniques based upon technology and design criteria. Sleep transistor is designed at 65nm scale and implemented in clock gating circuit.

Here we provide a novel circuit structure named "clock gating" as a new remedy for designer in terms of static power and dynamic powers. Unlike the sleep transistor technique, the stacking technique retains the original state. The stacking approach shows the least speed power product among all methods. Therefore, the stacking technique provides new ways to designers who require ultra-low leakage power consumption with much less speed power product. So, it can be used for future integrated circuits for power & area Efficiency

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