Design And Implementation Of Reliable Hybrid Bypassing Multiplier

J.Amulya and CH.Manaswini

Abstract **—** Digital multipliers are the crucial arithmetic functional units of digital filters. The overall performance of digital filters depends on the throughput of multiplier design. Multiplication possibly will be a profoundly utilized operation in digital signal processes and many scientific applications. Multipliers may be a extremely hardware concentrated components and thus we as users focus on some design issues like obtaining low-power, smaller space and better speed. This hold logic reduces the performance decline will effect on delay. The hybrid bypass reliable multiplier is used to reduce the delay. This hybrid bypassing multiplier has reliability so that this multiplier can be applied to digital filter so as to enhance its performance. The verilog language is used for coding, synthesis was done by using Xilinx ISE 13.1

Index Terms**—Throughput; Hold logic; Reliability; Bypassing Multiplier;Digital filters;Delay.**

I. INTRODUCTION

Day by day IC technology obtaining additional advanced in terms of style and its performance analysis. A quicker style with lower power consumption and smaller space is implicit to the trendy electronic styles. Unceasing advancement in electronics style technology makes improved use of energy, code knowledge with success, communicate info way more firm, etc. significantly, several of those technologies address low-power consumption [1] to fulfill the necessities of assorted transportable applications. In these application systems, a multiplier could be a basic arithmetic unit and wide employed in circuits that the multiplication method ought to be optimized properly.

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Multipliers typically have extended latency, huge space and consume substantial quantity of power. Thus low power design style has become a very important half in VLSI system style. Everyday new approaches square measure being developed to implement the low-power multipliers at technological, physical, circuit and logic levels [3]. Since multiplier is mostly the slowest component during the execution of system, the system's performance is decided by throughput of multiplier.

Column-bypassing multiplier [5] design was an enhancementof the standard array multiplier (AM). The multiplier array made up of (n−1)rows of carry save adder (CSA), in which each row incorporate with (n − 1) full adder (FA) cells [11]. All full adders have two outputs: 1.the sum bit moves down and 2. The carry bit moves to the lower left of full adder and the very last row is for carry propagation.

Full adder cells in the array multiplier were always in operating condition in any case of output states. Low power column bypassing multiplier [4] was designed in a way that the full adder cells were inoperative when the subsequent bit co-efficient was 0. In column bypass multiplier multiplicand bit was taken in to consideration.

All inputs were connected to the full adders by utilizing tristate gates. Presume the inputs were 1111_2*1001_2, by taking this example the two inputs to thefirst and second rows of full adder cells were become 0. In the above example b1 is 0 so the selection line to the multiplexer also 0 and it disable the full adder operations and selects aib0 as sum and 0 as carry because the tristate gates disable the input path of the full adder[11]. Therefore the outputs of the current full adder were bypassed to next stage full adder cells. Because of all these actions the power consumption was reduced.

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A. *Column Bypassing Technique*

Column Bypassing with reference to multiplier means switching off certain columns in the multiplier array each time certain multiplicand bits are zero. In this technique, throughout working, the operations in a column can be disabled if the corresponding bit in the multiplicand is 0, to save the power.This technique was completely depended on the number of zeroes in the multiplicand bits. For the column bypassing[5] multiplication operation the full adder cell in the normal array multiplier is modified. For the column bypassing multiplication operation the full adder cell in the normal array multiplier is modified.

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B. *Modified Full adder Cell*

The modified full adder cell of column bypassing multiplier constructed with two tristate gates and one multiplexer. Tristate gates were utilized for activating and blocking the inputs to the full adder cell depending on the selection line of the multiplexer. If the selection line of the multiplexer is one then the input to the full adder cell was disabled and preceding full adder sum is taken as the sum of the present full adder.

II. HYBRID BYPASSING MULTIPLIER

In the proposed hybrid bypassing multiplier architecture, the multiplicand or multiplicator to calculate the operation using hybrid bypass reliable multiplier. The multiplicator and multiplicand follows a standard distribution. The below figure 1 shows the hybrid bypass reliable multiplier architecture.

Multiplier implementation using hybrid bypass technique has two significant characteristics. Firstly, it was a variable-latency hybrid design that diminishes the non-critical paths delay. Secondly, it gives accurate output or product still after the aging effect [10].

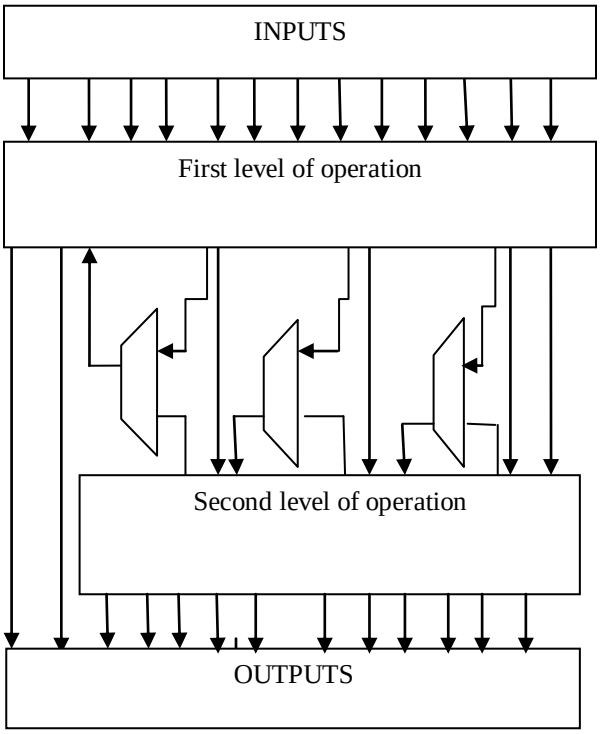

Fig: 1Hybrid Bypass Reliable Multiplier.

The inputs of the multiplier are multiplicand X and multiplier Y. These two inputs goes under first level of operation and then goes to second level of operation with mux gives the outputs of multiplier. First level and second level consists of adder cells and they perform required arithmetic operations to generate partial sums andthey were moved down to second level and carry bits were propagating to the next level through multiplexers.

Compared to the multiplier implementation using hold logic, number of operations using hybrid bypassing multiplier implementation was reduced. Due to this reduced number of operations the time required to execute the multiplication operation was reduced. So the delay of the multiplier has been reduced. Due to this reduced number of instructions hardware complexity of multiplier also reduces.

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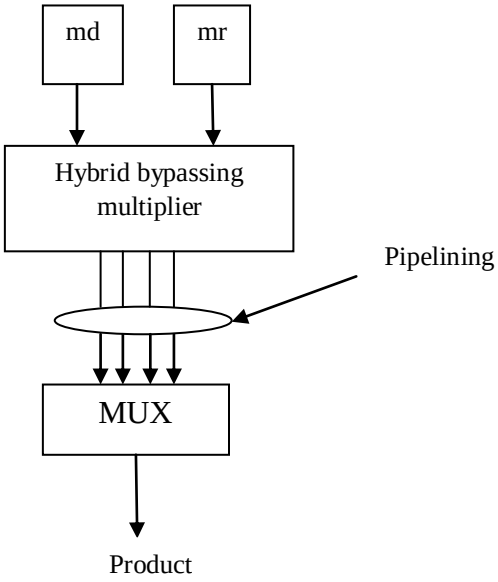

Fig: 2 Block Diagram Of Hybrid Bypass Multiplier.

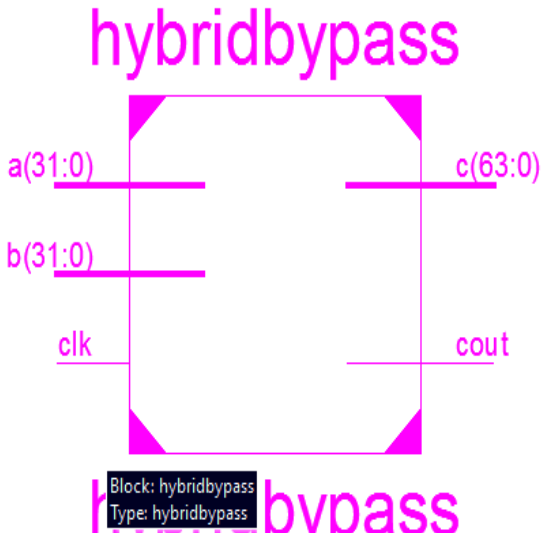

Fig: 3 RTL Schematic.

Above figure 2 shows the basic block diagram of hybrid bypassing multiplier with MUX family. It consists of two input registers to read two input values. Inputs are passed to the hybrid bypassing multiplier and after the completion of operation in hybrid bypassing multiplier the partial products are passed to multiplexer. Multiplexer gives the final product depending on the preferences. The main goal of this paper is to design and implement hybrid bypassing multiplier 32×32 multiplier. The experiment results shown below.

III. SIMULATION RESULTS

The below fig 3 shows the RTL schematic of hybrid bypass reliable multiplier.It consists of two 32 bit inputs and clock pulse. It also shows the 64 bit output and a carry out.

The below fig:4 shows thw gate level RTL schematic of hybrid bypass multiplier.

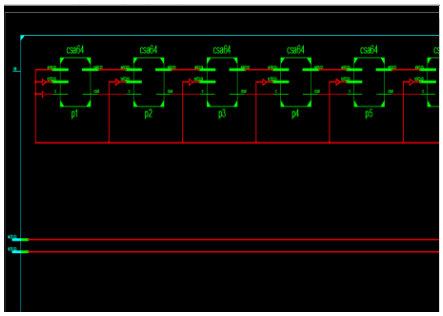

Fig:4 GATE Level RTL Schematic

The fig:6 shows the Gate Level RTL schematic of hybrid bypass reliable multiplier. RTL schematic is the schematic illustration of a synthesized source file. Above shown diagram is the RTL schematic of hybrid bypassing multiplier. In this figure pre-optimized representation of components utilized in the source code were displayed.

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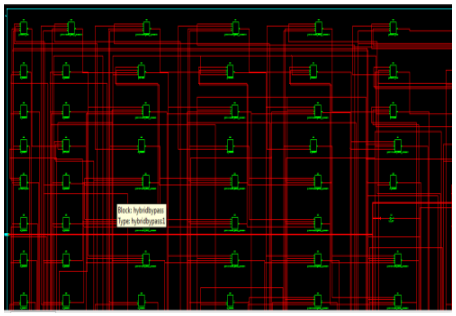

Fig: 5 TechnicalSchematic.

The above Fig: 5show the technical schematic of hybrid bypassing multiplier.

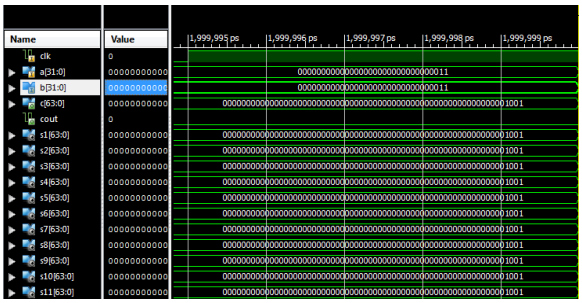

Fig: 6 Output Waveform.

The above fig: 6show the output waveform of hybrid bypass reliable multiplier.In the figure the timing waveforms a[31:0], b[31:0] represents two 32-bit inputs to the hybrid bypassing multiplier. The timing waveform c[63:0] represents the output signal that is the product of two 32-bit inputs.clk is the clock signal supplied to the system

AREA REPORT:

Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slices	2012	14752	13%
Number of 4 input LUTs	3693	29504	12%
Number of bonded IOBs	129	250	51%

Fig: 7 Area Report

The below tabular form shows the comparison of area and delay for both existed system and proposed system.

SYSTEM	AREA[kb]	DELAY[ns]
Existed	595912	178
Proposed	453664	126

Table: 1 comparison table

IV. CONCLUSION

Multiplication with hold logic reduces the performance will effect on delay. The hybrid bypass reliable multiplier is used to reduce the delay. By using proposed system will gives better performance than existed system. The parameters like area, delay and speed are highly positive perform to maintain the system. The delay of the system is reduced so speed is increased.

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