Implementation and Analysis of Different Line Coding Schemes using Verilog

Ankit Gupta, Gurashish Singh

Abstract—**Line Coding is a discipline in the field of telecommunication which governs several kinds of sophisticated coding methods for transmitting a digital signal. It is intensively employed in baseband communication systems. In educational institutions, Line Coding is practiced on electronic trainers. This paper represents the implementation of different Line Coding schemes like NRZ, RZ and Biphase on the Verilog-HDL software platform. The Verilog-HDL code is simulated and analyzed using ModelSim tool of MentorGraphics. The results have been observed on the software interface in the form of various waveforms. An attempt has been made for a user-friendly software oriented approach to study different kinds of Line Codes which eventually poses a merit over traditional trainers.**

Index Terms—**Biphase, HDL, Line Coding, NRZ, RZ and Verilog.**

1. INTRODUCTION

In every digital transmission, the data has to be reformatted before modulation. Modulation is a technique of producing a new signal by mixing it with a sinusoid of high frequency.

Expressing the digital data in a specified format is known as **Line Coding**. It is a process of encoding every bit into some signal elements where in every signal element is a discrete and discontinuous voltage pulse. This has huge application in modulation. It is an important part of any digital communication system. It has already been established that it is dependent on the available system parameters. As a block, it takes digital data as an input and gives digital data as output (not necessarily binary). So, it can be considered as a Digital Logic System.

Line Coding is done to achieve many goals such as

- Self-clocking,
- In-service error monitoring,
- Introducing spectral nulls in dc frequency when channel is ac coupled,
- Modifying the signal spectrum, thereby further reducing cross-talk in radio-frequency interferences and foreign systems,
- To reduce the complexity in equalization, detection, timing recovery circuits and echo cancellations etc. [1].

The encoding scheme is chosen on the basis of various distinct characteristics. Some vital features to demarcate and choose various kinds of **Line Coding** schemes are *Bandwidth, Self-synchronization, Error-detection, Differential encoding, Dc-component* and *Transparency.*

Generally, the **Line Coding** schemes are implemented on trainers in educational institutions. With the aid of this proposed project, one can simulate the **Line Coding** using versatile **HDL** (Hardware Description Language), **Verilog**.

Verilog is a Hardware Description Language, which is widely used as a textual format for describing electronic circuits and systems. It came into existence as a proprietary language supported by a simulation environment that was first to support mixed-level design representations comprising Switches, Gates, Register Transfer Level (RTL) circuits, and higher level abstractions of digital circuits. The simulation environment provides an authentic and uniform method to implement and verify digital circuits.

2. THE LINE CODING SCHEMES

The various **Line Coding** schemes that have been discussed in this paper are as follows:

2.1 Not-Return to Zero (NRZ):

It is one of the most commonly used signaling scheme which deals with different levels for different symbols. During the clock interval, the value of the signal does not return to zero. For NRZ-Unipolar, the bit '1' is represented by voltage +V whereas '0' is represented by voltage 0. If the bit '0' is represented by a negative –V, the signal is called NRZ-Bipolar.

2.1.1 NRZ- Level (NRZ-L):

When bits are represented with certain levels for the two symbols, it is called as NRZ - Level (NRZ-L).

$$A_1(t) = +V,\ 0 \le t \le T_b \quad (2)$$

$$A_0(t) = 0,\ 0 \le t \le T_b \quad (3)$$

At receiver side, the clock signal is not directly available. So, it can be extracted using the receiver signal. This is also called self-clocking and forms a basis for clock regeneration. It is required that transmitter and receiver clock should be synchronized for apt recovery of data. However, in NRZ-L coding, the synchronization and clock information is lost whenever a long stream of zeros or ones is encountered. Clock regeneration is difficult in this case.

This encoding has a maximum rate of change which is nearly equal to half of the clock input (alternate 1's and 0's). NRZ-L requires comparatively lower bandwidth than the other schemes.

For a system to be ac coupled, the dc energy is eliminated from its power spectrum. Hence, magnetic recording systems

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or systems with transformer coupling have very less sensitivity to low frequency signal components and thence information gets lost. NRZ-L contains dc level therefore it can't be used in systems which cannot pass dc signals. NRZ-L is most commonly in digital logic circuits [3].

2.1.2 NRZ- Mark (NRZ-M):

When bits are represented by change in levels, then we refer it as differential coding. When level changes for mark points i.e. bit 1, and then we call it NRZ-Mark (NRZ-M). It means that on arrival of bit '1' at input, the polarity of the signals changes and no change takes place for bit '0'.

The timing implementation can be extracted for the NRZ-M signal unless there are long periods which do not contain any level change. This corresponds to long stream of bit '0' in data. Long stream of ones is not a problem as changes occur at each mark point (1's).

It is somewhat similar to NRZ-L in terms of bandwidth utilization and dc level passing. However, as NRZ-M is independent of absolute level, therefore, receiver simply needs to know the level changes, which is an advantage in phase shift keying.

This type of encoding is primarily used in magnetic tape recording.

2.1.3 NRZ- Space (NRZ-S):

When level changes for space points i.e. bit '0', and then it is referred as NRZ-Space (NRZ-S). It means that on arrival of bit '0' at input, the polarity of the signals changes and no change takes place for bit '1'. NRZ-S is, in a way, a complement of NRZ-M. A '1' or mark is represented by no change in level and a '0' or space is represented by a change in level i.e. level changes from +V to 0 or vice versa.

Like NRZ-M, the bandwidth requirements and passing of Dc level is same as that for NRZ-L. Also if there are long streams of '1' in data, there is no level change in NRZ-S waveform and clock regeneration becomes difficult.

2.2 Return to Zero (RZ):

This type of encoding scheme incorporates signal whose value returns to zero at time $T_b/2$ (i.e. half the bit period). RZ codes (Unipolar, Bipolar and AMI) are widely used in baseband data transmission and also in magnetic recordings.

2.2.1RZ-Unipolar:

The RZ unipolar scheme may be implemented by representing bit '1' by the signal:

$$A_1(t) = \begin{matrix} +V,\ 0 \le t \le T_b/2 \\ 0,\ T_b/2 \le t \le T_b \end{matrix} \quad (4)$$

And bit '0' by the signal:

$$A_0(t) = 0,\ 0 \le t \le T_b \quad (5)$$

It has rising and falling transition for each data 1, therefore, the number of transitions increases. As a result, clock regeneration is simpler than NRZ scheme. This type of coding is not preferable if long stream of zeros occurs.

When a string of data '1' is transmitted, the maximum signal frequency of RZ signal occurs that implies the bandwidth. It is similar as sending two logic levels in a single clock period. Therein, the signal frequency is equal to the clock rate. It means RZ requires twice bandwidth as used in NRZ scheme. It does not have error detecting capability.

Passing of DC-level is a problem in RZ waveform i.e. systems that do not allow DC levels to pass, that results in information loss in RZ signals [4].

2.2.2RZ- Bipolar:

In long range transmission, stream of zeros can create synchronization problems. The general RZ-Bipolar has the following representation:

$$A_1(t) = \begin{matrix} +V,\ 0 \le t \le T_b/2 \\ 0,\ T_b/2 \le t \le T_b \end{matrix} \quad (6)$$

$$A_0(t) = \begin{matrix} -V,\ 0 \le t \le T_b/2 \\ 0,\ T_b/2 \le t \le T_b \end{matrix} \quad (7)$$

This is a three level code i.e. +V level for denoting data '1', - V level for denoting data bit '0', and level zero as the signal is RZ format (i.e. at $T_b/2$ it returns to 0).

Maximum signal frequency is same as the clock frequency. Thus, bandwidth requirement for RZ-Bipolar is double to that of NRZ and same as RZ-Unipolar and Biphase codes.

One of the most important advantages of RZ-Bipolar is that timing information is very easy to obtain. There is no loss of synchronization irrespective of data bits. However, due to the generation of three levels, the transmitter complexity increases.

DC level passing is dependent on the data bits. In a time frame which contains equal number of 1's and 0's, the DC level is null. But, if the number of bits is unbalanced, there exists a non-zero DC level.

The decoder design for this encoding scheme is easy. It requires a comparator with reference voltage set to zero volts.

2.2.3 RZ-Alternate Mark Inversion (RZ-AMI):

It is a code which contains positive and negative pulses of equal magnitude (i.e. +A and –A) alternatively to represent symbol '1'. For representation of bit '0', zero amplitude is used.

For RZ-AMI, the symbols can be defined by

$$A_1(t) = \begin{matrix} +V,\ 0 \le t \le T_b/2 \\ 0,\ T_b/2 \le t \le T_b \end{matrix} \quad (8)$$

$$\text{or } A_1(t) = \begin{matrix} -V,\ 0 \le t \le T_b/2 \\ 0,\ T_b/2 \le t \le T_b \end{matrix} \quad (9)$$

$$A_0(t) = 0,\ 0 \le t \le T_b \quad (10)$$

The signal returns to zero at time $T_b/2$ for each bit '1'. Due to alternative nature of bit '1', the clock synchronization problem is less as compared to the NRZ technique.

Long string of zeros implies null level in the output waveform which may cause the receiver to step out of

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synchronization. The generation of three levels makes the transmitter design complex.

AMI codes are independent of DC level because bit '1' is represented by alternative levels of equal amplitudes and different polarity. Hence, AC-coupled communication systems can easily employ RZ-AMI coding [5].

Transmission rate is equal to two transitions per period (as it is RZ) in case of a string of 1's. Thus, the bandwidth of RZ-AMI is twice that of NRZ codes.

The advantage of AMI is quoted in case where if noise corrupts the data bit '1' (such that it acquires the same polarity as the previous '1' bit), the coding rule will be violated. Thence, transmitter is required to re-send the string. In this way, the transmission reliability is increased in AMI and it finds wide application in telecommunication systems.

2.3 Biphase Coding:

The Biphase coding technique contains at least one transmission per bit interval irrespective of the input data. Therefore, its maximum frequency is same as the data clock rate. The required bandwidth is same as RZ codes and is double of NRZ codes. It finds application in magnetic recording systems, satellite telemetry links and optical communication [6].

2.3.1 Biphase Level Coding:

This coding is also referred as the **Manchester Coding.** In this, bit '1' is represented by a pulse in the first half of the clock period whereas bit '0' is represented by a pulse in the second half of the clock period.

$$A_1(t) = \begin{cases} +V, & 0 \le t \le T_b/2 \\ -V, & T_b/2 \le t \le T_b \end{cases} \quad (11)$$

$$A_0(t) = \begin{cases} -V, & 0 \le t \le T_b/2 \\ +V, & T_b/2 \le t \le T_b \end{cases} \quad (12)$$

Bit '0': Bit '1':

Fig.1 Representation of '1' and '0' bits in Biphase-L

Biphase code has high level for half of each bit interval and opposite polarity (low) for second half, irrespective of data. Therefore DC level becomes null. As a result, it can be used in AC coupled circuits.

There are many transitions in the Biphase coded waveform which make clock recovery easy [7].

2.3.2 Biphase Mark Coding:

In this coding scheme, a transition occurs at the beginning of every bit interval. A '1' is represented by a second transition one-half bit interval later (i.e. at $T_b/2$); whereas a zero is represented by no second transition [8].

Bandwidth requirements and passing of DC level is somewhat similar to Biphase-L. Clock regeneration is easier than Biphase-L. This is because at each positive edge of the clock, a transition certainly occurs in Biphase-M encoding.

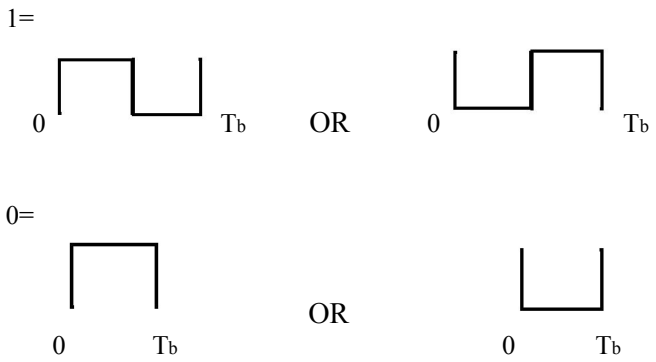

Fig.2 Representation of '1' and '0' bits in Biphase-M

2.3.3 Biphase Space Coding:

Its operation is complementary to that of Biphase-M. In Biphase-S, a transition occurs at the beginning of every bit interval. A '0' bit is represented by a second transition at one-half bit interval (at $T_b/2$). On other hand, bit '1' does not have a second transition within a single clock pulse.

Biphase-S shares all characteristics (bandwidth, clock recovery, and DC level passing) similar to Biphase-M.

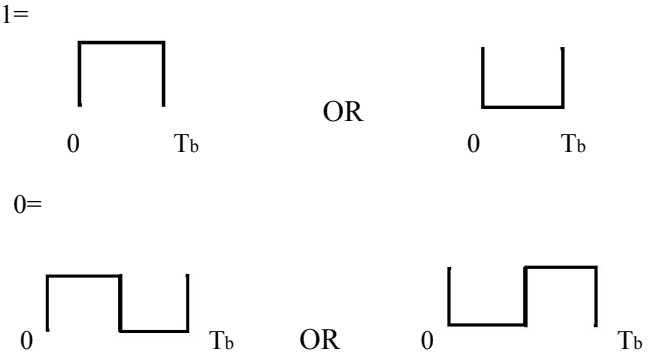

Fig.3 Representation of '1 and '0' bits in Biphase-S

Commonly, Line Coding schemes are used for digital data transport, digital baseband modulation or digital baseband transmission methods.

In coherence with the above discussion regarding **Line Coding** schemes, there are subtle differences amongst them which can be summarized and observed in the following Table 1 [9].

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Table 1 Comments for different Line Coding schemes

Signal	Comments
NRZ-L	Not Return to Zero Level. This is the standard positive logic signal format used in digital circuits. 1 forces a high level 0 forces a low level
NRZ-M	Not Return to Zero Mark 1 forces a transition 0 does nothing
NRZ-S	Not Return to Zero Space 1 does nothing 0 forces a transition
RZ-Unipolar	Return to zero 1 goes high for half the bit period 0 does nothing
RZ-Bipolar	There is always a transition in the middle of a bit period. 1 forces a positive pulse for half the bit period 0 forces a negative pulse for half the bit period
RZ-AMI	The positive and negative pulses alternate. 1 forces a positive or negative pulse for half the bit period 0 does nothing
Biphase-L	Manchester. Two consecutive bits of the same type force a transition at the beginning of a bit period. 1 forces a negative transition in the middle of the bit 0 forces a positive transition in the middle of the bit
Biphase-M	There is always a transition at the beginning of a bit period. 1 forces a transition in the middle of the bit 0 does nothing
Biphase-S	There is always a transition at the beginning of a bit period. 1 does nothing 0 forces a transition in the middle of the bit

3. Comparison Of Software Approach And Conventional Trainers

The proposed project has some noteworthy advantages when observed in comparison with the conventionally used electronic trainers. Some of them have been mentioned below:

1. Understanding the software is more convenient. It can be simulated according to the requirements of the programmer.
2. Many new coding schemes can be devised and tested on the **Verilog**, just merely with the help of code. Not all coding schemes are formulated directly on the hardware trainers. Rather they ought to be first verified on the software platform.
3. The trainer trainers act just like a black box. A learner is not aware of the internal connections and circuits and also, how the output is being generated. Whereas, the software approach requires programmer to first understand the code and then simulate it. This way, the software approach is more learning-oriented.
4. The hardware problems are a big deal while learning on the conventional trainer trainers as they are more wearisome. Moreover, a great deal of other hardware devices and accessories are also required like Data generator, DSO (Digital Storage Oscillation), connecting pins etc.
5. Software is portable and can be installed on almost all operating systems, while Hardware trainers are bulky, cumbersome and require professional advice for maintenance.
6. Many of the simulation tools for **Verilog** have an open access on the internet. This is a merit over the costly hardware trainers.

4. Implementation Using Verilog

Abou-El-Azm has implemented **Line Coding** schemes on the electronic trainer kit wherein there is an obvious presence of errors during transmission. They have tried detecting and correcting errors by re-transmitting the data block; which on the whole, is time consuming and results in eventual loss of system's efficiency [10].

Hardware description language languages like **Verilog** and VHDL are used commonly for design and implementation of various digital systems. The choice of **Verilog** mainly adheres to ease of programming and global acceptability. So, we have devised and implemented the encoding schemes using a **Verilog** Code.
The **Line Coding** schemes that have been implemented are categorized in two types:

- Having two levels in the waveform
- Having three levels in the waveform

The first category consists of NRZ-L, NRZ-M, NRZ-S, RZ-Unipolar, Biphase-L, Biphase-M, and Biphase-S. All these signals are either having levels +V and 0 (like the NRZ and RZ schemes in Unipolar format); or +V and -V (like the Biphase codes).
As there are only two levels, therefore, only one bit is required for representation. +V level is represented by logic level '1' while other level is represented by logic level '0'.

The second category has only two schemes: RZ-Bipolar and RZ-AMI. Both have three levels which are +V, -V and 0. For representing the three levels we require at least two bits. The encoding scheme used is

- +V is represented by 01
- 0 is represented by 00
- -V is represented by 11

Amongst the three modeling styles in **Verilog**, the Behavioral style of modeling has been used. The data assignment statements have been used in '*always'* block to account for the level transitions at the positive and negative edge. From programming point of view, clock signal is important for synchronization because changes made to a signal depend on the edges of the clock signal. Two '*always'* blocks have been used in the **Verilog** code in which one is sensitive to the positive edge and other to its negative edge. The transitions that occur at the positive edge are included in the former '*always'* block and similarly, the changes that occur at the negative edge are included in the latter *'always'* block.

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5. RESULTS AND OBSERVATIONS

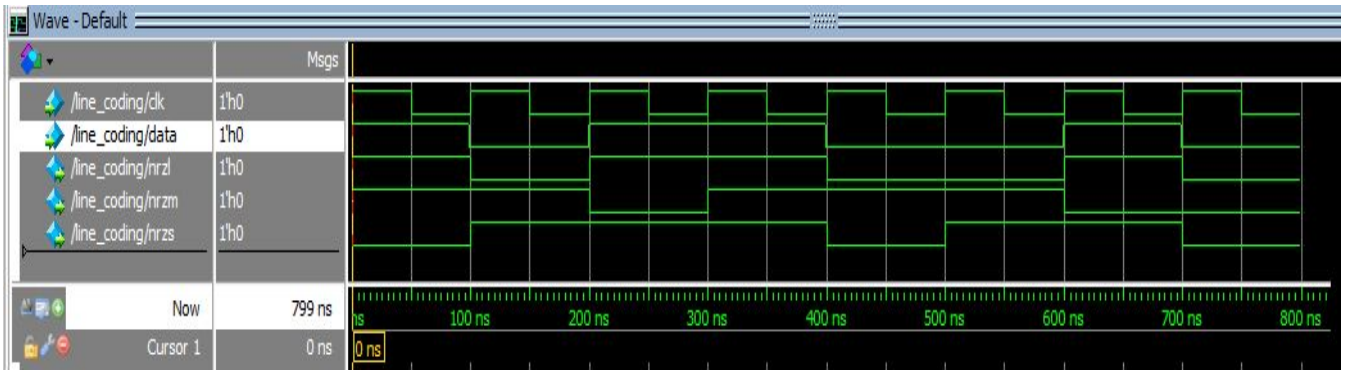

Fig.4 Screenshot of Waveforms after Simulating NRZ **Line Coding** schemes

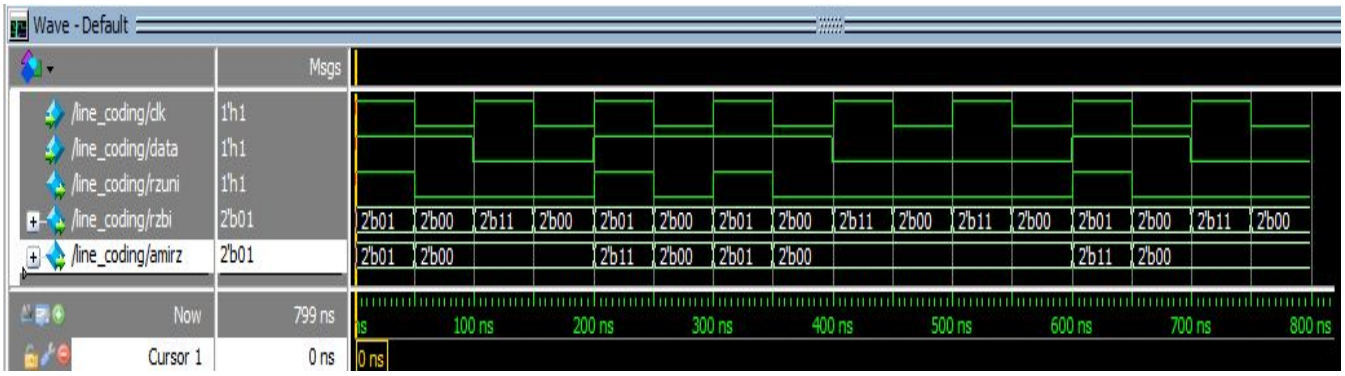

Fig. 5 Screenshot of Waveforms after simulating RZ **Line Coding** schemes

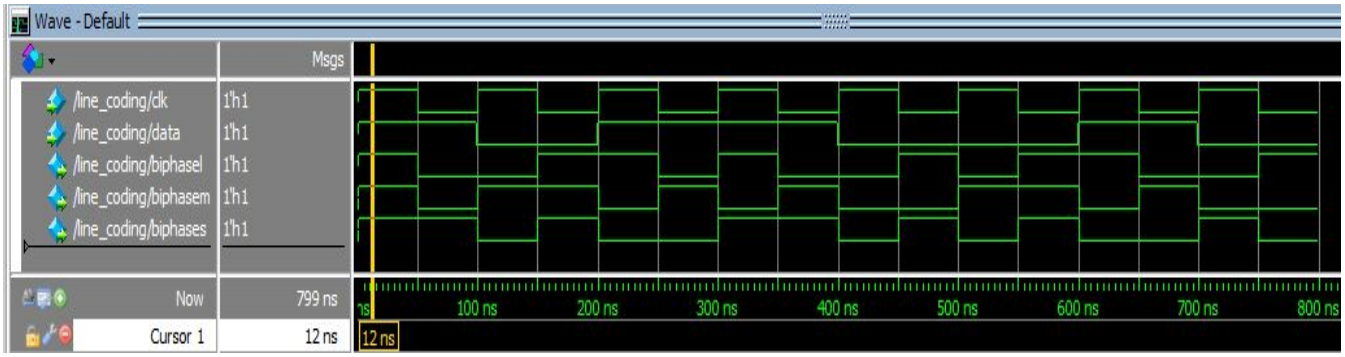

Fig. 6 Screenshot of Waveforms after simulating Biphase **Line Coding** schemes

The set of waveforms in Fig.4 shows the three NRZ (Non-Return to Zero) outputs along with the CLK (clock) and the ***DATA input signal (10110010).*** The data is sampled at positive edge of the clock only. It is observed that NRZ-L output changes with the data at each positive clock edge. Its waveform resembles the data itself. NRZ-M and NRZ-S are differential encoding schemes, which imply their value depends on the previous output as well. Thus, an initial 0 value is fed to the waveforms to obtain the first output.

In NRZ-M, a change in level takes place at data bit '1' which occur at time instants 0ns, 200ns, 300ns and 600ns. At other instants, no level changes takes place because of the presence of '0' bit.

In NRZ-S, a change in level takes place at data bit '0' which occur at time instants 100ns, 400ns, 500ns and 700ns. No level changes takes place at other instants because of the data bit '1'.

In Fig. 5, the waveforms displayed, are the result of simulation of RZ **Line Coding** schemes.

Here, the RZ-Unipolar takes the data value at clock's positive edge and holds it till half of the clock period. After this, the output returns to zero and remains at '0' value throughout the period.

The RZ-Bipolar is represented using two bits. Data '1' is denoted by bits '01' for first half interval and '00' for the second half (according to Return to Zero scheme). Similarly data '0' is denoted by bits '11' for first half interval and '00'

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for the second half. The last output wave here is of RZ-AMI (Alternate Mark Inversion). This is also represented by two bits per symbol. Data '0' is witnessed as a '00' for entire clock period. Data '1' first occurs as '01' for first half period and '00' in second half. The next immediate occurring bit'1' is formatted as '11' in first half period whereas '00' in second half. Thus, at instants 0ns and 300ns, data '1' is '01' and at instants 200ns and 600ns, data '1' is '11', thereby showing the alternative nature of transition.

The last set of waveforms is displayed in Fig.06, which shows the Biphase Codes.

The Biphase-Level code represents the data '1' by a high pulse in first half of clock period and data '0' by high pulse in second half of clock period. Thus, the Fig.01 in Section 2.3.1 represents the data bits '0' and '1'. Biphase-Mark and Biphase-Space are also differential codes. Initial value of 0 has been fed to them. At all positive edges, a transition in the level occurs.

For Biphase-Mark, another transition occurs at middle of clock period for data bit '1' (mark-point) i.e. at instants 50ns, 250ns, 350ns and 650ns. Likewise, for Biphase-Space, the transition occurs for data bit '0' at instants 150ns, 450ns, 550ns and 750ns.

Relative bandwidth utilization can also be compared using the above waveforms. All NRZ waveforms have a frequency which is half the clocking rate as there is at most one change within a bit period. In RZ codes and Biphase codes, the frequency is same as of the clock signal. This is so because transitions occur at most twice within a clock period. Thus, RZ and Biphase codes require double bandwidth than NRZ codes.

Ease of clock regeneration can also be observed using the same set of waveforms. In NRZ codes, RZ-Unipolar and RZ-AMI long stream of zeros or ones or both causes no level change in the coded waveform. Hence, there is a higher chance of synchronization loss. On the other hand, RZ bipolar and Biphase codes have ample number of transitions due to which clock regeneration is easy, and probably cause less synchronization loss.

This is a very efficient way of knowing how these coding schemes actually work as compared to the trainer trainers where the aforementioned bit by bit running procedure is not possible. Hence, software simulation gives a better insight to the students for analyzing the output with respect to varying data input.

7. Conclusion And Future Scope

In this project work, the various **Line Coding** schemes that are commonly employed in baseband modulation systems have been discussed. Their vivid characteristics have been studied. These different **Line Coding** schemes namely NRZ-L, NRZ-M, NRZ-S, RZ-Unipolar, RZ-Bipolar, RZ-AMI, Biphase-L, Biphase-M and Biphase-S, have been implemented and simulated on **Verilog**-HDL using the ModelSim tool of Mentor-Graphics. The methodology of implementation and analysis of the results have been specified. However as a limitation it may be said that a few coding schemes that are used now-a-days have not been discussed. This can be an extension to the project whereby synthesis and FPGA implementation of the system can be done. However, the merit of software based approach over electronic trainer trainers has been explicitly explained, which is the main purpose of the paper.

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Ankit Gupta is currently in the final year of Bachelors of Technology in Electronics and Communication Department of Bharati Vidyapeeth's College of Engineering, New Delhi. He is a gold medalist from Delhi Public School, RK Puram. He has been awarded twice by the Lambda Eta chapter of IEEE-HKN for academic excellence. The field of interest mainly includes subjects of electronics and communication discipline.

Gurashish Singh is currently in final year of Bachelors of Technology of Electronics and Communication Department in Bharati Vidyapeeth's College of Engineering. He is a student member of IEEE-HKN and has one published work in the field of Digital Image Processing. The research field of interest broadly includes electronics and communication discipline.

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