ISSN: 2278 – 7798
International Journal of Science, Engineering and Technology Research (IJSETR)
Volume 5, Issue 4, April 2016

# DESIGN AND IMPLEMENTATION OF LOW POWER EXPLICIT PULSE TRIGGERED FLIP-FLOPS

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*Abstract*— **In digital CMOS design, power consumption has been a major concern for the past several years. Advanced IC fabrication technology allows the use of nano-scaled devices; so the power dissipation becomes the major problem. Flip-flops are widely used in many sequential logic circuits such as registers, memory elements, counters, etc. These circuits are widely used in the implementation of VLSI chips. Pulse-triggered FF has a simple circuit which lowers the power consumption of the clock tree system. Explicit pulse triggered flip-flop provides high speed operation due to higher toggle rate. This paper presents an efficient dual edge pulse triggered Flip-flop (P-FF) design in terms of power consumption and speed. The Proposed design features pulse generator based on NAND-logic that can be shared among flip-flops to reduce power dissipation and a unique modified true single phase clock latch (TSPC) based on a signal feed-through scheme. The design successfully reduces the transistor sizes in discharging path. Adoption of Conditional discharging technique causes reduction in internal switching activity. The simulations are carried out in tanner tool software using 250nm CMOS Technology. The proposed design provides solution to the long discharging path problem resulting in improved speed and power performance.**

*Index Terms*— **flip-flop (FF), pulse triggered, dual edge, low power..**

## I. INTRODUCTION

Flip-Flops are basic storage and timing elements in VLSI circuits having a great impact on circuit power consumption as well as speed. The Power delay product of a Flip-flop can affect the systems overall performance. Hence the design in the Flip-flop with low power dissipation and low propagation delay improves the modern digital design to greater extent. Clock system consists of clock generator, storage element and clock distribution network. Thus Power consumed by the clock system is up to 30% to 60 % of the total power consumed by system. To overcome this problem a triggered based Flip-Flop is implemented.

Pulse-triggered FF (P-FF), because of its single-latch structure, is more popular than the conventional transmission gate (TG) and master–slave based FFs in high-speed applications. Besides the speed advantage, its circuit simplicity lowers the power consumption of the clock tree system. A P-FF consists of a pulse generator for strobe signals and a latch for data storage. If the triggering pulses are sufficiently narrow, the latch acts like an edge-triggered FF. Pulse-triggered flip-flops (P-FF) are characterized by an uncomplicated structure, negative setup time; soft edge and higher toggle rate giving improved performance over traditional master slave flip flop. P-FF has less number of clocked transistors. Pulse triggered flip-flops can be static, semi-static, dynamic or semi-dynamic.

PF-FFs, in terms of pulse generation, can be classified as an implicit or an explicit type. In an implicit type P-FF, the pulse generator is part of the latch design and no explicit pulse signals are generated. In an explicit type P-FF, the pulse generator and the latch are separate. Without generating pulse signals explicitly, implicit type P-FFs are in general more power-economical. However, they suffer from a longer discharging path, which leads to inferior timing characteristics. Explicit pulse generation, on the contrary, incurs more power consumption but the logic separation from the latch design gives the FF design a unique speed advantage. Its power consumption and the circuit complexity

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can be effectively reduced if one pulse generator is shares a group of FFs (e.g., an *n*-bit register). In this brief, we will thus focus on the explicit type P-FF designs only.

In this paper we present a low power and high performance Dual edge explicit pulse triggered flip-flop design. Here the internal node of the latch design is feed directly with input signal to fasten the data transition. A simple pass transistor is introduced to implement the mechanism which provides extra signal driving .when it is combined with pulse generation circuitry, gives enhanced speed and PDP performances. Use of dual edge triggering along with extra pull up NMOS transistor acts as a current limiter by passing the current only when clock is enabled resulting in lower power consumption in a circuit.

## II.CONVENTIONAL EXPLICIT TYPE P-FF DESIGNS

Explicit Pulse triggered Flip-Flop made up of Pulse generator for generating the pulse explicitly and a Latch network .Pulse generator circuit generates a short pulse around the rising (or falling) edge of the clock. This short pulse is given as clock input to a latch. Thus in this short window, Sampling of latch is done. To provide a fine comparison there are few existing designs are discussed

### A. Explicit-Pulse Data-Close-to-Output (ep-DCO) Flip Flop

Due to its semi-dynamic true-single-phase clock (TSPC) structured latch, it is considered to be the fastest FF. The pulse width is determined by delay of three inverters. Fig 1 shows the circuit diagram of ep-DCO Flip Flop. Explicit Data Close to output Flip-Flop suffers from large switching power dissipation problem due to discharging of internal node on each rising edge of clock whenever it has static input 1 case. This flip-flop does not produce any useful operation at internal node resulting in more power consumption.

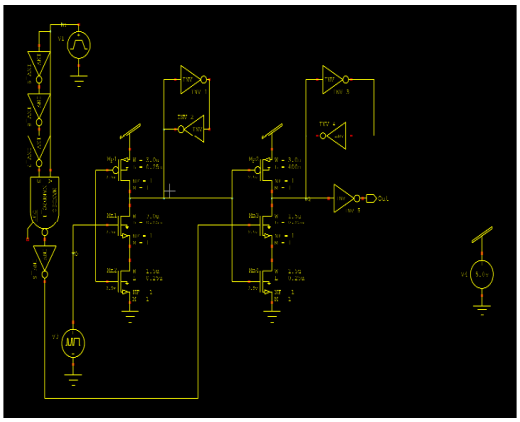

**Fig 1: schematic diagram of ep-DCO Flip Flop**

### B. Conditional Discharge Flip-flop (CDFF)

Conditional discharge mechanism is introduced to reduce power dissipation. An extra NMOS_5 transistor is employed which is controlled by the output feedback signal Qfdbk. Fig 2 shows the circuit diagram of CD Flip-Flop. Thus if the input data remains "1" no discharge occurs. But this design Suffers from worst case delay caused by longer discharging path. Keeper-logic for internal node is simplified by having only inverter and a pull up pMOS transistor.

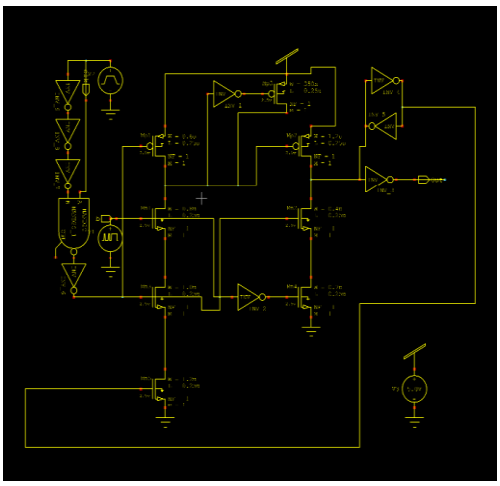

**Fig 2: schematic diagram of CD Flip Flop**

### C. Static Conditional Discharge Flip-flop (S-CDFF)

S-CDFF uses static latch structure and thus differs from the CDFF. It doesn't consist of periodical pre charges of internal node. Fig 3 shows the schematic diagram of S-CD Flip Flop. It is having a longer data-to-Q delay as compared to CDFF design. The three transistors NMOS_1- NMOS_2 - NMOS_5 constitutes a discharging path which results in worst case delay. A larger data-to-Q (D-to-Q) delay is exhibited by S-CDFF design as compared to the CDFF design.

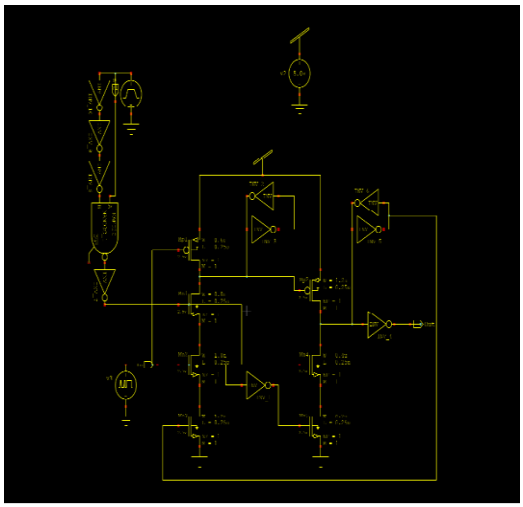

**Fig 3: schematic diagram of S-CD Flip Flop**

D. **Modified Hybrid latch Flip-flop (MHLFF)**

To overcome worst case delay problem caused by discharging path consist of three stacked transistor MHLFF is introduced**.** Fig 4 shows the circuit diagram of MHLFF. In this flip flop the keeper logic at internal node is removed. Though, this circuit is simple, it encounters two drawbacks. MHLFF drawback is that internal node x becomes floating in cases when output Q is „1"and input Data also equal to"1" resulting in extra dc power. A long 0 to 1 delay is expected since the node *X* is not pre discharged.

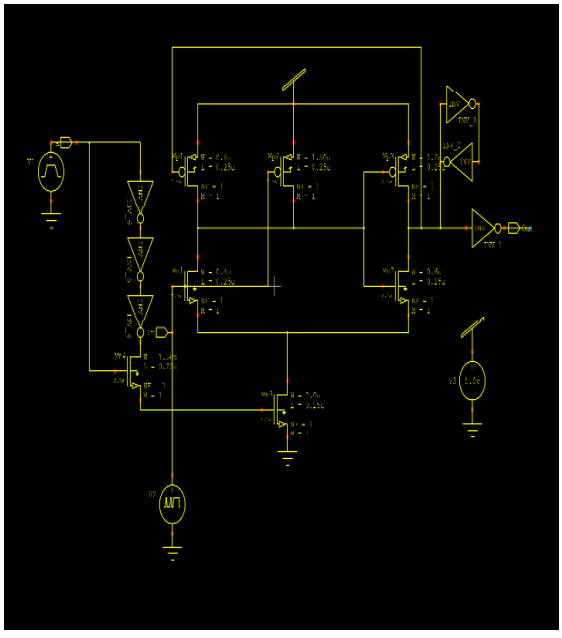

**Fig 4: schematic diagram of MHL Flip Flop**

III.PROPOSED PULSE TRIGGERED FLIP-FLOP

By studying the various conventional type flip-flops it is observed that there are some drawbacks regarding these flip-flops as belows:

- Power consumption at the internal node is high.
- Glitches appear at the output that would cause noise problem.
- Discharging occurs on every rising edge of the clock.
- Large switching power dissipation.
- Delay caused by a discharging of stacked transistors.
- Longer Data-to-Q (D-to-Q) delay during „0" to „1" transitions.
- Internal node becomes floating when output and input Data both are equal to 1.

To overcome the above drawbacks we implemented pulse triggered flip-flop that avoids switching at an internal node, improves the "0" to "1" delay and reduces the difference between the rise time and the fall time. The proposed Flip Flop circuit diagram is shown in fig 5.

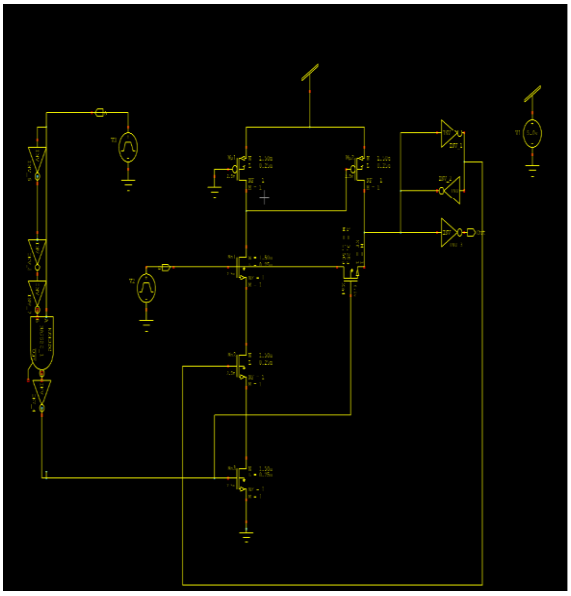

**Fig 5: Schematic diagram of proposed Flip Flop**

**IV. SIMULATION RESULTS**

ALL THE CONVENTIONAL PULSE TRIGGERED FLIP-FLOP MENTIONED IN FIG 1,2,3,4 PROPOSED MODEL DESCRIBED IN FIG 5 WERE ANALYSED BY USING TANNER EDA 250NM. THE WAVE FORM OF THE PROPOSED FLIP FLOP AS SHOWN IN THE FIGURE 6.AFTER SIMULATION DELAY,NUMBER OF TRANSISTORS AND POWER IS LESS COMPARED TO EXISTING FLIP FLOP THIS IS SHOWN IN TABLE 1.

| Parameter | Ep-DCO | CD-FF | S-CDFF | MHLFF | Proposed |
|---|---|---|---|---|---|
| No of Transistors | 28 | 30 | 31 | 19 | 24 |
| Delay in ps | 120 | 130 | 140 | 175 | 110 |
| Average Power Consumption | 9.2mW | 7.43µW | 7.11mW | 0.481 mW | 3.12 µW |

**Table 1: comparison of various Flip Flops in terms of no of Transistors, Delay and Power consumption**

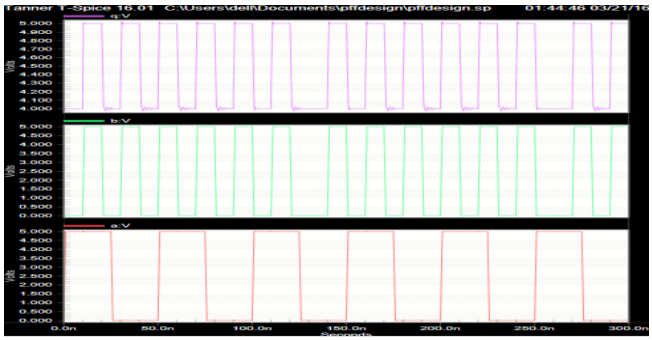

**Fig 6: output wave form**

## v. Conclusion

Extensive post layout simulations were conducted on the existing type of implicit and explicit pulse triggered flip-flops using 250-nm CMOS process. From the simulations MHLFF exhibited good speed performance but the power dissipation is very high. The proposed design support the claim in both speed and power performances. A new pulse triggered FF with an explicit pulse generator is designed using CMOS NAND logic for the pulse generation. The simulation results obtained prove that it is far better than the other design shown in this paper and many other FF's. The power reduced is almost 50% when the pulse generator is shared with number of flip-flops when compared with the all above circuits. It has also produced a better D-Q delay and reduced the overall transistor count.

## REFERENCES

[1] Jin-Fa Lin, "Low-Power Pulse-Triggered Flip-Flop Design Based on a Signal Feed-Through Scheme," IEEE Transactions On Very Large Scale Integration (Vlsi) Systems, Vol. 22, No. 1, January 2014.

[2] H. Kawaguchi and T. Sakurai, "A reduced clock-swing flip-flop (RCSFF)for 63% power reduction," *IEEE J. Solid-State Circuits*, vol. 33, no. 5,pp. 807–811, May 1998.

[3] K. Chen, "A 77% energy saving 22-transistor single phase clocking D flip-flop with adoptive-coupling configuration in 40 nm CMOS," in *Proc. IEEE Int. Solid-State Circuits Conf.*, Nov. 2011, pp. 338–339.

[4] E. Consoli, M. Alioto, G. Palumbo, and J. Rabaey, "Conditional push-pull pulsed latch with 726 flops energy delay product in 65 nm CMOS," in *Proc. IEEE Int. Solid-State Circuits Conf.*, Feb. 2012, pp. 482–483.

[5] H. Partovi, R. Burd, U. Salim, F.Weber, L. DiGregorio, and D.Draper, "Flow-through latch and edge-triggered flip-flop hybrid elements,"in *Proc. IEEE Int. Solid-State Circuits Conf.*, Feb. 1996,pp. 138–139.

[6] F. Klass, C. Amir, A. Das, K. Aingaran, C. Truong, R. Wang, A. Mehta,R. Heald, and G. Yee, "A new family of semi-dynamic and dynamic flip-flops with embedded logic for high-performance processors," *IEEE J. Solid-State Circuits*, vol. 34, no. 5, pp. 712–716, May 1999.

[7] V. Stojanovic and V. Oklobdzija, "Comparative analysis of master slave latches and flip-flops for high-performance and low-power systems, "*IEEE J. Solid-State Circuits*, vol. 34, no. 4, pp. 536–548,Apr. 1999.

[8] J. Tschanz, S. Narendra, Z. Chen, S. Borkar, M. Sachdev, and V. De,"Comparative delay and energy of single edge-triggered and dual edge triggered pulsed flip-flops for high-performance microprocessors," in *Proc. ISPLED*, 2001, pp. 207–212.