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A REVIEW PAPER ON DIFFERENT EXISTING 2D DISCRETE COSINE SYSTEM

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***Abstract*-The recent time witnesses a tremendous need for high performance digital signal Processing (DSP) systems for high end emerging applications like HD-TV, medical imaging, satellite communication, 3G mobile technologies etc. For all these applications, the sources of data are video signals. For transmission of video signals significant amount of bandwidth required. Since the captured video data contain huge amount of redundant data, there is an opportunity for video data compression keeping the picture quality intact. DCT is a well known technique used in video or image compression. DCT algorithms are computation intensive and involve large number of multiplication and addition operations. Therefore, with the increase in number of length of the DCT, the number of multiplication and addition operations also increase leading to larger chip area and performance degradation. The primary aspect of the 2-D DCT computation is to compute the DCT coefficients, where a large number of mathematical computations are required.**

Keywords: DSP, DCT, 2-D DCT , DCT Coefficient, Video/Image Compression, computation intensive

I. INTRODUCTION

In classical lossy image compression techniques where transform coding is used, the transform is applied to non-overlapping sub-blocks of the image. This is in particular the case with the lossy modes of JPEG, where a 2D discrete cosine transform (DCT) is applied to non-overlapping 8 * 8 sub-blocks. Yet it is standard practice to use windowed overlap-and-add transforms, specifically the windowed modified DCT (MDCT), in audio compression techniques. The reason for doing so is to mitigate undesirable edge effects, namely the contamination of frequency components caused by the resulting discontinuities at the boundaries of transform blocks.

While modern transform coding based image compression algorithms (such as JPEG2000) have eliminated this problem by applying wavelet transforms to entire images, one is still faced with the question: What if we were to do the same in image compression as is done in audio compression, replacing the standard DCT with a windowed MDCT?

MDCT is one of the core units in JPEG XR which consumes more time in compression unit. Apart from this the previous works are mainly focused on accurate analysis and efficient estimations of frequency of advance audio applications. There is no efficient and swift unit for MDCT in JPEG XR. The main theme of the work is to minimize the simulation time for a compressor unit using the bit depth of the image with a scalable coefficients with a varying cost of quality of Image. For optimal quantization we adapt and apply an algorithm, designed for JPEG, to MJPEG

With the increasing capacity in today's hardware systems enabled by technology scaling, image processing algorithms with substantially higher complexity can be implemented on a single chip enabling real-time performance. Combined with the demand for low power consumption or larger resolution seen in many applications such as mobile devices and HDTV, new design methodologies and hardware architectures are constantly called for to bridge the gap between designer's productivity and what the technology can offer.

Imaging and video applications are one of the fastest growing sectors of the market today. Typical application areas include e.g. medical imaging, HDTV, digital cameras, set-top boxes, and machine vision and security surveillance. As the evolution in these applications progresses, the demands for technology innovations tend to grow rapidly over the years. Driven by the consumer electronics market, new emerging standards along with increasing requirements on system performance imposes great challenges on today's imaging and video product development. To meet with the constantly improved system performance measured in, e.g., resolution, throughput, robustness, power consumption and digital convergence (where a wide range of terminal devices must process multimedia data streams including video, audio, GPS, cellular, etc.), ne design methodologies and hardware accelerator architectures are constantly called for in the hardware implementation of such systems with real-time processing power.

The construction of a typical real-time imaging or video embedded system is usually an integration of a range of electronic devices, e.g. image acquisition device, signal processing units, memories, and a display. Driven by the market demand to have faster, smarter, smaller and more interconnected products, designers are under greater pressure to make decisions on selecting the appropriate technologies in each one of the devices among many of the alternatives. Trade-offs are constantly made concerning e.g. cost, speed, power, and configurability.

In a brief overview of the varied alternative technologies is given along with elaborations on the plus and minus sides of each of the technologies, which motivates the decisions made on the selection of the right architecture for each of the devices used in the projects.

Digital image processing has a wide range of application related to our day to day life such as remote sensing, space exploration and medical imaging applications etc. The image scaling is an important concept in the digital image processing and adopted in electronic devices such as digital camera, mobile phone, tablet PC, digital video recorders, and digital photo frames etc.

Image scaling is widely used in many fields ranging from consumer electronics to medical imaging. It is indispensable when the resolution of an image generated by a source device is different from the screen resolution of a target display. For example, we have to enlarge images to fit HDTV or to scale them down to fit the mini-size portable LCD panel. The most simple and widely used scaling methods are the nearest neighbor and bilinear techniques. According to the required computations and memory space, we can divide the existing scaling methods into two classes: lower complexity and higher complexity scaling techniques. The complexity of the former is very low and comparable to conventional bilinear method.

II. LITERATURE REVIEW

Yanchang Liu and Wei Zheng in "Research in a Fast DCT Algorithm Based on JPEG" presented a fast discrete cosine transform(DCT) algorithm which was implemented in image compression based on JPEG would be presented. Firstly, based on the application of DCT in image compression, several fast DCT algorithms were analyzed first, then the efficiency fast DCT algorithm, binary DCT, was demonstrated. According to the experiment result., the performance of binary DCT in JPEG encoder could be comparable with the traditional JPEG encoder. In the algorithm, all coefficients are in binary and all multiplications were replaced by shifting and addition operations which are easier and faster achieved by hardware and software. The complexity of transform was reduced by the binary DCT algorithm. Binary DCT can be implemented with 16-bit data bus, making it very suitable for low-lost, fast and low-power multimedia applications.

Yuebing Jiang and Marrios Pattichis' "A Dynamically Reconfigurable DCT Architecture for Maximum Image Quality Subject to Dynamic Power and Bit rate Constraints" has proposed a dynamically reconfigurable DCT architecture system is proposed that can be used to maximize image quality while meeting real-time constraints on bit rate and dynamic power. Optimal DCT architectures are computed using dynamic partial reconfiguration and are generated by varying both the number of non-zero DCT coefficients and the quality factor from the quantization table

Jongsun Park, Jung Hwan Choi, and Kaushik Roy in "Dynamic Bit-Width Adaptation in DCT: An Approach to Trade Off Image Quality and Computation Energy" have proposed variable bit precision DCT algorithm can be efficiently implemented using carry save adder trees. The reconfigurable DCT architecture can achieve power savings ranging from 36% to 75% compared to normal operation at the expense of minor image quality degradation.

A low power, reconfigurable DCT architecturemto allow efficient tradeoff between image quality and computation energy. The DCT architecture uses the dynamic bit-width adaptation, where operand bit-widths are changed according to image quality and/or power consumption requirements. Different tradeoff levels are specified and the proposed DCT architecture can be dynamically reconfigured from one trade off level to another. The proposed reconfigurable DCT architecture leads to 36% power savings with little degradation in image quality (0.61 dB). With the proposed architecture, larger computation power savings can be achieved at the expense of additional degradation in image quality.
Jongsun Park, Soonkeon Kwon, Kaushik Roy "Low Power Reconfigurable DCT Design Based On Sharing Multiplication" has proposed a low-power reconfigurable DCT architecture, which is based on computation sharing multiplier (CSHM). CSHM specifically targets computation re-use in vector-scalar products and is effectively used in our OCT implementation. A low power reconfigurable OCT architecture is exploited by making a trade-off between image quality and power consumption. The proposed OCT architecture was implemented using 0.35" technology. The experimental results show that

reconfigurable OCT using CSHM can improve power consumption by 40 % without noticeable image quality degradation. Using the CSHM algorithm, the DCT matrix multiplication can be significantly simplified to add and shift operations of alphabets multiplied by input x. Furthermore, by changing the number of alphabets in the pre computer bank, trade-off between image quality and power consumption is exploited. Based on the trade off, we propose the reconfigurable DCT architecture, which works in two different modes. Consequently, the reconfigurable OCT in low power mode leads to 40 % power savings without seriously compromising the image quality. The idea presented in this paper can assist design of DSP algorithms and their implementation for low power application.

Bhuvanan Kaliannan, Vijaya Sankara Rao Pasupureddi "Implementation of a Charge Redistribution Based 2-D DCT Architecture for Wireless Capsule Endoscopy" proposes a charge redistribution based CMOS implementation of an ultra low power 2-D DCT architecture for wireless capsule endoscopy applications. The ultra low power operation of the proposed system is highly desirable in wireless capsule endoscopy applications, where power efficiency is critical. This technique is also suitable for other low power applications where moderate accuracy is required. In this implementation, the basic principle of charge redistribution is used to perform the low power multiply and accumulate(MAC) operation in the DCT kernel. The DCT frequency components are computed parallely, making the transform to operate at high speed. a 2-D DCT architecture for high speed, ultra low power wireless capsule endoscopy applications has been proposed. The principle of charge redistribution has been used to realize the DCT coefficients. The absence of active components in the DCT kernel has enabled low power operation of the system. The developed charge mode DCT technique can also be used in other applications, where power performance is critical.

Emre Y., Chakrabarti C., "energy and quality aware multimedia signal processing" proposed techniques to reduce energy with minimum degradation in system performance for multimedia signal processing algorithm. It provides survey of energy saving techniques such as those based on voltage scaling reducing number of computation and reducing dynamic range. While these reduces energy these introduces error that affect the performance quality to compensate for these errors, techniques that further reduce the energy consumption are presented. A combination of computation reduction for DCT shows on average 33-40% reduction in energy consumption while incurring 0.5-1.5 dB in PSNR.

"Process-Variation Resilient and Voltage-Scalable DCT Architecture for Robust Low-Power Computing" In this author deals with respect to parameter variations and low power operation typically impose contradictory requirements in terms of architecture design. It isolates the computation paths based on high energy and low energy contributing components. All coefficients of the 2-D DCT matrix do not affect the image quality in a similar manner. Analysis of the image shows around 85% or more energy is contained in the first 20 coefficients of the DCT matrix after the 2D-DCT operation. It allows supply voltage scaling (single supply) to trade-off power dissipation and image quality even under process parameter variations. To obtain power savings, it is necessary to skew the different path-lengths in the DCT computation.

III. RESEARCH GAPS

Error Resilient feature of Image Compression is not fully utilized in terms of, Optimized hardware, power requirement, Coefficient aware design, Optimization in JPEG architecture.

IV. FUTURE OBJECTIVE

Reducing the simulation time taken by JPEG unit. (DCT simulation time) To reduce the simulation time we adopt the error resilient technique in which the image quality at user end is decided as per the user. Minimizing the number of coefficient computations as per the accuracy level of end user. As stated above reducing the coefficient computation as per the user error resilient can reduce the computational time to compress an image. Minimizing number of matrix computation in DCT core of JPEG*(Algorithm level) Using algorithms and optimization techniques we can reduce the matrix computational time.

In the general overview of the JPEG process. The input image can be read by using imread function and then broken into 8x8 block of matrixes. The algorithm can be applied for gray scale by suitably using functions such as is gray functions. DCT is applied to each block on its both the rows and columns. Strassen's matrix multiplication algorithm is applied on the DCT matrix multiplication calculation. Each block is compressed by quantization. Suitably the quantization matrix is selected. They are standard matrices used in JPEG. The array of compression blocks that constitute the image is stored in a significantly reduced amount of space. The image is reconstructed through decompression using Inverse DCT.

V. APPLICATION

With the increasing capacity in today's hardware systems enabled by technology scaling, image processing algorithms with substantially higher complexity can be implemented on a single chip enabling real-time performance.
Combined with the demand for low power consumption or larger resolution seen in many applications such as mobile devices and HDTV signal processing has a wide range of application related to our day to day life such as remote sensing, space exploration and medical imaging applications etc.

The image scaling is an important concept in the digital image processing and adopted in electronic devices such as digital camera, mobile phone, tablet PC, digital video recorders, and digital photo frames etc.

VI. CONCLUSION

It is concluded that the existing systems can be improvised to provide an error resilient DCT architecture to compete the existing architecture and to Design, Implement & Validate DCT architecture on different standards using an appropriate image processing parameter. In this paper we study about the previous existing 2D DCT approaches and we found there are lots of issues which are related to algorithm & architecture level. So in this area there is lots of future scope where we can still make lots of improvement.

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