ISSN: 2278 – 7798
International Journal of Science, Engineering and Technology Research (IJSETR)
Volume 5, Issue 4, April 2016

DESIGN OF OPTIMIZED REVERSIBLE BCD ADDER USING REVERSIBLE LOGIC GATES

JAYAPRIYA.S NIRMALKUMAR.R ANU.P

***ABSTRACT*:Reversible logic has emerged as a possible low cost alternative to conventional logic in terms of speed, power consumption and computing capability. An adder block is a very basic and essential component for any processor and optimized design of these adders' results in efficient processors. In this work we propose optimized Binary adders and BCD adders. The adders designed in this work are optimized for Quantum cost, Delay and Area. A modified BCD adder is also proposed which removes redundancy in the circuit and acts as most efficient BCD adder. Here we explore the use of Negative control lines for detecting overflow logic of BCD adder which considerably reduces Quantum cost, delay and gate count which result in high speed BCD adder with optimized area which give way to lot of scope in the field of reversible computing.**

1 INTRODUCTION

Reversible logic has a great attention in the recent years due to their ability to reduce the power dissipation which plays the major role in low power VLSI design. It is used in wide applications in low power CMOS and Optical information processing, quantum computing,nano technology. Irreversible hardware computation results in energy dissipation due to the information loss. The heat generated due to the loss of one bit of information is very small at room temperature but when the number of bits is increases then in the circuits of high speed computational works the heat dissipated by them will affects the performance and results in the inefficiency of components. Reversible logic is the process of propogating the logical circuit together in leading and backward propogation.so it is called as bidirectional propogation. This means that reversible computations can provoke inputs from outputs and output from the input . A circuit is said to be reversible if the input vector can be individually recovered from the output vector and there will be one-to-one correspondence between its input and output assignments.

2 REVERSIBLE GATES

A reversible gate is an n-input and n-output (denoted by n × n) gate that produces a unique output pattern for each possible input pattern. In other words, reversible gates are circuits in which the number of outputs is equal to the number of inputs and there is a one-to-one correspondence between the vectors of inputs and outputs. Feynman gate is a 2*2 one through reversible gate as shown in figure 2.1. The input vector is I(A, B) and the output vector is O(P, Q). The outputs are defined by P=A, Q=A⊕B. Quantum cost of a Feynman gate is 1. Feynman Gate (FG) can be used as a copying gate. Since a fan-out is not allowed in reversible logic, this gate is useful for duplication of the required outputs.

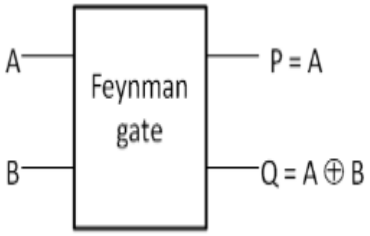

Figure 2.1 feynman gate

The 3*3 Toffoli gate has the input vector I (A, B, C) and the output vector isO(P,Q,R). The outputs are defined by P=A, Q=B, R=AB⊕C. Quantum cost of a Toffoli gate is 5.

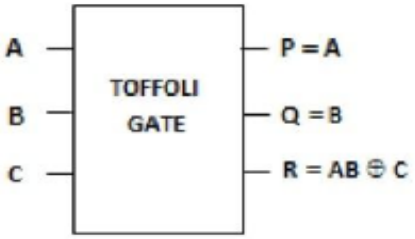

Figure 2.2 Toffoli gate

The 3*3 Fredkin gate has input vector I (A, B, C) and the output vector is O (P, Q, R). The output is defined by P=A, Q=A′B⊕AC and R=A′C⊕AB. Quantum cost of a Fredkin gate is 5.

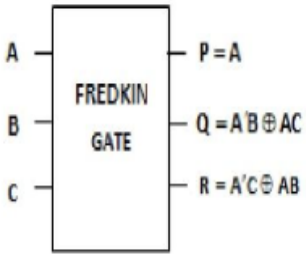

Figure 2.3 Fredkin gate

The 3*3 Peres gate has input vector I (A, B, C) and the output vector is O (P, Q,R). The output is defined by P = A, Q = A⊕Band R=AB⊕C. Quantum cost a Peres gate is 4. In the proposed design Peres gate is used because of its lowest quantum cost.

Figure 2.4 Peres gate

3 WHY LOW POWER DESIGN

During the desktop PC design era VLSI design efforts have focused primarily on optimizing speed to realize computationally intensive real-time functions such as video compression, gaming, graphics etc. As a result, we have semiconductor ICs that successfully integrated various complex signal processing modules and graphical processing units to meet our computation and entertainment demands. While these solutions have addressed the real-time problem, they have not addressed the increasing demand for portable operation, where mobile phone need to pack all this without consuming much power. The strict limitation on power dissipation in portable electronics applications such as smart phones and tablet computers must be met by the VLSI chip designer while still meeting the computational requirements. While wireless devices are rapidly making their way to the consumer electronics market, a key design constraint for portable operation namely the total power consumption of the device must be addressed. Reducing the total power consumption in such systems is important since it is desirable to maximize the run time with minimum requirements on size, battery life and weight allocated to batteries. So the most important factor to consider while designing SoC for portable devices is 'low power design'.The growing market of portable (e.g., cellular phones, gaming consoles, etc.), battery-powered electronic systems demands microelectronic circuits design with ultra low power dissipation. As the integration, size, and complexity of the chips continue to increase, the difficulty in providing adequate cooling might either add significant cost or limit the functionality of the computing systems which make use of those integrated circuits. As the technology node scales down to 65nm there is not much increase in dynamic power dissipation. However the static or leakage power is same as or exceeds the dynamic power beyond 65nm technology node. Hence the techniques to reduce power dissipation is not limited to dynamic power. Total Power dissipated in a CMOS circuit is sum total of dynamic power, short circuit power and static or leakage power. Design for low-power implies the ability to reduce all three components of power consumption in CMOS circuits during the development of a low power electronic product.

4 1-BIT REVERSIBLE FULL ADDER USING TOFFOLI GATE

4.1 POSITIVE CONTROLLED TOFFOLI GATE

An n*n Toffoli gate given in Fig 1.a, maps the input vector[nI,m, n3... nk] to the output vector [01,02,03...01<], where OJ=nj (for j=l, 2... k-l) andOk=nln2....nk-1 EBnk. The first (n-l) bits are called control lines and last bit is called target line. Here the target bit is toggled only when all control lines are I. The Toffoli gate is characterized by Quantum cost of 5 and with a delay of 5

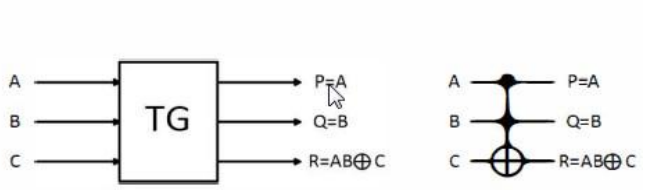

Fig. 1. a: Positive Controlled Toffoli gate (TG)
b: TG Symbol

4.2 NEGATIVE CONTROLLED TOFFOLI GATE

A negative controlled Toffoli gate has one or more negative control lines. In this case toggling happens at target bit if all negative control lines are at logic 0 and if any positive control, it should be at logic I. The Quantum Cost of Negative controlled Toffoli gate is 6 with a delay of M.

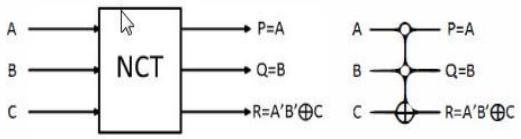

Fig. 2. a: Negative controlled Toffoli (NCT) gate
b: NCT symbol

5 PROPOSED DESIGN

5.1 1-BIT REVERSIBLE FULL ADDER

There are various variants of Toffoli gate. 2*2 Toffoli gate is generally called CNOT gate / Feynman gate. A 1-bitreversible full adder has

been designed using only n*n positive controlled Toffoli gates as shown in Fig 3. The proposed design is simple and has a gate count of 4 with 0 garbage output.

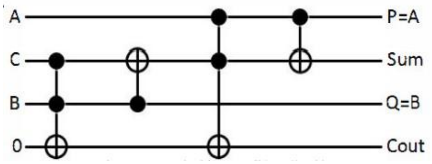

Fig 5.1:1-bit reversible full adder

5.2 DESIGN OF BCD ADDER USING TWO 4-BIT FULL ADDER

BCD codes makes calculation and analysis more simple in processor design. A BCD adder plays a major role in these designs. A conventional BCD adders are constructed using Full Adder circuit with an overflowing detector circuit. In this design we have proposed a 4-bit reversible BCD adder using proposed reversible full adder circuit (NAFA) and an overflow detector circuit as shown in Fig 4.3. The overflowing detector circuit has been designed using two 3*3 negative controlled Toffoli gates and a positive controlled Toffoli gate. The use of negative logic reduces the gate count and hence aids the requirement. In this design two reversible 4-bit full adders (NAFA) are used to realize the reversible BCD adder.

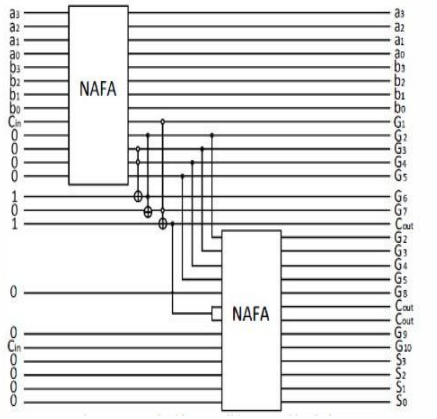

Fig 5.2:bcd adder

5.3 MODIFIED BCD ADDER

A BCD code consists of numbers from 0 to 9 and any value greater than the range is corrected by adding 6 (0 I 10) to the resulting value. There is a need to detect this overflow of the resulting value. Hence we have designed overflow logic using negative controlled Toffoli gate followed by a 4-bit reversible full adder to add 6 to the resulting value. But we need to add l's only for 2nd and 3rd bits. Hence we need only two I-bit adders to perform the same instead of 4-bit full adder as discussed in previous section. Hence we modified the previously proposed BCD adder design. A BCD code consists of numbers from 0 to 9 and any value greater than the range is corrected by adding 6 (0 I 10) to the resulting value. There is a need to detect this overflow of the resulting value. Hence we have designed overflow logic using negative controlled Toffoli gate followed by a 4-bit reversible full adder to add 6 to the resulting value. But we need to add l's only for 2nd and 3rd bits. Hence we need only two 1-bit adders to perform the same instead of 4-bit full adder as discussed in previous section. Hence we modified the previously proposed BCD adder design

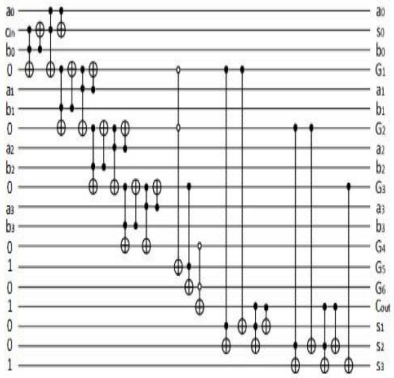

Fig 5.3:modified bcd adder

The modified BCD adder designed is much more efficient than proposed BCD adder (Design 1). For a 4-bit adder, the percentage improvement in quantum cost when compared to design I is 25.5% and also 21.25% improvement in delay. Hence it is much more efficient than the proposed design 1.

A binary coded decimal is a form of number system in which every four bits of a number is represented by its equivalent value. For example, a decimal number 45 is represented as 0100 0101 in BCD system. This makes things simple and facilitates the logic designer to understand the logic. While designing a combinational circuit using BCD logic, we may need to perform different operations on it such as addition, subtraction, etc.

6 APPLICATIONS

Reversible computing may have applications in computer security and transaction processing, but the main long-term benefit will be felt very well in those areas which require high energy efficiency, speed and performance .It include the area like

1. Low power CMOS.
2. Quantum computer.
3. Nanotechnology

4. Optical computing
5. Design of low power arithmetic and data path for digital signal processing (DSP).
6. Field Programmable Gate Arrays (FPGAs) in CMOS technology for extremely low power, high testability and self-repair

7 SIMULATIONS

7.1 1-BIT REVERSIBLE FULL ADDER

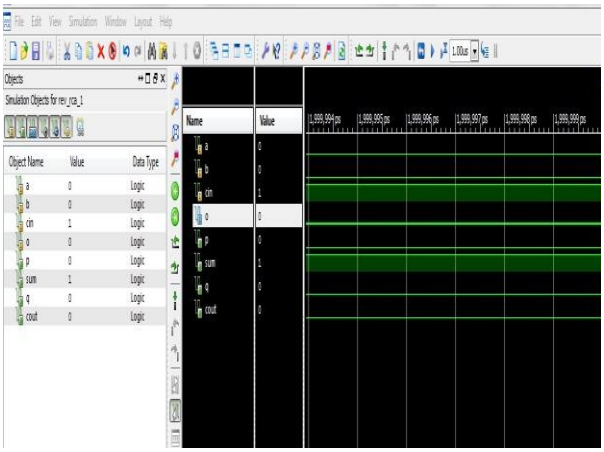

Fig 7.1: 1-Bit Full Adder

7.2 REVERSIBLE FULL ADDER

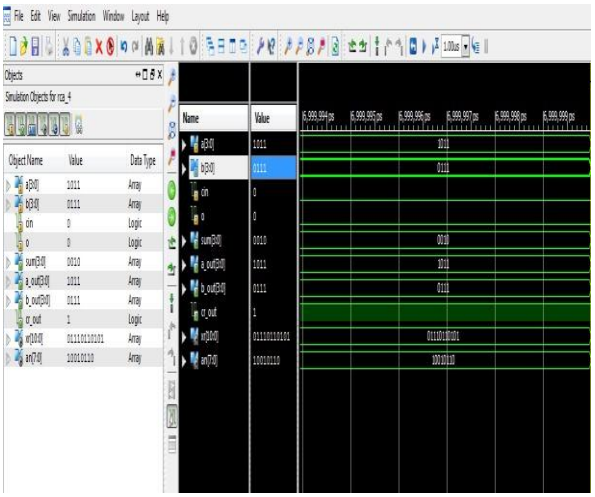

Fig 7.2 Reversible Full adder

7.3 REVERSIBLE BCD ADDER

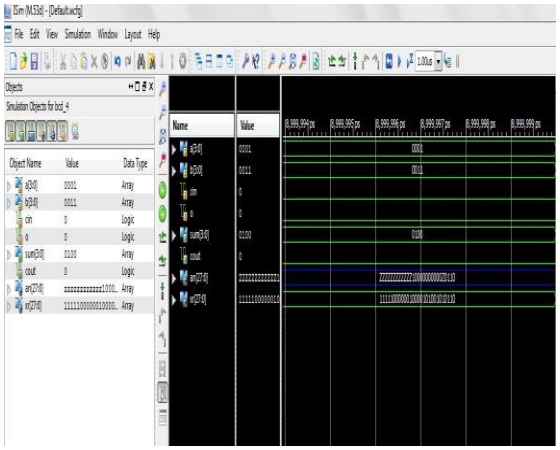

Fig 7.3: Reversible BCD Adder

8 CONCLUSION

We have presented an approach to the realize the multipurpose binary reversible gates. Such gates can be used in regular circuits realizing Boolean functions. In the same way it is possible to construct multiple-valued reversible gates having similar properties. we have proposed a reversible binary adder design with optimized quantum cost and delay compared to previous work in literature and using this adder, an optimized reversible BCD adder in terms of Quantum cost, delay and garbage outputs have been designed. All the designs are functionally verified using Xilinx ISE tool. The use of negative control lines in the design for detecting overflow logic of BCD adder has considerably reduced delay and gate count which result in high speed BCD adder with optimized area. Thus we conclude that the use of Negative control lines reduces the gate count and hence area, for specific signal processing which gave way to lot of scope in the field of reversible computing in near future.

REFERENCES

[1] R. Landauer, "Irreversibility and heat generation in the computationalprocess",IBM1. Res. Develop., vol. 5, pp. 183-191, 1961.
[2] C. H. Bennet, "Logical reversibility of computation", IBM 1. Res. Develop., vol. 17, no. 6, pp. 525- 532,1973.
[3] Vasudevan, Lala and Parkerson, "A Novel Approach for On-Line Testable Reversible Logic Circuit Design", Proceedings of the 13th Asian Test Symposium (ATS 2004).
[4] Polian and Hayes, "Advanced Modeling of Faults in Reversible Circuits", IEEE 978-1-4244-9556-6/10 2010
[5] B. Parhami, "Fault tolerant reversible circuits", in Proceedings of 4(jh Asimolar Con! Signals,

Systems, and Computers, Pacific Grove, CA, pp. 1726-1729, October 2006.
[6] Eleonora, Kamalika, Wille, Sengupta, Rahaman, Rolf, "Optimizing DDbased Synthesis of Reversible Circuits using Negative Control lines", IEEE, 978-1-4799-4558-0/14,2014
[7] Wille, Soeken, Nils, Rolf: "Exact Synthesis of Toffoli Gate Circuits with Negative Control Lines", IEEE 42nd International Symposium on Multiple Valued Logic, 2012.
[8] Rahman, Saiflil Islam, Zerina Begum, Hafiz, Mahmud, "Synthesis of Fault Tolerant Reversible Logic Circuits", IEEE, 978-1-4244-2587-7/09,2009.
[9] Kamalika, Gaurav, Wille, "Exploiting Negative Control Lines in the Optimization of Reversible Circuits", Springer- Verlag Berlin Heidelberg 2013.
[10] H. M.H. Babu and AR. Chowdhury. "Design of a compact reversible binary coded decimal adder circuit". Elsevier Jour. of Systems Architecture, 52:272-282, 2006.