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A Review Paper On High Speed Adder Logic

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***Abstract*— This paper represent the reviewing of the construction of 16 bit high speed on adder. The motivation behind the investigation is that an adder is a very basic building block of Arithmetic Logic Unit (ALU) and would be a limiting factor in performance of Central Processing Unit (CPU).In the past, through examination of the algorithms with respect to particular technology has only been partially done. The merit of the new technology is to be evaluated by its ability to efficiently implement the computational algorithms. In the other words, the technology is developed with the aim to efficiently serve the computation algorithms. The reverse path; evaluating the merit of the algorithms should also be taken. Therefore, it is important to develop computational structures that fit well into the execution model of the processor and are optimized for the current technology. In such a case, optimization of the algorithms is performed globally across the critical path of its implementation. In this research article, we will present fast 16 bit adder with some approximation technique which is used in arithmetic application.**

***Index Terms*—Adders, Error tolerance (ET), Accuracy Configurable Adder (ACA), Speed Power Area Accuracy (SPAA), Application Specific Integrated Circuit (ASIC).**

I. INTRODUCTION

Adders are primary circuits validate arithmetic operations where they are calculate addresses, table indices and similar operations. High speed addition and multiplication are fundamental requirements of high performance processors. Therefore fast and accurate operation of digital system depends on the performance of adders. The core of every microprocessor, digital signal processor (DSP), and data processing application- specific integrated circuit (ASIC) is its data path. It is often the crucial circuit component if die area, power dissipation, and especially operation speed are of concern. At the core of data-path and addressing units in turn are arithmetic units, such as comparators, adders, and multipliers. Finally, the basic operation found in most arithmetic components is the binary addition.

Therefore, binary addition is the most important arithmetic operation. It is also a very critical one if implemented in hardware because it involves an expensive carry-propagation step, the evaluation time of which is dependent on the operand word length. The efficient implementation of the addition operation in an integrated circuit is a key problem in VLSI design. Productivity in ASIC design is constantly improved by the use of cell based design techniques such as standard cells, gate arrays, and field programmable gate arrays (FPGA) and by low and high level hardware synthesis. This asks for adder architectures which result in efficient cell-based circuit realizations which can easily be synthesized. Furthermore, they should provide enough flexibility in order to accommodate custom timing and area constraints as well as to allow the implementation of customized adders .Besides of the simple addition of two numbers, adders are also used in more complex operations like multiplication and division. The conventional electronic circuit design methodology utilizes three parameters in the tradeoff argument such as the energy consumption of the circuit, the area occupied by the circuit and the speed at which the circuit is being operated.

There are two important challenges that the world of computing is facing. Currently, the first challenge is due to the increasingly ubiquitous nature of the present day *portable* electronics ranging from mobile phones to GPS-based navigation devices. Portability demands lower energy consumption without compromising on the functionality. Also, demand for low energy consuming, also referred to as green design, electronics [1] is gaining a lot of momentum. The second challenge is manufacturing reliable and predictable electronic devices. Moore's Law predicts that the number of transistors on a single die is going to increase at an exponential rate. This has been accomplished by decreasing the size of an individual transistor up to 20nm where particular layers are gate oxide layer. But engineering considerations on lithography have limitations of designing these tiny elements precisely which leads to hindrances like thermal noise, parametric variations and other device perturbations [3,4,5] which leads to unreliable computing. These two challenges have competing requirements in the design of a VLSI system. A straightforward method of lowering the energy consumption is to lower the supply voltage of the circuit. But this would lead to transistors behaving unreliably because noise becomes a dominant factor. To ensure reliability, techniques such as redundancy and majority voting [6] can be used. However these

techniques tremendously increase the energy consumption of the circuit. Thus conventional methods typically have contradictory results and do not offer a common solution to both energy consumption and reliable design.

The conventional electronic circuit design methodology utilizes three parameters in the tradeoff argument such as the energy consumption of the circuit, the area occupied by the circuit and the speed at which the circuit is being operated. To face the challenges, a radically new solution to introduce a new alternate dimension, the accuracy of the circuit to the traditional design approach has been proposed recently. Currently there are three different techniques, applicable in different scenarios that use this novel fourth dimension in circuit design [9]. The first approach uses CMOS circuits that operate probabilistically due to noise [12]. The concept of a probabilistic CMOS switch (PCMOS) was introduced where a PCMOS inverter is correct with a probability parameter *p* ::: 1. The probabilistic inverter has been characterized in detail in terms of the relation between its energy consumption per switching and its probability of correctness. These probabilistic inverters were then used to design bigger probabilistic gates which switch correctness. These probabilistic inverters were then used to design bigger probabilistic gates which switch correctly with a probability of correctness. This work was later extended to develop a probabilistic Boolean logic, because it was realized that conventional Boolean logic was no more valid in the universe where devices are probabilistic and not deterministic [13]. In probabilistic Boolean logic, the basic operators are defined with a probability of correctness, for example, an AND gate with a probability of correctness *p* is defined as */\p*. Further extending the foundational probabilistic Boolean logic, a probabilistic arithmetic was developed, where the operators are also defined with a probability of correctness, such as + *p*.

II. LITERATURE REVIEW

According to the 2008 International Technology Roadmap for Semiconductors (ITRS) "Energy Consumption has become an increasingly important topic of public discussion in recent years because of global C02 emission .In general, the ITRS documents the impressive trends and, more importantly, sets aggressive targets for future electronics energy efficiency, for example, computational energy/operation (per logic and per memory-bit state changes). The most detailed targets relate directly to semiconductor materials, process and device technologies, which form the bases of integrated-circuit manufacturing and components, respectively." [2] . ITRS report states as a long term challenge "Dealing with fluctuations and statistical process variations". Also the report mentions that "Increasing yield loss due to non-visual defects and process variations requires new approaches in methodologies, diagnostics and control".

In [13] the author proposed a new novel adder targeting to reduce the area and increase the speed of the circuit. The work is shown below , first splitting the input operands into two parts: an accurate part that includes higher order bits and the inaccurate part that includes remaining lower order bits. Length of each part need not be equal and depends upon MAA′s and AP′s of application. The addition process starts from the joining point towards the two opposite directions simultaneously. Since the higher order bits play more important role than the lower order bits, normal addition method is applied for accurate part to preserve its correctness.

For inaccurate part no carry signal will be generated or taken in at any bit position to eliminate the carry propagation path. So eliminating the carry propagation path in the inaccurate part and performing addition in two separate parts, the overall delay and power is reduced. But the accuracy of the ETA-I is poor for small input numbers. In ETA-I the AP's are strong function of input range and degrades as input range decrease, but AP's are 100% for large input range.

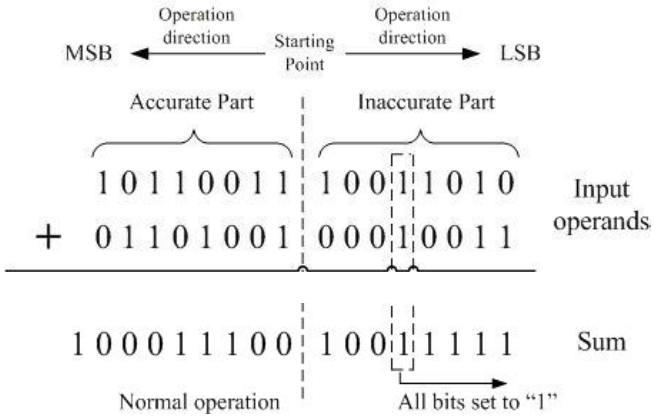

Figure 1: Approximate flow of Accuracy Configurable Adder

To solve small number addition problem, ETA-II [14] was proposed by Zhu. For the small input numbers, the accuracy of the ETA-I is poor, i .e. the AP′s are strong function of input range and degrades as input range decreases. ETA-I was limited only for low accuracy applications and to solve this problem, ETA-II was proposed by Zhu. ETA-II splits the entire carry propagation path into a number of short paths and completes the carry propagations in these short paths concurrently. In binary addition, worst-case happens when the carry signals are generated at the LSBs and propagates along the carry chain to the MSBs. If this worst case happens, tremendous amount of time and power will be consumed. As the worst case seldom happens, hence for most of the cases, this carry signal can be determined by just considering several input bits on the right of the current bit position. In ETA-II [14], an N − bit adder is divided into M blocks (M _ 2). Each block contains N/M bits and consists of two separate circuitries – Carry Generator and Sum Generator. The carry generator creates the carry-out signal and does not take carry-in signal from previous block and, hence the carry propagation only exists between two neighboring blocks. The longest carry propagation path of ETA-II is 2N/M and, hence worst-case delay of ETA-II is only 2/M times of the conventional adder. The accuracy of ETA-II for large input operands is degraded than ETA-I. The degraded accuracy for large input may still restrict ETA-II use. In modified ETA-II [14] design, the higher order bits should be more accurate

than the lower order bits. In modified structure, the first three carry generators are cascaded together to generate the carry signals. In this way, the carry signal for the highest block is generated by the preceding 12 bits and the carry signal for the others block is generated by the preceding 8 bits.

The approximate designs have difficulty of detecting and correcting errors, since they are designed for error-acceptable applications with target accuracy. In some applications, however, more accurate or totally accurate results are required under certain conditions, e.g., image processing in security cameras. In contexts where the required accuracy changes during runtime, the accuracy of results should be configurable to maximize the benefit of approximate operations. Figure illustrates how power benefits can be achieved with an accuracy-configurable design.

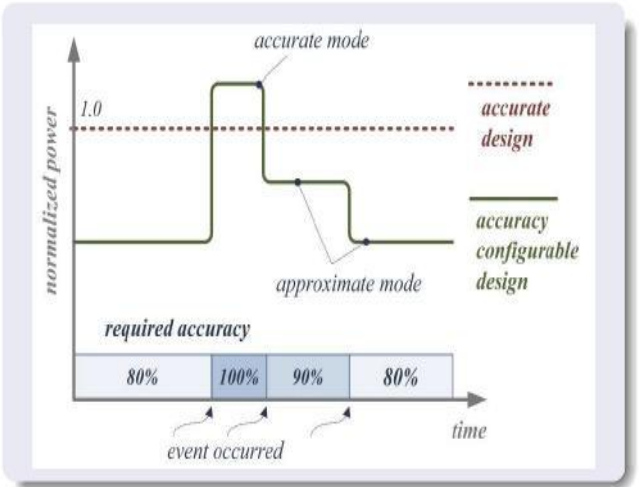

Figure 2: Accuracy level of Accuracy Configurable Adder

The Accuracy Configurable Adder (ACA) [16] adder has feature of runtime accuracy configurability for better trade-off between accuracy, performance, and power. In ACA adder, the carry chain is cut to reduce critical-path delay, and sub-adders generate results of partial summations to increase accuracy Without the middle sub-adder, for random input patterns the error rate is 50.1%, whereas with the introduction of the middle sub-adder, error rate is reduced to only 5.5%.In the real implementation all redundant parts are optimized only for carry generation. In modern adder design, such as carry look ahead (CLA), carry select adder and Kogge Stone adders, the path depth and area are asymptotically proportional to *log2N and Nlog2N* respectively, where *N* is the bit width of the adder. Based on this delay, area and power are reduces. In implementation of N bit ACA adder with a parameter k, which is a bit width of the sub adder result. In this adder, each divided sub module produces a k bit result except for the last sub module which produces a 2k bit result. The ACA adder consists of the (Nk-1) sub modules. Table 1 shows the result of ACA adders with different parameter values of k. With smaller value of k, the minimum clock period and dynamic power can be reduced but the pass rate will be decreased.

Table 1: Estimated minimum clock period, area, dynamic power and pass rate for each value of k.

	K=2	K=3	K=4	K=5	K=6
Min. clock period	0.5	0.65	0.75	0.83	0.89
Area	0.87	1.05	1.12	1.15	1.12
Dynamic power	0.44	0.68	0.84	0.95	1.00
Pass rate	0.55	0.82	0.94	0.98	0.99

Variable latency adder [24] can be categorized into two functional units. The first one is designing a ACA (almost accurate adder).The conventional adder will be replaced with almost accurate adder, which produces correct results in majority cases. The design of ACA is done on the idea of longest prorogated signals in input addenda. The second application is which corrects the sum of the adder when the accurate result is required. In second functional unit we perform addition to the input addenda that which cross the limit of prorogated signals in previous speculative sequence. This is simple error detection and error correction unit. An extremely fast adder can be constructed by creating several small adders from 1 long adder. For example, if we want to add two 20-bit integers. Since the longest sequence of propagate signals is 4, the carry output ci at bit position i will be independent of ci-5. Hence, si can be computed only using the input bits of 6 preceding bit positions starting from ith bit position. In other words, we can form several 6 bit adders, each computing the carry-in and sum bit for a particular bit position as shown in Figure. The delay of this particular 20-bit adder will be virtually the same as that of a 6-bit adder.

In this paper [24] they took a specific case of 20 bit VLSA, which have two elements: 20 bit almost correct adder and an error detection circuit. In order to add two n-bit integers A and B, one can define generate, propagate and kill signals at each bit position as follows: The binary integers are denoted by uppercase letters, e.g., A, B are n bit binary numbers; the ith least significant bit of an integer A is denoted by ai. In order to add two n-bit integers A and B, one can define generate, propagate and kill signals at each bit position as follows:

gi = aibi
pi = ai xor bi
ki = ai + bi

III. RESEARCH GAP

Many authors develop imprecise but simplified arithmetic units, which provide an extra layer of power savings over conventional low-power design techniques. This is attributed to the reduced logic complexity of the proposed approximate arithmetic units. Note that the approximate arithmetic units not only have reduced number of transistors, but care is taken to ensure that the internal node capacitances are much reduced. Due to the limitations in this methods and the accuracy level requirements still the complexity can be reduced and the SPAA metrics can be still achieved efficiently. So to improve SPAA metrics we need a novel

arithmetic unit with low power, high speed, with increased density and PVC aware circuits.

IV. OBJECTIVE

The goal of this project is to design and implement an efficient adder unit. In this work, the main focus is on performance and accuracy, but we do provide some numbers for the arithmetic units relating to energy and power. This is to provide an estimate of the amount of energy and power consumed by the units we choose to implement. The priorities of this project in order of importance are:

1) Robust and safe circuits.
2) Design time.
3) Area/speed balance.

V. APPLICATIOONS

The set of RMS [21] workloads is examined next in terms of usage, mathematical models, numerical algorithms, and underlying data structures. In image processing and many other DSP applications, the computational process of FFT involves a large number of additions and multiplications. Applications exclaim for approximate designs:

1) Recognition, Mining, Synthesis (RMS) Applications.
2) Human Sense Applications.
3) Inherent Error Applications.
4) Image processing.

VI. CONCLUSION

In this paper basically we study about the previous existing different kind of adder logic. According to previous study we found that there are lots of issues with those design. Some previous adder logic is fast but there hardware unit is very high and some have less hardware unit but they are slow in simulation. So in this paper we present some of the future objective which can still need modification on these area.

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