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Enhanced Memory Reliability against Multiple Cell Upsets Using Decimal Matrix Code for 32-Bit Data

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Abstract— **Transient multiple cells upsets (MCUs) is an important issue if consideration is the reliability of memories exposed to radiation environment .Many superior packaging technique are available which protect the memory data from radiations and transients. However, a particular packaging provides protection from a limited variation of radiations. Due to the increasing demand in the application in wireless communication field the devices are exposed to a very wide range of environment radiations. Consequently some supplementary data protection techniques are always preferred for authenticating the data before it is processed. A number of these techniques use encoded data to be stored in memories. Error correction codes (ECCs) are used to encode the data which is used to be stored in the memory. A less number of redundant bits to be stored and a minimized delay overhead in data correction are always chosen to implement an error correction code. This paper presents an FPGA based execution of memory data error detection and correction code that involves simple decimal addition algorithm in the encoding of data that is to be stored in memory and The Hamming code is used for decoding of the data for error detection and correction. Symbolic codes are composed by divide-symbol concept to represent the linear data in groups. The length of the symbol is inversely proportional to the delay overhead of the code.**

***Index Terms*— Decimal Metric Code, Decimal Addition, Logic Gate Comparator, Memory Error Correction Codes, Syndrome.**

I. INTRODUCTION

The increasing size of embedded memories electronic systems and scaling down of CMOS technology to deep nanoscale that are exposed to space environment radiations are the cause for rapidly increasing the soft error rate in memory cells. The soft error in the memories are introduced due to the radiations that have ionizing character that affect the charge stored as data in semiconductor memory. With the help of memory block the phenomena of error generation due to radiation effect the memories that are exposed to the environmental radiations are shown by fig. 1. While a major concern about memory consistency is single-bit error but in some cases "multiple-bit error" or "multiple cell upset" (MCUs) becomes a serious reliability concern. Many researchers recommend some error correction codes (ECCs) in order to tolerant the faults in the memory upto the maximum possible extent. A simple block diagram of the fault tolerant memory encoder implementation is shown in fig. 2.

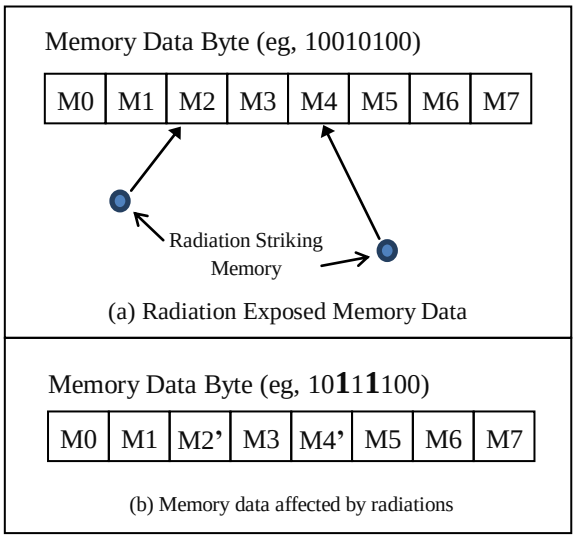

Fig. 1. Soft Error in Semiconductor Memory due to Energy Radiation

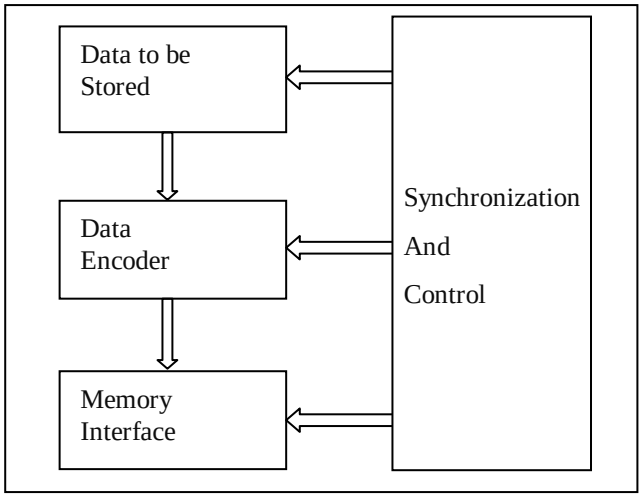

Fig 2. Data Encoder Block Diagram

With the help of the encoder circuit the data to be stored is first encoded to generate redundant bits for fault tolerant memories. The data and the redundant bits are stores in the memory with the help of memory interface. Decoder can use these redundant bits for correcting the errors from the memory data. only some of the most reliable codes include Bose-Choudhary-Hocquenghem (BCH) code, Reed-Solomon (RS) code and Punctured Difference Set (PDS) code. These codes have been used to deal with MCUs in memories. To control MCUs Interleaving technique has also been used that rearranges cells in the physical arrangement to separate the

bits into different physical words from the same logical word. Interleaving with content-addressable memory (CAM) is not practically used with the fixed coupling hardware architecture from both cells and comparison circuit structure. Against MCUs the researchers also proposed a single error correction and double error detection technique like Built-in-Current-Sensors (BICS). MCUs per word can be efficiently corrected by recently proposed 2-D matrix code (MC). In 2-D matrix code one word is divided into multiple rows and multiple columns, and two codes were use to protect the bits per rows and per columns and these are Hamming code and Parity code where the bits per row are protected by Hamming Code and the bits per column are protected by parity code. Two bit error detected by Hamming code is corrected by using the vertical syndrome bits. The 2-D MC is accomplished of correcting only two errors in all cases. As compared to other codes this code has a lower delay overhead. In this paper a novel decimal matrix code (DMC) is proposed. The function of the proposed code is based on divide-symbol to provide improved memory consistency. Decimal integer addition (decimal algorithm) on the divided symbols of binary code is utilizes by the proposed DMC. To detect and correct error bits a logic comparator is used by the decoder in the proposed work to find the error syndrome. The reliability of the error detection capability of the code is enhanced by the decimal algorithm. The rest of this paper is arranged as follows: section-II presents the work published by some recent scholars under the title 'Literature Review'. Section-II presents the proposed design of DMC Encoder and Decoder. The simulation and synthesis based results and comparative analysis of the proposed designs are given in section-IV. Finally the conclusion based on the proposed work is discussed in section-V.

II. Literature Review

In [1] a novel per-word DMC was proposed to guarantee the dependability of memory by utilizing decimal algorithm to detect errors, so that more than one error can be detected and corrected. Now an alternative approach to overcome the reliability issue of radiation is discussed in [2] and this gives a comparative study of various error correction codes. In reference [3] and [4] a new technique that uses hamming code for the correction of errors are implemented for a highly reliable decimal code. A mechanism derived From Orthogonal Latin Square Codes for: (i) single error correction, double error detection triple-adjacent error detection using hamming code, and (ii) single error correction, double error detection, double adjacent error correction Codes are proposed in reference [5].In reference [6] a CAM data protection scheme using DMC is proposed. For error correction references [7, 8] presents the implementation of decimal matrix code and parity matrix. In memory data synthesis results against multiple bit error are shown in reference [7, 8]. In 2-D arranged memory data Carry Save Adder (CSA) based decimal error detection technique is implemented in reference [9]. A better quality protection level against large MCUs in memory shown in reference [10] which gives an enhanced error detection technique using Hybrid Matrix Code (HMC) To obtain better performance of DMC against Hamming code a decimal matrix code technique is performed in [11, 12, 13]. In reference [14] a DMC architecture is proposed that is capable of correcting up to 5-bit error. For error correction with high reliability an implementation of DMC and HMC are performed in [15-16]. An Encoder Reuse Technique (ERT) based DMC implementation is presents in [17-18] to reduce the area of the proposed algorithm design.

III. Proposed Design Of Decimal Matrix Code Encoder And Decoder

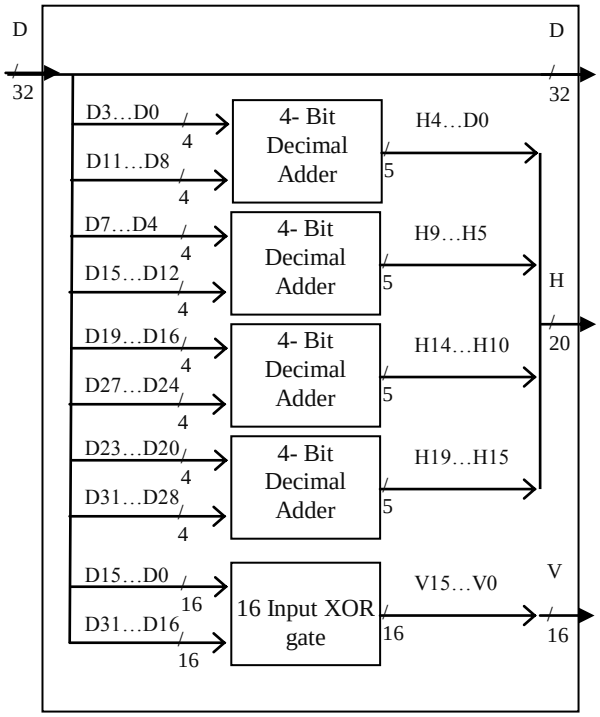

Figure4. Proposed 32-bit Architecture of DMC Encoder

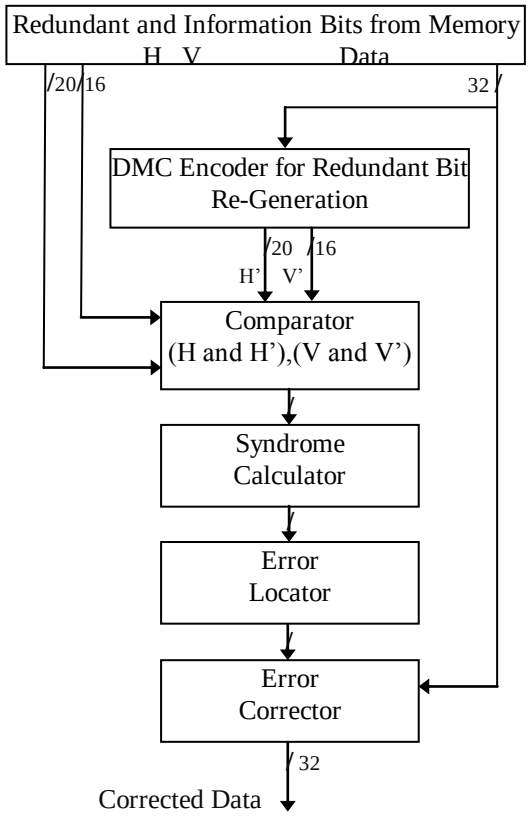

Fig 4. Proposed DMC based Architecture of Fault Tolerant Memory

In the proposed work the syndrome bits are generated by using the XOR comparator gate. The unadventurous design of error syndrome producer utilizes decimal subtractor logic to generate the syndrome data. The Syndrome creation in the proposed work is shown in fig. 6. The horizontal and vertical syndrome bits are sown by the equations that are shown as follows:

$$V_{syn} = V \text{ xor } V'$$
$$H_{syn} = H \text{ xor } H'$$

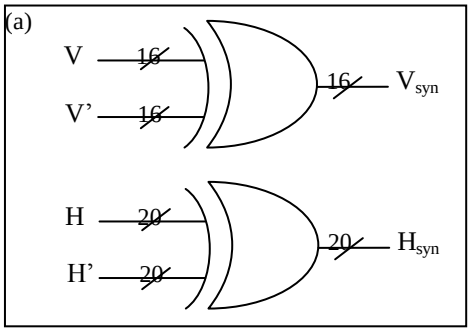

Figure6. Syndrome generation using proposed XOR-comparator (a) Vertical Syndrome, (b) Horizontal Syndrome

To place the symbol that contains error the horizontal and vertical syndrome bits are grouped with the same length as that of horizontal and vertical redundant bits. This grouping is depicted in fig. 7.

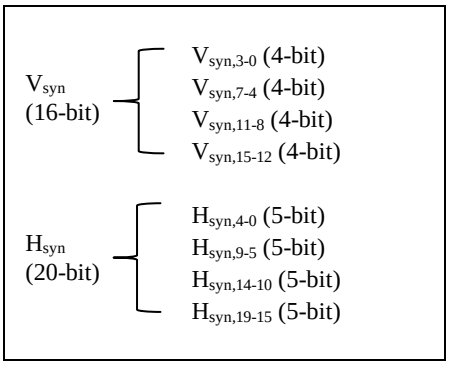

Fig 7. Grouping of Syndrome Bit

For identefing the error location in the data matrix a common symbol in the data matrix from the non-zero syndrome horizontal and vertical symbols are present. This is depicted in fig. 8. Thus the indication of the non zero value od the syndrome bits shows that there is an error in the stored data symbol D'_{3-0}. Similarly errors in other stored data symbols can also be located.

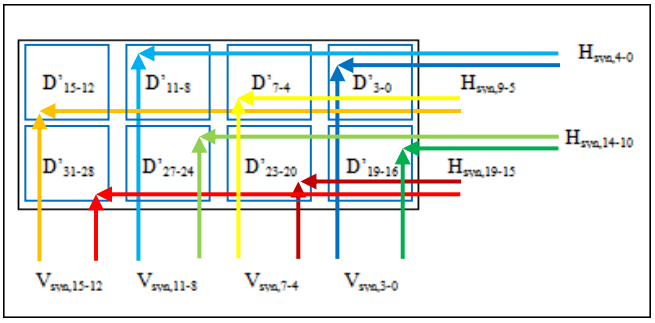

Fig. 8 Error Location using Syndrome Data

The error syndrome is "zero" selects the memory data as it is, else, the error is corrected by the error corrector logic by performing the bit inversion from the error symbol. The bit inversion is performed by using XOR operation which is shown as follows.

Corrected Data		Memory Data		Syndrome Data
Sym-0_out	=	Sym-0	xor	$V_{syn,3-0}$
Sym-1_out	=	Sym-1	xor	$V_{syn,7-4}$
Sym-2_out	=	Sym-2	xor	$V_{syn,11-8}$
Sym-3_out	=	Sym-3	xor	$V_{syn,15-12}$
Sym-4_out	=	Sym-4	xor	$V_{syn,3-0}$
Sym-5_out	=	Sym-5	xor	$V_{syn,7-4}$
Sym-6_out	=	Sym-6	xor	$V_{syn,11-8}$
Sym-7_out	=	Sym-7	xor	$V_{syn,15-12}$

IV Simulation And Synthesis Results

Fig-9, Fig-10 respectively shows the Encoder and Decoder simulation waveforms. The current work is simulated using Xilinx. Fig-12(a) and Fig-12(b) respectively shown the RTL Schematic diagrams of Encoder and Decoder.

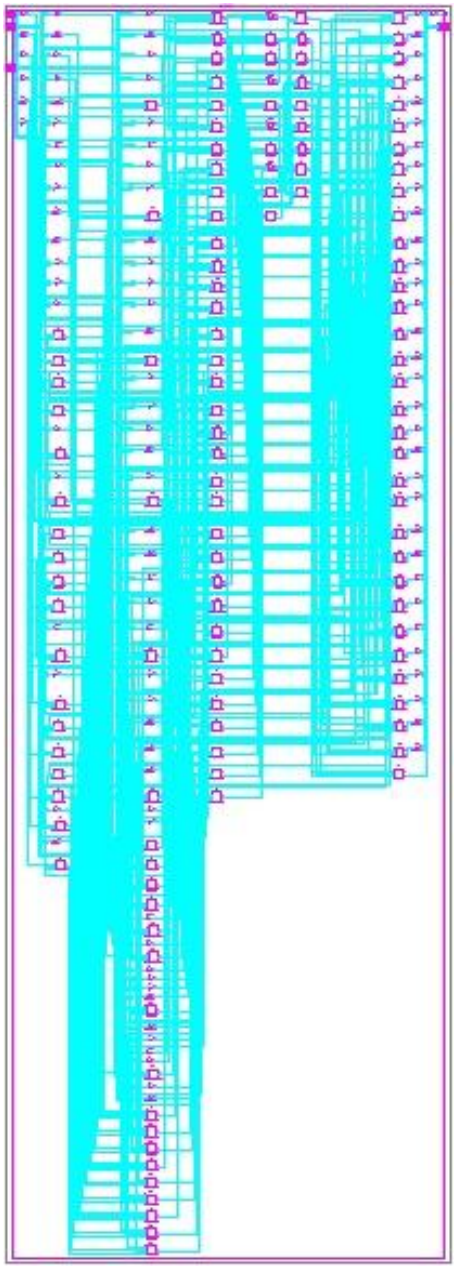

Fig. 9. RTL Schematic of Proposed DMC Decoder

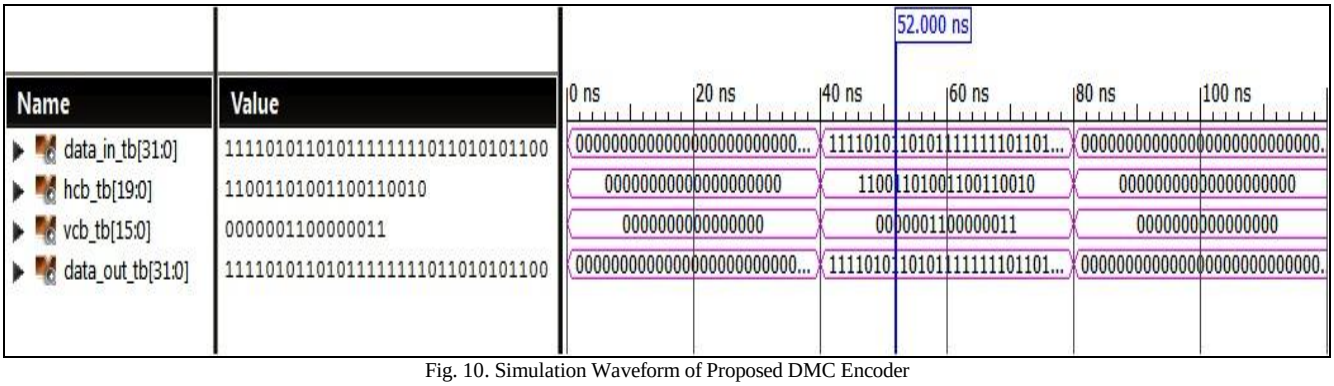

Fig. 10. Simulation Waveform of Proposed DMC Encoder

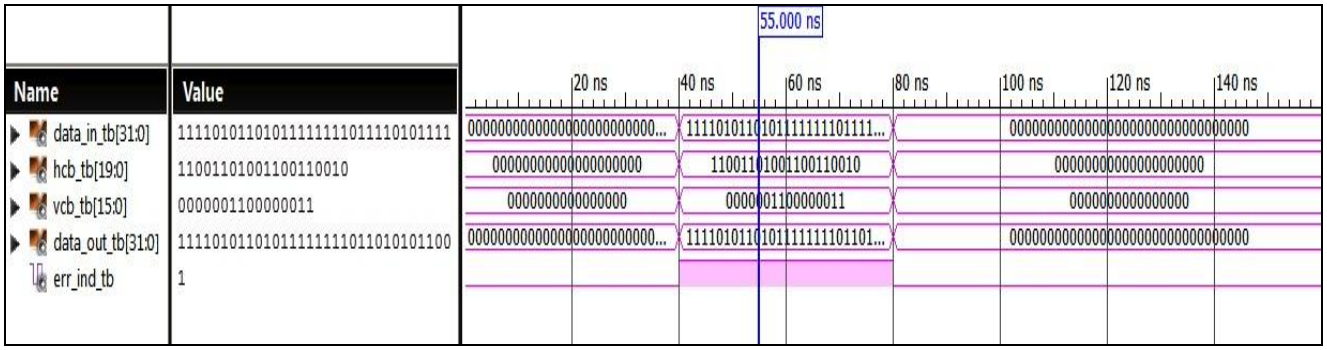

Fig. 11. Simulation Waveform of Proposed DMC Decoder

The proposed design is simulated for FPGA device based hardware with a capability of burst error handling. The FPGA hardware utilization summary of the Encoder and Decoder proposed in this brief are presented in Table-I and Table-II respectively.

TABLE I
HARDWARE UTILIZATION SUMMARY OF PROPOSED 32-BIT DMC ENCODER

Spartan-3E XC3S500E-4PQ208	Total	32-bit DMC Encoder	
		Used	%
Slices	4656	26	0
LUTs 4-Inputs	9312	48	0
Bonded IOBs	158	100	63

TABLE II
HARDWARE UTILIZATION SUMMARY OF PROPOSED 32-BIT DMC DECODER

Spartan-3E XC3S500E-4PQ208	Total	32-bit DMC Decoder	
		Used	%
Slices	4656	70	0
LUTs 4-Inputs	9312	123	0
Bonded IOBs	158	101	63

CONCLUSION

In proposed DMC XOR comparator is projected for the modified Syndrome calculation in the presence of MCUs. Now the horizontal redundant bits *H* and vertical redundant bits *V* are obtained by the information bits when they are fed to the encoder. And the corrected words from the cell upset are obtained from the decoding process. The area of DMC is minimized by reducing its decoder block. Replacement of the decimal subtractor by simple XOR based comparator are proposed in this work and reduces the area overhead of the decoder.

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