ISSN: 2278 – 7798
International Journal of Science, Engineering and Technology Research (IJSETR)
Volume 5, Issue 5, May 2016

SPAA Aware Approximate Processing Unit for 2D Discrete Cosine System

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Abstract-

The recent time witnesses a tremendous need for high performance digital signal Processing (DSP) systems for high end emerging applications like HD-TV, medical imaging, satellite communication, 3G mobile technologies etc. For all these applications, the sources of data are video signals. For transmission of video signals significant amount of bandwidth required. Since the captured video data contain huge amount of redundant data, there is an opportunity for video data compression keeping the picture quality intact. DCT is a well known technique used in video or image compression. DCT algorithms are computation intensive and involve large number of multiplication and addition operations. Therefore, with the increase in number of length of the DCT, the number of multiplication and addition operations also increase leading to larger chip area and performance degradation. The primary aspect of the 2-D DCT computation is to compute the DCT coefficients, where a large number of mathematical computations are required.

Keywords: DSP, DCT, 2-D DCT

I. INTRODUCTION

Image data which is processed for communication mainly undergo with some standards of Digital Image Processing(DIP) compression like JPEG (Joint Photographic Expert Group) , MPEG-x DCT has been utilized in various applications like image recognition, watermarking, encryption, compression of image and video data, etc. DCT being a lossy compression which hardly detected by human eye, this has opened a new area of research for multimedia operations by allowing the constraints to have imprecise computation or approximate computation. Approximation can be used in the application where human sense is required, because human eye is unable to recognize correct image or approximate image with accuracy greater than 95% [2]. By approximation we can improve the VLSI domain entities like computation time, area, power consumption required to implement the circuit and hardware cost with trade-off in image/video precision. The construction of a typical real-time imaging or video embedded (Motion Picture Expert Group), which begins major component in today's data centered world. Image and video procession governs mainly with the processing unit mainly known as compression unit. Compression unit is distinguished on two types:

1) Lossless: In this the image pixels are not compressed or compromised.
2) Lossy: With the help of some transform, utmost compression is achieved.

While Studying the Structures/Standards of Image/Video, the most prominent and computing part is Discrete Cosine Transform (DCT)/ Discrete Wavelet Transform (DWT) & solely depends for data compression and data flooding in the communication channel apart from encoding and decoding. In this thesis we will concentrate on DCT and its application, DCT transforms the signal or data in the form of low to high frequency spreaded in various locations for proposed block of data. The frequencies are concentrated on the different corners of block.

In this report, my prime focus is on the JPEG IP block. JPEG is abbr. as Joint Photographic Expert Group. This is an international compression standard for still image may it be gray or color.

system is usually an integration of a range of electronic devices, e.g. image acquisition device, signal processing units, memories, and a display. Driven by the market demand to have faster, smarter, smaller and more interconnected products, designers are under greater pressure to make decisions on selecting the appropriate technologies in each one of the devices among many of the alternatives. Trade-offs are constantly made concerning e.g. cost, speed, power, and configurability.

The latter yields visually pleasing images by utilizing more advanced scaling methods. In many practical real-time applications, the scaling process is included in end-user equipment, so a good lower complexity scaling technique, which is simple and

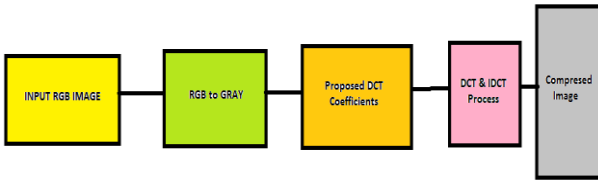
suitable for low-cost VLSI implementation, is needed.

II. METHODOLOGY

In this section the methodology to overcome the research gaps are mentioned. Reducing the simulation time taken by JPEG unit. (DCT simulation time). To reduce the simulation time we adopt the error resilient technique in which the image quality at user end is decided as per the user .

Here we will design an novel algorithm which is based on truncate approach as we know for DCT coeffients there is need of 64 blocks means 8X8 matrix, but according to our proposed design there is no need to take all 64 blocks because some blocks are having te all information which will create complete image so there is no need to take all coeffiencts. According to proposed design we will take only 30 blocks. Now theps we will follow in our proposed algorithm:

1. The input image can be read by using imread function and then broken into 8x8 block of matrixes.
2. The algorithm can be applied for gray scale by suitably using functions such as is gray functions.
3. Apply total 30 coefficients on input image block.
4. DCT is applied to each block on its both the rows and columns. Strassen's matrix multiplication algorithm is applied on the DCT matrix multiplication calculation.
5. Each block is compressed by quantization. Suitably the quantization matrix is selected. They are standard matrices used in JPEG.
6. The array of compression blocks that constitute the image is stored in a significantly reduced amount of space.
7. The image is reconstructed through decompression using Inverse DCT.



As we can see according to our proposed algorithm of DCT it will take only 30 coefficients which will generate out image as a compressed image. In this thesis basically we are targeting original accurate DCT approach and also we done comparative analysis with previous existing design. For analysis point of views we use these parameters:

1. **Time Complexity**
2. **Logic**
3. **Delay**
4. **Frequency**

III. RESULT & ANALYSIS

In this section we will represent the comparative analysis between exsistng and proposed design. Here we will did both algorithm leval and hardware level analysis. Algorithm leval analysis is done on MATLAB tool. Similar architecture level analysis we did on Verilog HDL language.

Here for algorithm analysis we use a test images which is:

- **Boat**

We will apply our proposed and previous existing design on the test image and did comparative image quality analysis in terms of:

- PSNR(peak signal to noise ratio)
- SSIM(structural similarity based image quality assessment)
- FSIM(feature similarity based image assessment)
- GMSD(gradient magnitude similarity deviation)
- % Similarity

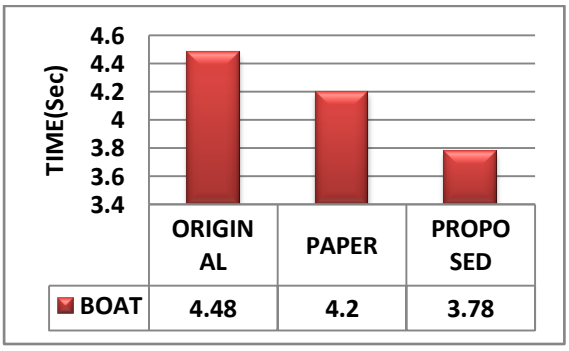
Test Image

Paper Image

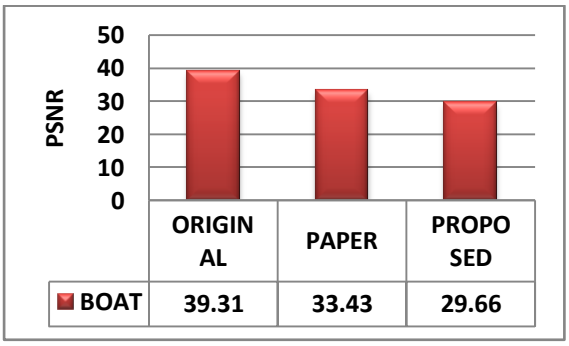
Proposed Image

Algorithm Analysis for BOAT Image:

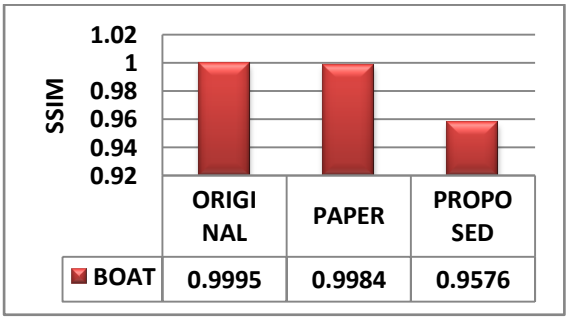
Time Complexity Analysis:



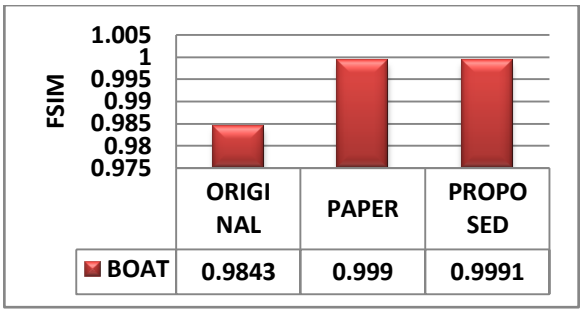
PSNR Analysis:



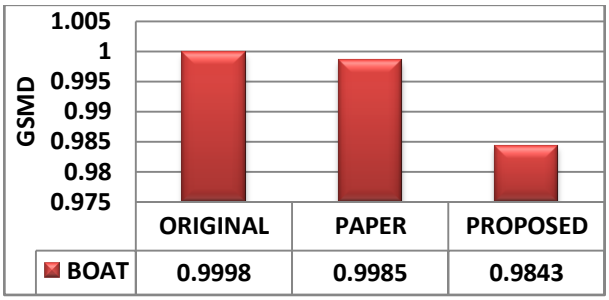
SSIM Analysis:



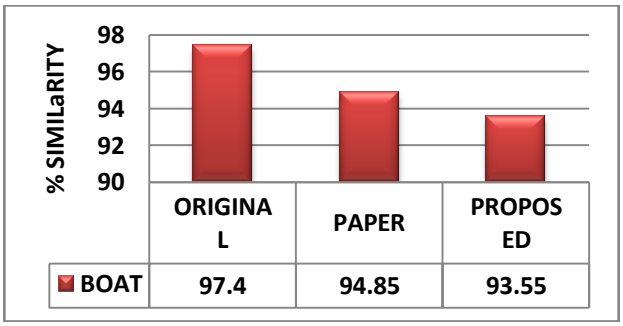
FSIM Analysis:



GMSD Analysis:



% Similarity Analysis:

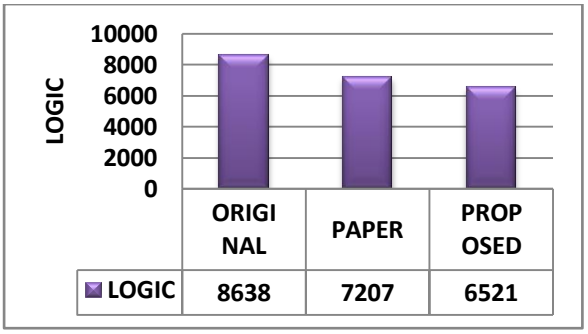


Hardware Level Analysis:

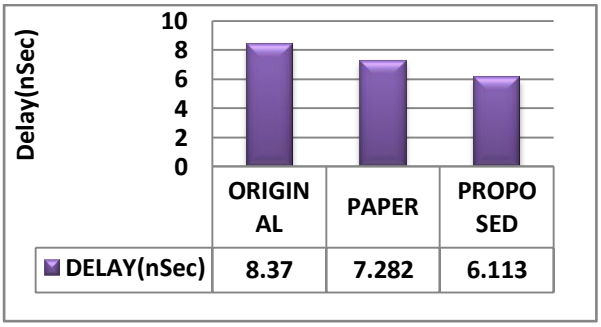
Here we did hardware level analysis by using we use Model SIM tool. Here we use some parameters for comparative hardware level analysis. Those parameters are:

1. **Logic**
2. **Delay**
3. **Frequency**

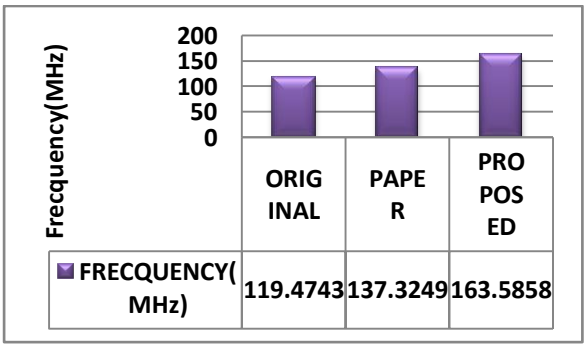
Comparative analysis on LOGIC:



Comparative analysis on Delay:



Comparative analysis on Frequency:



So according to result analysis we can say that our proposed approach is better than paper DCT because it will require less hardware unit with less time complexity. Our proposed approach reduce the hardware complexity. Here our image analysis parameters show that proposed technique will generate image with acceptable image. So those error are tolerable by human eye. Here we did improvement of approx 10-20% in terms of all parameters.

IV. CONCLUSION

In this thesis basically we represent a novel algorithm with novel architecture. Our proposed algorithm is having less time complexity fundamental. Here according to our proposed algorithm we will reduce the number of coefficients. According to our proposed design we use only 30 coefficients which are efficient for generation of compressed image with maintaining quality level. Algorithm level analysis is done on MATLAB by using of some scientific parameters which shows the generated image having acceptable quality. Similar hardware design is done on Xilinx 14.2 using HDL language and output result shows there is approx 10-20% improvement in terms of area, delay frequency as compare to previous existing design.

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