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A NOVEL THREE PHASE 31-LEVEL CASCADED MULTILEVEL INVERTER FED INDUCTION MOTOR DRIVE

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ABSTRACT-A new topology of cascaded multilevel converter is proposed. The proposed topology is based on a cascaded connection of single-phase sub multilevel converter units and full-bridge converters. Compared to the conventional multilevel converter, the number of dc voltage sources, switches, installation area, and converter cost is significantly reduced as the number of voltage steps increases. Then, the structure of the proposed topology is optimized in order to utilize a minimum number of switches and dc voltage sources, and produce a high number of output voltage steps. The prior H-bridge based multilevel inverter can increase the number of output voltage levels by adding switch components and DC input voltage sources.If it employs twelve switches and four DC sources, the number of output voltage levels becomes thirty-one .In this project first single phase 31-level cascaded multilevel inverter is proposed with series connection of submultilevel inverters and there after proposed topology is extended to a novel three phase 31-level cascaded multilevel inverter fed induction motor drive. In this topology electromagnetic torque, speed, three phase currents of induction motor are observed. As the number of levels increases the harmonics are decreased. This topology offers very less THD which is equal to THD=1.25. The operation and performance of the proposed a single-phase 31-level multilevel inverter and three phase 31-level with induction motor drive is verified by MATLAB/ SIMULINK.

Index Terms—multilevel inverter, optimal structure, sub-multilevel inverter, PWM technique, H-Bridge Inverter.

I.INTRODUCTION

Over many years, Induction motor drives have been popularly used for variable speed control applications in industries. This is because the induction motor is simple in construction and requires less maintenance. In recent times, multilevel inverters (MLI) are gaining popularity and widely used for induction motor drive applications [1-3]. It is especially used for medium to high voltage and high current drive applications. There are many advantages of multilevel inverters as compared to conventional inverters. Main advantages are low total harmonics distortion (THD), low switching losses, good power quality and reduced electromagnetic interference (EMI). Main feature of multilevel inverter is that it reduces voltage stress on each component [4-8]. The topologies of multilevel inverters are classified into three types. They are flying capacitor, diode clamped and H-bridge cascaded multilevel inverters. Cascaded H-bridge (CHB) multilevel inverter is one of the most popular inverter topology used in high-power medium voltage (MV) drives. It is composed of a multiple units of single-phase H-bridge power cells. In practice, the number of power cells in a CHB inverter is mainly determined by its operating voltage and manufacturing cost.

Cascaded H-bridge multilevel inverter requires the least number of components for the same voltage level as compared to all three types of inverter [9-11]. The growth of multilevel inverter caused development of various modulation schemes. The most common initial application of multilevel converters has been in traction, both in locomotives and track-side static converters. More recent applications have been for power system converters for VAR compensation and stability enhancement, active filtering, high-voltage motor drive, high-voltage dc transmission and most recently for medium voltage induction motor variable speed drives. Many multilevel converter applications focus on industrial medium-voltage motor drives, utility interface for renewable energy systems, Flexible AC Transmission System (FACTS) and traction drive systems. In recent years, multilevel inverters have received more attention in industrial applications, such as motor drives, static VAR compensators and renewable energy systems. Compared to the traditional two-level voltage source inverters, the stepwise output voltage is the major advantage of multilevel inverters.

The CHB multilevel inverters use series-connected H-bridge cells with an isolated dc voltage sources connected to each cell. The CHB multilevel inverters can be divided into two groups

from the viewpoint of values of the dc voltage sources: the symmetric and the asymmetric topology. In the symmetric topology, the values of all of the dc voltage sources are equal. This characteristic gives the topology good modularity. However, the number of the switching devices rapidly increases by increasing the number of output voltage level. This paper proposes a new multilevel inverter topology using series-connected sub-multilevel inverters. The proposed multilevel inverter uses reduced number of switches. Initially, the proposed sub-multilevel inverter is described and then the series connection of them to form a multilevel inverter is discussed. The optimal structures of the proposed multilevel inverter regarding several factors (e.g., number of switches, number of dc voltage sources, standing voltage on the switches, etc.) are also obtained. The power loss of the proposed topology is calculated. Afterward, the proposed multilevel inverter is compared with other multilevel inverter topologies considering the number of switches. A design example is then given which is used for simulation and experimental studies.

II. PROPOSED TOPOLOGY

A.PROPOSED SUB-MULTILEVEL INVERTER

Fig. 1 shows the proposed sub-multilevel inverter. As depicted in Fig. 1, the topology consists of n dc voltage sources. In general, the dc voltage sources can have different values. However, in order to have equal voltage steps, they are considered to be the same and equal to Vdc. Each sub-multilevel inverter consists of n+2 switches. Some of the switches are unidirectional and the others are bidirectional. The unidirectional switches consist of an insulated gate bipolar transistor (IGBT) with an anti-parallel diode.

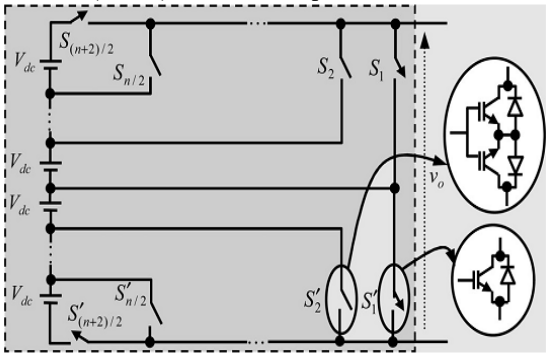

Fig.1. Proposed sub-multilevel inverter.

The same conditions are valid for the other switches. Therefore, the switches have to withstand both positive and negative voltages. In addition, the switches have to conduct backward current that is as a result of inductive characteristic of the load. It can be concluded that the switches must be bidirectional. There are several circuit configurations for bidirectional switches. In this study, the common emitter topology is used as it needs one gate driver for a switch. Considering the types of the switches, 2nIGBTs are required in the proposed sub-multilevel inverter. It is worth mentioning that the number of the anti-parallel diodes is equal to the number of IGBTs.

The proposed sub-multilevel inverter can only generate zero and positive voltage levels. The zero output voltage is obtained when the switches S1 and S1 are turned ON simultaneously. The other voltage levels are generated by proper switching between the switches. Table I shows the states of the switches for each output voltage value. In this table, 1 means that the corresponding switch is turned ON and 0 indicates the OFF state.

TABLE I: OUTPUT VOLTAGES FOR STATES OF SWITCHES

State	Switches states									v_o
	S_1	S'_1	S_2	S'_2	…	$S'_{n/2}$	$S_{n/2}$	$S_{(n+2)/2}$	$S'_{(n+2)/2}$	
1	1	1	0	0	…	0	0	0	0	0
2	0	1	1	0	…	0	0	0	0	V_{dc}
3	0	0	1	1	…	0	0	0	0	$2V_{dc}$
⋮	⋮	⋮	⋮	⋮	…	⋮	⋮	⋮	⋮	⋮
$n-1$	0	0	0	0	…	1	1	0	0	$(n-2)V_{dc}$
n	0	0	0	0	…	0	1	0	1	$(n-1)V_{dc}$
$n-1$	0	0	0	0	…	0	0	1	1	nV_{dc}

B.PROPOSED 31-LEVEL MULTILEVEL INVERTER

The 31-level inverter shown in Fig.2 can be proposed. This topology consists of ten unidirectional power switches and four dc voltage sources. According to Fig. 2, for the asymmetric topology, the value of the dc voltage sources is different from a submultilevel inverter to another. In other words, if the dc sources of the first submultilevel inverter is $V_{dc,1}$, the dc sources of the second submultilevel inverter is $V_{dc,2}$. To get maximum number of level for the output voltage, there must be no redundancy.

This is achieved when the value of the dc voltage sources in submultilevel inverters have the following relation. It is important to note that the 31-level topology can be provided through the

structure presented in Fig.1, where the only difference will be in the polarity of the applied dc voltage sources.

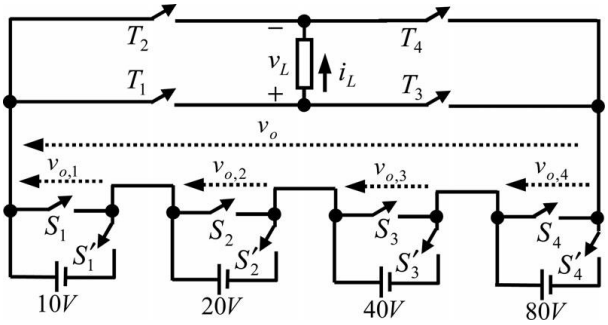

Fig.2. Proposed 31-level multilevel inverter.

By developing the proposed 31-level inverter. This topology,

$$V_{dc,2} = (n+1).V_{dc,1} \quad (1)$$

$$V_{dc,3} = (n+1).V_{dc,1} + nV_{dc,2} \quad (2)$$

$$V_{dc,3} = (n+1)V_{dc,1} + n(n+1)V_{dc,1} \quad (3)$$

$$V_{dc,3} = (n+1)(n+1).V_{dc,1} \quad (4)$$

Therefore, in general, the following relation should be valid for the dc sources of the sub multilevel inverters:

$$V_{dc,i} = (n+1)^{i-1}.V_{dc,1}, \quad i = 1,2,3,\dots\dots m \quad (5)$$

Where $V_{dc,i}$ is the value of the dc sources in the ith submultilevel inverter.
The maximum value of the output voltage (sum of all dc
voltage sources) for the proposed asymmetric topology can be obtained as follows:

$$V_{0,max} = n\sum_{i=1}^{m} V_{dc,i} \quad (6)$$

Using (5) and (6), the maximum value of the output voltage can be written as

$$V_{0,max} = [(n+1)^m - 1]V_{dc,1} \quad (7)$$

With the aforementioned arrangement of the dc voltage
sources, the number of voltage levels will be equal to

$$N_{level} = 2(n+1)^m - 1 \quad (8)$$

For the asymmetric topology, the total standing voltage of the switches $V_{stand,total}$ is sum of standing voltages on the switches of the sub multilevel inverters and also the standing voltage on the switches of the H-bridge part ($4V_{0,max}$). Therefore, it can be written as follows:

$$V_{stand,total} = \sum_{i=1}^{m} V_{stand,i} + 4V_{0,max} \quad (9)$$

the total standing voltage of the switches can be written as follows:

$$V_{stand,total} = \left[\frac{(n+1)^m - 1}{n}\right].$$

$$V_{stand,1} + 4[(n+1)^m - 1].V_{dc,1} \quad (10)$$

Using (8) and (10), the total standing voltage in terms of
Number of output voltage level and can be expressed as follows:

$$V_{stand,total} = \left[\frac{N_{level} - 1}{2}\right].\left(\frac{V_{stand,1}}{n} + 4V_{dc,1}\right) \quad (11)$$

III. POWER CONVERSION EFFICIENCY AND TOTAL HARMONICDISTORTION (THD %)

In order to determine the efficiency of the proposed inverter, it is necessary to determine the value of conduction and switching power losses generated by the semiconductor components. Basically, the main losses in semiconductor components such as IGBTs and diodes are categorized into two groups: conduction loss (P_{con}) and switching loss (P_{sw}) as follows:

$$P_{SW\_IGBT} = \frac{1}{T}\int_0^T E_{on}(t)i(t)dt + \frac{1}{T}\int_0^T E_{off}(t)I(t)d(t) \quad (12)$$

$$P_{SW\_diode} = \frac{1}{T}\int_0^T E_{rr}(t)i(t)dt \quad (13)$$

Where $E_{on}(t)$ is a turn-on loss and $E_{off}(t)$ is a turn-off loss. Switching losses $E_{on}(t)$ and $E_{off}(t)$ are experienced during the ON and OFF states, respectively. While $E_{rr}(t)$ is the reverse recovery loss of the diode, the majority of switching loss, which is experienced when the diode is turned OFF (OFF state)

$$P_{con\_IGBT} = \frac{1}{T}\int_0^T V_{on\_IGBT}\, i(t)dt \quad (14)$$

$$P_{con\_Diode} = \frac{1}{T}\int_0^T V_{on\_diode}\, i(t)dt \quad (15)$$

Conduction power losses of IGBT and diode are approximated based on their forward voltage drops V_{on} IGBT, V_{on} diode, and the instantaneous current $i(t)$ flowing through IGBT or diode. The total losses P_t are expressed as follows:

$$P_t = P_{con} + P_{sw} \quad (16)$$

Once the total semiconductors losses P_t in the introduced inverter are defined, the relative inverter efficiency is determined based on the following expression:

$$n\% = \frac{P_{out}}{P_t + P_{out}} \times 100 \quad (17)$$

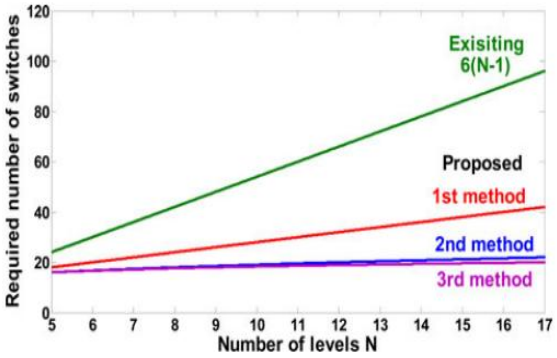

Fig.3. Comparison of required number of switches among existing inverters and the proposed topology

Moreover, the proposed inverter has been tested under different modulation indices (*Ma* = 0.9, 1, and 1.15). THD% of the output voltage can be calculated by

$$\text{THD\%} = \frac{\sqrt{\sum_{k=2}^{\infty} V_k^2}}{V_1} \times 100\% \quad (18)$$

Where V_1 and V_k are the fundamental component and harmonic order, respectively. NPC, FC, and CHB multilevel inverters have been tested under the same operating conditions.

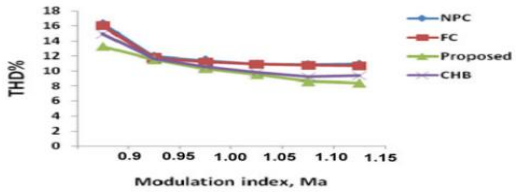

Fig.4. NPC, FC, CHB, and proposed inverter: line-to-line voltage THD%versus *Ma* .

The goal of this test is to compare the proposed inverter with the existing inverters in term of THD%. It can be seen that the THD% of all inverter is slightly different. The measured values of THD% for the proposed inverter are within a range of 8.4–13.25%. As a result, the proposed inverter essentially adds the attractive aspects of the traditional two-level inverter such as less power components, simple working principle, and minimum conduction power loss to the main advantages of the multilevel inverter such as low THD% and high output voltage quality.

IV. PERFORMANCE OF THE INDUCTION MOTOR

The sinusoidally-distributed flux density wave produced by the stator magnetizing currents sweeps past the rotor conductors, it generates a voltage in them. The result is a sinusoidally-distributed set of currents in the short-circuited rotor bars. Because of the low resistance of these shorted bars, only a small relative angular velocity, r, between the angular velocity, s, of the flux wave and the mechanical angular velocity of the two-pole rotor is required to produce the necessary rotor current. The relative angular velocity, r, is called the slip velocity. The interaction of the sinusoidally-distributed air gap flux density and induced rotor currents produces a torque on the rotor. The typical induction motor speed-torque characteristic is shown in Figure.

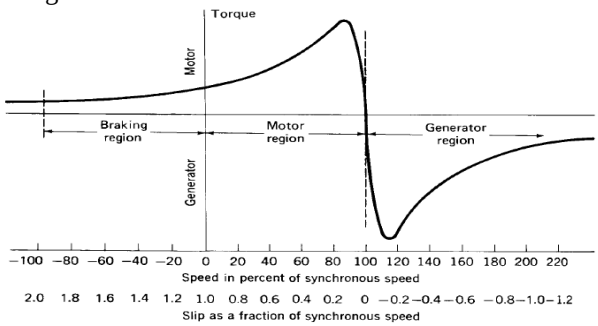

Fig.5. Speed-torque characteristics of induction motor

An induction motor (IM) is a type of asynchronous AC motor where power is supplied to the rotating device by means of electromagnetic induction. An electric motor convert's electrical power to mechanical power in its rotor. There are several ways to supply power to the rotor. In a DC motor this power is supplied to the armature directly from a DC source, while in an induction motor this power is induced in the rotating device. An induction motor is sometimes called a rotating transformer because the stator (stationary part) is essentially the primary side of the transformer and the rotor (rotating part) is the secondary side. Induction motors are widely used, especially poly phase induction motors, which are frequently used in industrial drives. When induction motors are given supply, they draw the current as I_a= As initially E_b= 0 Motor draws a very high current initially; due to which voltage dip will forms, which show the effect on the power system network. In order to avoid such problems a effective controlled APF is placed without effecting the power quality or the motor performance characteristics.

V. MATLAB CIRCUIT & SIMULATION RESULTS

This section deals with the simulation validation of the proposed multilevel inverter topology. The validity of the proposed multilevel inverter is demonstrated with simulation results. Simulation was done by using MATLAB/ Simulink software.

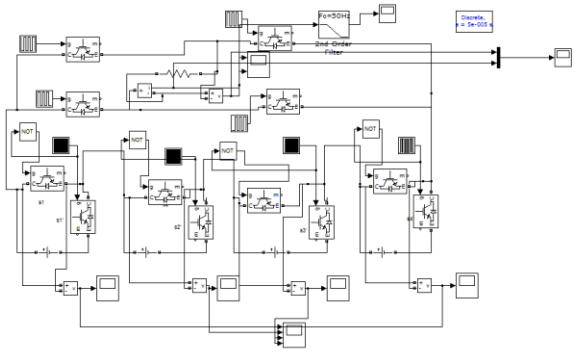

Fig.6. Simulation circuit for one phase 31 level multilevel inverter

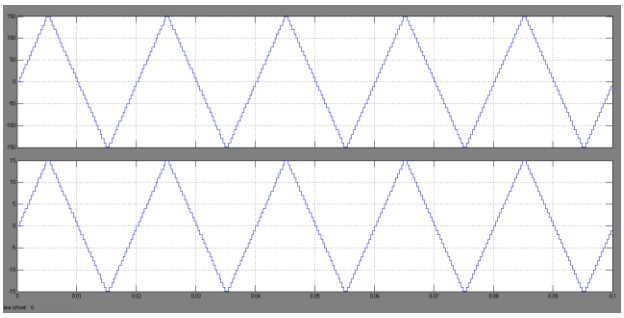

Fig.7. Simulation results of voltage& current for one phase 31 level multilevel inverter

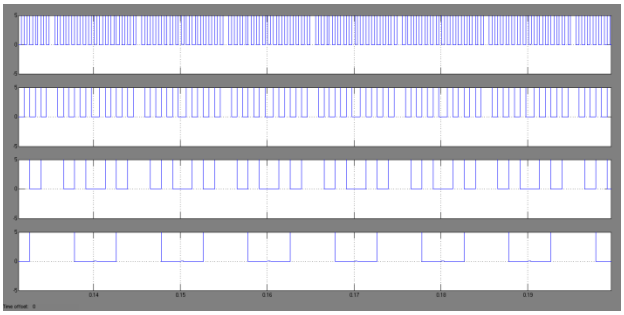

Fig.8. Gate pulses for multilevel inverter switches for one phase

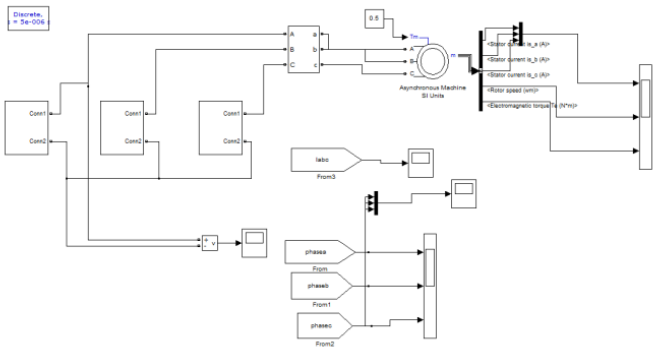

Fig.9. Simulation circuit for three phase 31 level multilevel inverter

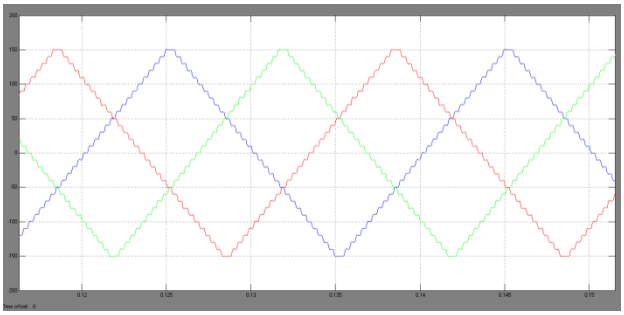

Fig.10. Simulation results of voltage for three phase 31 level multilevel inverter

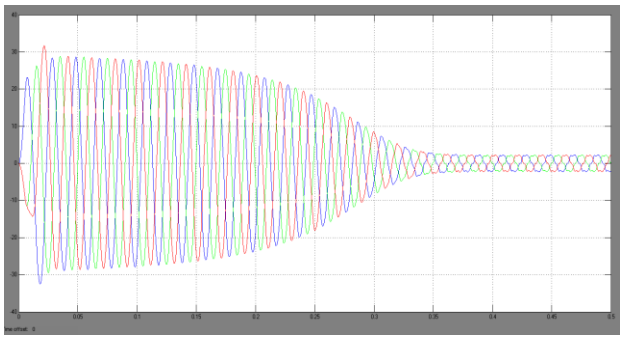

Fig.11. Simulation results of current for three phase 31 level multilevel inverter

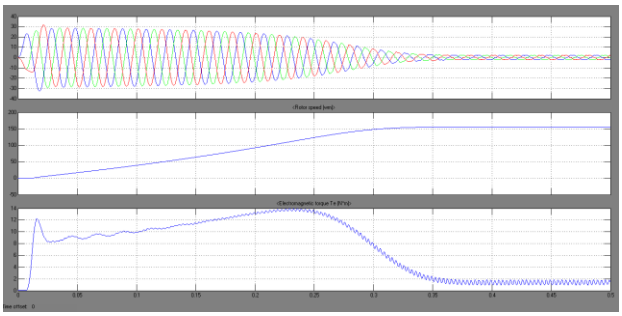

Fig.12. Simulation results of multilevel inverter fed induction motor drive for three phase currents, speed, and electromagnetic torque

CONCLUSION

The proposed topology employs twelve switches and four DC sources, the number of output voltage levels becomes thirty-one .In this project first single phase 31-level novel cascaded multilevel inverter is proposed with series connection of sub multilevel inverters and there after proposed topology is extended to a novel three phase 31-level cascaded multilevel inverter fed induction motor drive. In this topology electromagnetic torque, speed, three phase currents of induction motor are observed. As the number of levels increases the harmonics are reduces.. This topology offers very less THD (ic) THD=1.25. The operation and performance of the proposed a single-phase 31-level multilevel inverter and three phase 31-level with induction motor drive is verified by MATLAB/ SIMULINK.

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