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A Survey on Design of Low Power Low Voltage Circuit using CMOS Ternary Logic

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***Abstract*— Binary logic and devices have been in use since inception with advancement and technology and millennium gate design era. Now binary logic has become tedious and complicated. For this purpose the low power and low voltage arithmetic and logic circuit designed. In this paper we will presents the design and performance of Arithmetic and Logic circuit using Ternary logic and CMOS design styles. The design is targeted for the 45nm CMOS technology. Design tool for simulation will be MICROWIND 3.1 software and DSCH tool. We will estimate area, power and delay and the design of arithmetic circuit with optimized number of transistors as compared to binary circuit.**

***Index Terms*—Logic, Ternary, CMOS, Arithmetic Circuit, Low Power, Low Voltage.**

I. INTRODUCTION

In new technologies, most delay and power occurs in the connection between gates. When designing a function using Ternary logic or Multiple valued logic, need less gates, which implies less number of connections and the less delay. The ternary logic or trivalent logic is one of logical calculi in which there are more than two possible truth value. But Logical calculi are bivalent. There are only true and false possible values for any proposition. Two value and three value logic i.e. (True, false and intermediate) proposed by first author Lukasiewiczs. In this technology more than one or two value logic is implementing. Ternary logic means more than two truth value (0,1) logic i.e. n-value logic for n > 2. Here we implement three truth value logic i.e. (0,1,2) i.e. 2 for true, 1 for intermediate and 0 for false.

There are two modes i.e. current mode and voltage mode, where MVL is implemented. In current mode, in terms of output current MVL states are defined, which is an integral multiple of reference current and in voltage mode, MVL states are in terms of distinct voltage levels. In voltage mode operation of the circuit three distinct logic levels are defined in terms of voltage i.e. Low voltage level corresponds to logical state 0; intermediate to logical state 1; high to logical state 2 respectively.

- TERNARY LOGIC SYSTEMS

In this section, ternary logic system is described. The system includes a set of logic gate operators. The circuits can be designed using them. As discussed earlier ternary logic offers significant advantages in development. It is used to design entry method for our planned project.

- TERNARY LOGIC GATES

In ternary logic system, logic levels ranges from 0 to 2 as against 0 and 1 in binary logic. The logic systems uses logic gates and their operations is known as operators. The gates and operators can be interchangeably used. The following ternary gates/operators are in use and have been considered in our project.

1. NOT GATE – A NOT gate have one input and produce one output in ternary algebra. These gates are known as fundamental operator. Truth table gives the output 0; in case of when input is 2. Gives output 1; in case of input is 1. And when output is 2; then input would be 0. Their truth table and symbolic representation given below.

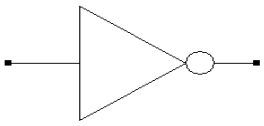

Fig.1.Ternary NOT Gate

Table.1.Ternary NOT Gate Truth Table

Operand	A	0	1	2
Output	$\bar{A}$	2	1	0

2. NAND GATE - A NAND gate have two inputs and produce one output in ternary algebra. These gates are known as a functional operator. Truth table gives output 2; in case of when input is 00. Gives output 2; in case input is 01. Gives output 2; in case input is 02, respectively. Their truth table and symbolic representation given below.

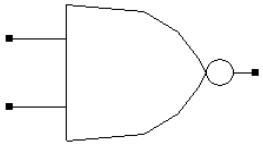

Fig.2. Ternary NAND Gate

Table. 2.Ternary NAND Gate Truth Table

Operand	A	0	1	2	0	1	2	0	1	2
	B	0	0	0	1	1	1	2	2	2
Output	$\overline{AB}$	2	2	2	2	1	1	2	1	0

3. NOR GATE- A NOR gate have two inputs and produce one output in ternary algebra. These gates are known as a functional operator. Truth table gives output 2; in case when input is 00. Gives output 1; in case when input is 10. Gives output 0; when input is 02,and so on. Their truth table and symbolic representation given below.

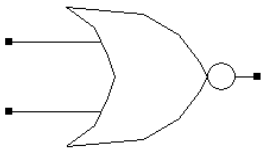

Fig.3.Ternary NOR Gate
Table.3.Ternary NOR Gate Truth Table

Operand	A	0	1	2	0	1	2	0	1	2
	B	0	0	0	1	1	1	2	2	2
Output	$\overline{A+B}$	2	1	0	1	1	0	0	0	0

II. RELATED WORK

1] A. P. Dhande, V.T.Ingole [10] This paper presents 3-valued R-S & D type of flip-flops is studied and described. To implement single clocked gates the minimum number of transistors are used. Less power consumption and speed of operation achieved.

2] Boris Svilicic, Antun Kras 2006[5] This paper examines issues related to the future development of CMOS technology. There is no alternative logic technology is evolving to threaten the CMOS dominance within cost or performance products on the market today. CMOS provides lower power dissipation, higher packing densities and higher circuit speeds.

3] A.P.Dhande, R.C.Jaiswal, S.S.Dudam 2007 [9] This paper presents, the VHDL modeling and simulation of 1-bit multiplier circuit and T gate is described. The proposed work describes basic procedure & establishes VHDL as tool for simulation of ternary circuits and systems. To synthesis and to verify the performance of ternary logic circuits, the proposed simulator can be used.

4] Omid Hashemipour, Akbar Doostaregan, and Keivan Navi [4] 2010 In this paper, a low power and high performance Standard Ternary Inverter for CMOS technology has been proposed. Less power consumption can be achieved using MOS transistor and capacitor. Operation and performance of the proposed design has been examined and simulated by using Synopsys HSPICE tool.

5] R.K.Nagaria,S.S.Mishra and Adarsh Kumar Agrawal 2010[1] In this paper, author reviewed various design techniques for XOR-XNOR circuit. Evaluates & compares the performance of various design techniques of XOR-XNOR circuits based on delay, PDP, EDP etc. Very low power consumption and a very high speed performance can be achieved.

6] Kanchan S. Gorde 2010[2] This paper presents, design and simulation of ternary logic based arithmetic circuits is explained. At ±5V power supply voltage STI, PTI and NTI inverters have been designed for operation. Simulation have been carried out by using MICROWIND and SPICE software.

7] Mariana Aguirre-Hernandez, Monico Linares- Aranda 2011 [7] In this paper author describes all the detail information regarding to design and performance comparison of full adder using alternative internal logic structure. Full adder were built in combination with pass-transistor powerless or groundless logic styles and designed with a TSMC 0.18-m CMOS technology. From this paper we got information regarding to the problem occur during the design of full adder. Also we get the alternative structure which is used for designing adder.

8] Rajendra Kumar Nagaria, Sudarshan Tiwari, and Subodh Wairya 2011[11] This paper presents a comparative study of high-speed and low-voltage full adder circuits. Using hybrid-CMOS design style with pass transistor a new full adders designed are presented in this paper that targets low PDP. An alternative internal logic structure for designing full adder cells is introduced.

9] V.T.Gaikwad, P.R.Deshmukh 2012 [12] This paper describes the architecture, design & simulation of ternary logic gates. Reducing the component count and overall power dissipation and improving the transition time. Design of the circuits are verified and analyzed by using Microwind3.1 with 45 nm technology.

10] M.B. Srinivas, Chetan Vudadha, Sreehari V 2012[3] This paper presents a multiplexer based methodology for design of ternary logic circuits. CNFET based ternary and binary circuits are used to implement the proposed methodology. Simulations results indicate that the proposed 1-bit half adder has 27% less delay and 23% lower power delay product, when compared to the existing design. Existing as well as proposed design methodology, have been performed in HSPICE using the CNTFET model.

11] Bhavna Jharia, Priyanka Rathore 2014[6] This paper presents comparison of different full adder circuits which are made of various logic styles. On the basis of comparison of different full adder circuits which are made of various logic styles and suggests the best technique of designing on the basis of performance. Power consumption and area parameters are considered.

12] Shruti Tiwari and Dwejendra Arya 2014[8] This paper presents modeling and simulation of low power 1 bit CMOS full adder cells. The highest speed of operation i.e. minimum delay is achieved by using proposed circuit. Very low leakage power consumption, the speed of operation is modest i.e. intermediate delay is achieved by the circuit.

III. PROPOSED WORK

In this paper low power low voltage circuit using CMOS ternary logic will design to overcome the drawback of binary logic. And arithmetic and logic circuits will built in optimized form that means with minimum number of transistors in order to reduce power consumption. For the design of digital system such as the implementation of the half adder, full adder, comparator, multiplier; T-gates are required for the implementation of arithmetic and logic circuits. But it has some disadvantages which is an number of gates more. The digital system become more complex. To overcome these disadvantages, first design the ternary design based on CMOS technology like NOT, NAND, NOR gates which can be helpful for the design of digital system. It will reduced number of count, low power dissipation, reduced propagation delay, and area etc.

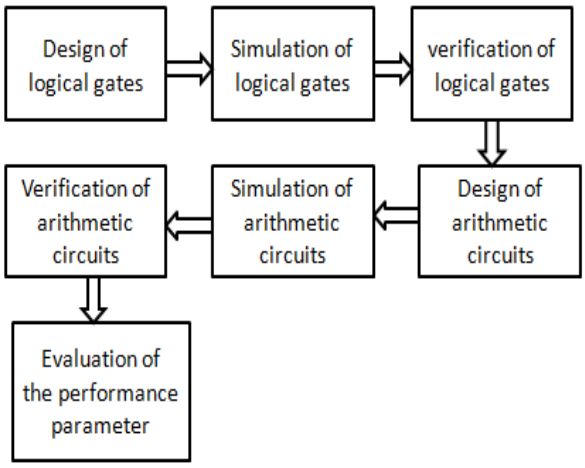

Fig.4.Proposed System Design Flow

Above figure shows Stepwise working of the proposed system. In this model, first we have to design schematic of logic gates like NOT, NAND and NOR gate using DSCH tool. After CMOS schematic of logic gates, we make simulation and verification of logic gates. After made the verification, we have to draw the CMOS layout using Microwind 3.1 software and evaluate the parameters. Similarly, we have to design arithmetic circuits using these logic gates in DSCH tool and MICROWIND 3.1 software. Then we make simulation and verification of arithmetic circuits and evaluate the parameters.

IV. CONCLUSION

A ternary logic circuit processing environment that it offers ease of ternary logic circuit design and development platform of ternary logic system. As the binary to ternary circuit is feasible and efficient in terms of designing while being implemented in CMOS technology, as the technologies are becoming more complex, ternary logic will be the future of circuit design. In this paper, we will present a design of various arithmetic and logic circuits like inverter, NOR gate, NAND gate, half adder, full adder, comparator and multiplier etc. combined in a single unit this technique helps in reducing power consumption, propagation delay, and area of circuits while maintaining low complexity of logic design.

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