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Dynamic Threshold MOS (DTMOS) And its Application

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***Abstract*— In this paper dynamic threshold MOS (DTMOS) and its application in a current mirror is discussed. The input/output characteristics of the proposed circuit are discussed. DTMOS technique meets the requirement for the low voltage and low power for the design of analog circuits. Due to larger current driving capacity and low leakage current, DTMOS is attractive for low power applications. In this work high performance super cascode CM is analyzed using DTMOS technique. The designed circuit is simulated using cadence spectre tool and the technology used is 180µm.**

***Index Terms*— CMOS, DTMOS technique, Input resistance, Output resistance, Super cascode configuration, High performances, Low power.**

I. INTRODUCTION

The market demand for portable and efficient electronic devices have pushed the industry to design chip with high integration density, low power consumption and better performance .To obtain these objectives the technology size of the CMOS has to face constant downscaling. As the technology is being reduced day by day with the reduction of channel size i.e. Length of the MOSFET, the other parameter dimensions also need to be minimized. Obtaining lower power supplies has become an important aspect in today's analog and digital circuit design. For existing design methodology in which the design of a low voltage circuit, the power supply must be at least equal to the sum of the magnitude of the cascode p-type and n-type threshold voltage. In the literature several technique such as sub-threshold, self cascade, floating gate, bulk driven, DTMOS, have been proposed to develop a high performance analog circuits under low voltage power supply.

The DTMOS technique in which body (bulk) terminal is connected to the gate terminal is a promising method for achieving enhanced performance without even modifying the existing structure of MOSFET [1].This is the major advantage of DTMOS as it is fully compatible with the conventional CMOS process.

For the existing MOSFET it is necessary to meet the need of $V_{gs} > V_{th}$ for the MOSFET to function in the triode or saturation region. In contrast the DTMOS technique allows even smaller voltage to be set at the input terminal and generate saturation voltage at the output terminal [2]. Thus DTMOS technique is applied in the circuit design to get the enhanced performance especially in the low voltage and low power applications. Today DTMOS technique has attracted strong interest from researchers, especially for the design of the building-block circuits such as OTA, Mixer, and Current mirror. In this paper we have applied DTMOS technique in the design of compact current mirror and evaluated the performance of both the model one with DTMOS technique CM and other without DTMOS technique for 180nm technologies. The paper is organized as follows: the DTMOS technique and its analysis is discussed in section2. Proposed super cascode CM using DTMOS technique is presented in section3. Section4 deals with comparison of measurement and simulation result followed by the wave form using cadence virtuoso tool in 0.8um technology which is followed by the conclusion drawn.

II. BACKGROUND

A. DTMOS TECHNIQUE :

The technique behind the dynamic threshold MOS is that the input voltage V_{bs} is greater than Zero for NMOS and for PMOS it is negative and hence the threshold voltage can be reduced accordingly. The DTMOS structure uses both the gate and the body terminal to provide the signal input. Since in DTMOS both the gate and the body terminal are shorted V_{bs} become the function of the input signal which is applied to the gate terminal thus $V_{bs}=V_{gs}$ is maintained. Due to dynamic body bias, potential in the channel region is strongly controlled by the gate and body terminals, leading to a high transconductance owing to faster current transport. The relation between input signal and V_T is described using the following equation

$$V_{T0} = 2\phi_B + V_{FB} + \frac{\sqrt{2q\varepsilon_s N_a (2\phi_B)}}{Cox} \quad (1)$$

Where V_{FB} is the flat band voltage and ϕ_B is the inversion layer voltage the inversion layer potential, N_a is the channel doping, ε_s is the Si permittivity, q is the electron charge. Considering body biasing, V_T is given as

$$V_T = V_{T0} + \gamma(\sqrt{\Psi s + VBS} - \sqrt{\Psi s}) \quad (2)$$

Where $\gamma = \frac{\sqrt{2q\varepsilon_s N_a (2\phi_B)}}{Cox}$ and V_T is threshold voltage due to body effect. The DTMOS transistor and its small signal model is shown in Fig.1.and Fig.2 it has two transconductances, the gate tranconductance (gm) and body transconductance (gmb).And the relation between both the transconductance is given by

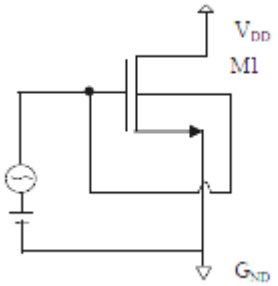

Fig.1 DTMOS Transistor

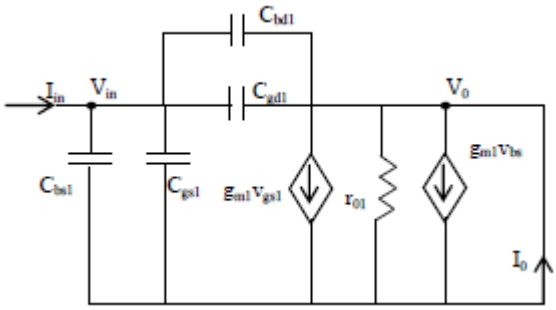

Fig.2 Small Signal Model of DTMOS Transistor

$$\frac{gm}{gmb} = \frac{CBC}{CGC} = 0.2\text{-}0.4$$

Where C_{BC}, C_{GC} are the total body-channel capacitance, the total gate channel capacitance. From Fig.2, the effective input capacitance is given as

$$C_{BC} = C_{gs1} + C_{bs1} \quad (3)$$

From small signal model

$$V_{gs1} = V_{bs1} = V_{in} \quad (4)$$

Applying KCL at the input terminal

$$I_i = V_{in}(sC_{bs1}+sC_{gs1}) + (V_{in}-V_o)(sC_{bd1}+sC_{gd1}) \quad (5)$$

Applying KCL at the output terminal

$$I_o = \frac{V0}{ro1} + g_{mb1}V_{gs1} + g_{m1}V_{gs1} + (V_{in}-V_o)(sC_{bd1}+sC_{gd1}) \quad (6)$$

Using value of V_{gs} from Eq.4 in Eq.6

$$I_o = \frac{V0}{ro1} + (g_{mb1}+g_{m1})V_{in} + (V_{in}-V_o)(sC_{bd1}+sC_{gd1}) \quad (7)$$

For calculation of unity gain frequency make short circuit current gain = unity i.e. I_o (V_o=0) =I_i. Putting V_o = 0 in Eq.5 and Eq.6 and neglecting r_{o1},

$$I_O = I_i$$

$$(g_{mb1}+g_{m1} - sC_{bd1} - sC_{gd1}) = (sC_{bs1}+sC_{gs1} + sC_{bd1}+sC_{gd1})$$

$$\omega_t = \frac{(gmb1+gm1)}{(2Cgd1+2Cbd1+Cgs1+Cbs1)} \quad (8)$$

$$f_t = \frac{(gmb1+gm1)}{2\Pi(2Cgd1+2Cbd1+Cgs1+Cbs1)} \quad (9)$$

Assuming $C_{gd1}=C_{gs1}=C_{db1}=C_{bs1}=C$, $g_{m1}=g_m$,$g_{mb1}=g_{mb}$ in Eq.9 ,we get

$$f_t = \frac{(gm+gmb)}{12\Pi C} \quad (10)$$

Since the transconductance of the DTMOS is greater than the conventional CMOS transistor, from equation (10) it is clear that the frequency bandwidth for the DTMOS increases with the increase in the transistor transconductance.

III. PROPOSED SUPER CASCODE CM USING THE DTMOS TECHNIQUE

The current mirror shown in fig.3 is a high performance CM, which is the combination of the compact CM structure of Garimell et.al and super-cassode configuration. This CM topology provides very low input-resistance , high output impedance and also has high degree of accuracy,but the supply voltage used is 1.5 V and needs to be improved due to market demands for low voltage, low power devices. In the proposed CM,the conventional supercascode CM is utilized with DTMOS technique.

The DTMOS technique allows the lowering of the supply voltage by reducing the threshold voltage dynamically. Schematic for the proposed CM is shown in fig.4. In the proposed work DTMOS technique is used in the feedback loop of the amplifier A_1, A2. In DTMOS technique body of transistor MA11 and MA22 is connected to respective gate of the transistor MA11 and MA22.

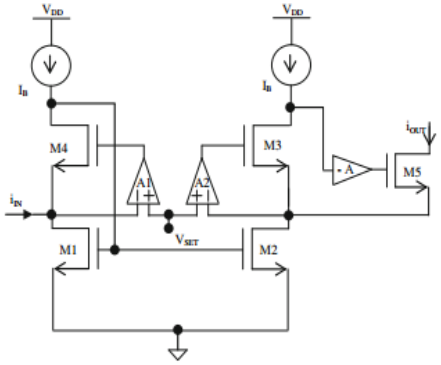

Fig.3 (a) Schematic of the conventional super cascode CM

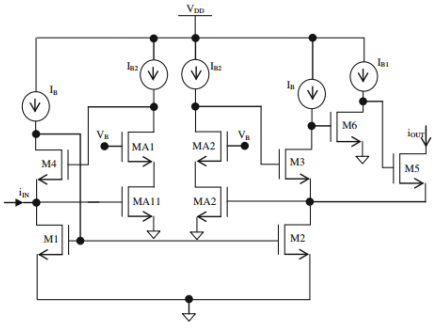

Fig.3 (b) The complete implementation of the super cascode CM

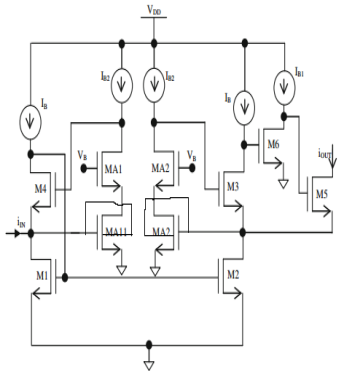

Fig.4 Proposed Modified Design of Super Cascode Structure

This method offers dynamic threshold voltage, which reduces the power consumption of the circuit. Dynamic body bias technique is implemented using triple well CMOS technology which eliminates latch-up and is also compatible with the entire CMOS transistor.

IV. SIMULATION RESULT AND WAVEFORM

In this section simulation result of the proposed CM have been presented. For the design and simulation of the work cadence virtuoso tool in 0.18µm technology is used. The design parameters for the proposed CM are summarized in Table 1.

Table 1 Design parameters of the proposed CM

Component name	Value
Technology	1.8µm
V_{DD}	1V
M1-M5	5µm/0.25 µm
M6	20 µm/0.18 µm
MA11-MA22	1 µm /0.25 µm
I_B	10µA
I_{B1}	100µA
I_{B2}	2µA
V_B	1.5V
i_{IN}	0-500 µA

The super cascode CM and the proposed CM shown in Fig. 3 and 4, is simulated using cadence virtuoso schematic editor and analog design environment. Waveforms for the various parameters are shown below.

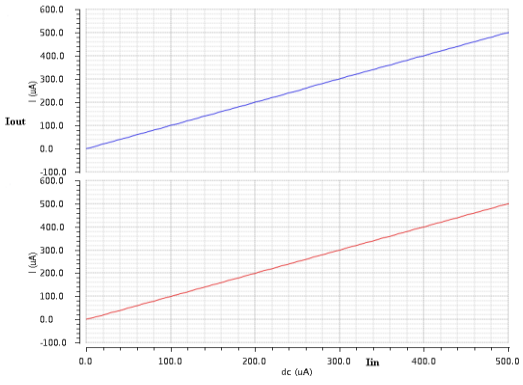

Fig. 5 waveform for output current vs input current of supercascode CM

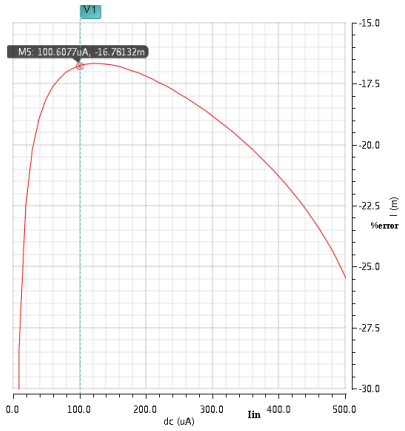

Fig.6 Simulated current matching error ratio of the supercascode CM

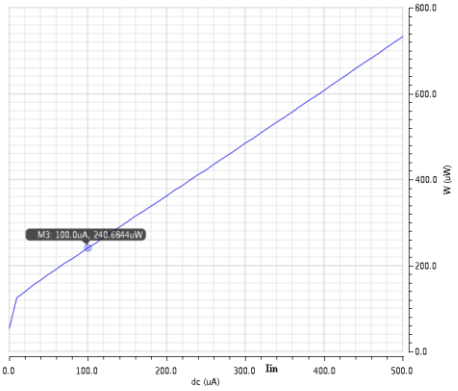

Fig. 7 Waveform for power consumption in supercascode CM

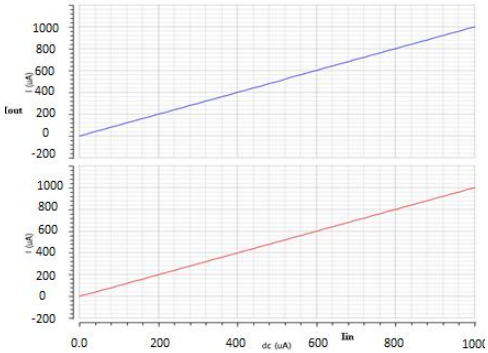

Fig.8 Waveform for output current vs. input current of proposed circuit.

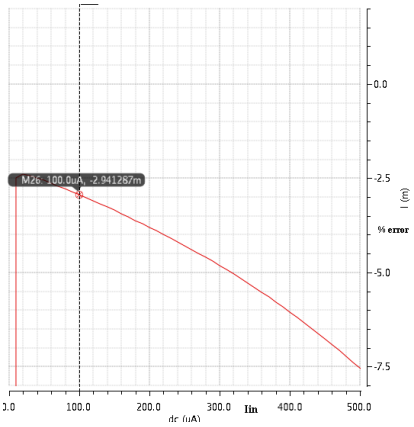

Fig.9 Simulated current matching error ratio of proposed CM

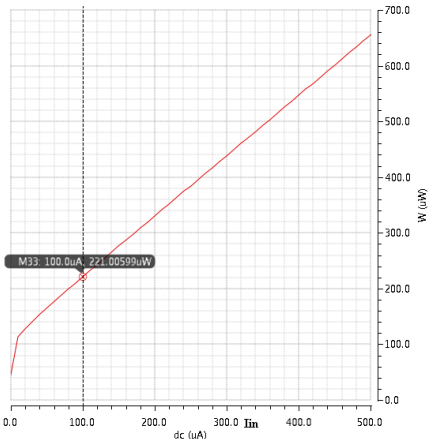

Fig. 4.6 Waveform for power consumption in proposed CM

All the simulation of the supercascode CM and proposed circuit were done under the similar conditions and same technology for fair comparisons It is observed that using DTMOS technique allows to replicate the input current at the output side with very less offset, it also improves the power consumptions of the circuit. Further going for the ac analysis of the circuit bandwidth of the device also increases by applying DTMOS technique since transconductance of the circuit increases. Transistors always work in the saturation region for analog and RF applications therefore analog and RF characteristics of DTMOS in saturation region are also attractive. The performance of analog circuits strongly depends on how the characteristics of the transistors are exploited and mastered.

Table 2 Comparative result of super cascode CM and proposed CM

Parameters	Base paper	Proposed
Technology	0.18µm	0.18µm
Supply voltage	1.5V	1V
Current range	0-500µA	0-1000µA
% Error (at i_{IN} = 100 µA)	0.016	0.002
Power (at i_{IN} = 100µA)	241 µW	221 µW

V. CONCLUSION

In this paper,a modifiefd form of super cascode CM is studied which utilizes DTMOS technique. Modified circuit has high accuracy with very less current copying error. Modified CM consumes less power compared to CM without applying DTMOS technique.

REFERENCES

[1]. E.Sackinger,& Guggenbuhl, W. (1990). "A High-Swing, High Impedance MOS Cascode Circuit", *IEEE Journal of Solid-State Circuits*,Vol .25 No.1,pp 289–298.

[2]. Fariborz Assaderaghi,(1997) Dynamic Threshold-Voltage MOSFET (DTMOS) for Ultra-Low Voltage *VLSI IEEE Transactions On Electron Devices*, Vol. 44, No. 3,pp.23-28.

[3]. Rajput, S. S., & Jamuar, S. S. (2000). A High Performance Current Mirror For Low Voltage Designs. *IEEE Asia–Pacific conference on circuits and systems (IEEE APCCAS)* Vol.23 No.4,pp.270-273

[4]. Xuguang Zhang and Ezz I.El-Mary.(2002), Low-Voltage, Body-Driven CMOS Current Mirror. *Dept. of Electrical & Computer Engineering*, Vol.55, No.7, pp.34-38

[5]. Torralba, A., Carvajal, R. G., Ramirez-Angulo, J., & Munoz, E. (2002), "Output Stage for Low Supply Voltage, High-Performance CMOS Current Mirrors", *Electronics Letters*, Vol.38,No.24,pp.1528–1529.

[6]. Michele Quarantelli, Marco Poles, Marco Pasotti, Pierluigi Rolandi (2003), "High Compliance CMOS Current Source For Low Voltage Applications. *VLSI IEEE Transactions On Electron Devices"*, Vol. 132, No. 3,pp.232-238.

[7]. Xuguang Zhang,(2004), "A Regulated Body-Driven CMOS Current Mirror for Low-Voltage Applications", *IEEE Transactions On Circuits And Systems—II*, Vol. 51, No. 10,pp. 232-236

[8]. Ramirez-Angulo, J., Carvajal, R. G., & Torralba, A. (2004), "Low Supply Voltage High-Performance CMOS Current Mirror With Low Input And Output Voltage Requirements*", IEEE Transactions on Circuits and Systems II*, Vol. 51No.3, pp.124–129.

[9]. Garimella, A., Garimella, L., Ramirez-Angulo, J., Lopez-Martin A. J., & Carvajal, R. G. (2005). "Low-Voltage High Performance Compact All Cascode CMOS Current Mirror", *Electronics Letters*, Vol. 41, No.25, pp.1359–1360.

[10]. Koliopoulos, C., & Psychalinos, C. (2007), "A Comparative Study Of The Performance Of The Flipped Voltage Follower Based Low-Voltage Current Mirrors". *International Symposium on Signals, Circuits and Systems (ISSCS)*,Vol.67,No.13,pp.745-749

[11]. H.Gabbouj W.Guggenbuhl. (2008), "CMOS Current Mirror For Low Power Applications", *IEEE Journal of Solid-State Circuits*, vol. 89,No.11, pp. 389–398.

[12]. Aggarwal, B., & Gupta, M. (2009). "Low-Voltage Cascode Current Mirror Based On Bulk-driven MOSFET and FGMOS Techniques", *IEEE .International conference on advances in recent technologies in communication and computing*. Vol.56 No.27 pp. 473–477

[13]. Lakkamraju, N., & Mal, A. K. (2011), "A Low Voltage High Output Impedance Bulk Driven Regulated Cascode Current Mirror", *International conference on electronics computer technology (ICECT)* Vol. 3, No.31 pp. 79–83.

[14]. Tikyani, M., Pandey,(2011), "A New Low-Voltage Current Mirror Circuit With Enhanced Bandwidth", *in Proceedings of the International Conference on Computational Intelligence and Communication Networks*.Vol.31,No.41, pp. 42–46.

[15]. Gupta, M., Aggarwal, B., & Gupta, A. K. (2013), "A Very High Performance Self-Biased Cascode Current Mirror For CMOS Technology", *Analog integrated circuits and signal processing mixed signal letter (Springer)*,Vol. 75,No.4,pp.67–74.

[16]. N. Raj, A.K. Singh and A.K. Gupta (2014) "Low-Voltage Bulk-Driven Self-Biased Cascade Current Mirror With Bandwidth Enhancement , *Electronics Letters*, Vol. 50 No. 1 pp. 23–25

[17]. V.Niranjan,A.Kumar, S. B. Jain,(2014), "Maximum Bandwidth Enhancement Of Current Mirror Using Series-Resistor And Dynamic Body Bias Technique", *Radio engineering*, Vol. 23,No.3,pp.321-328.

[18]. Bhawna Aggarwal • Maneesha Gupta •Anil Kumar Gupta (2013) "A very high performance self-biased cascode current mirror for CMOS technology", *Analog Integr Circ Sig Process, Vol.75*, pp.67-74.

[19]. Bhawna Aggarwal • Maneesha Gupta •Anil Kumar Gupta • Sahil Bansal(2014), "A very high performance compact CMOS current mirror", *Analog Integr Circ Sig Process* ,Vol.81,No.3,pp.367-375.

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