ABSTRACT - This project reveals the design of a comparator for pipeline ADC. These comparator is designed using preamplifier and latch. The preamplifier latch comparator which we have design gives high speed, low offset and low power dissipation very useful for pipeline ADC design.

CMOS is a Complementary Metal Oxide Semiconductor which is a combination of PMOS & NMOS. This technology is used because of it very low power dissipation. The comparator is a circuit that compares an analog signal with another analog signal or reference and outputs a binary signal based on the comparison. The pre-amplifier used in this design is a simple common source differential amplifier with PMOS transistors as active loads. A latch is defined as the memory unit that stores the charge on the gate capacitance of the inverter. By using both of these in a combination can obtain high speed and low power dissipation pipeline ADC.

For simulation of these comparator Tanner EDA is used, in which EDA is an Electronic Design Automation. The 13 version of Tanner EDA tool is used for simulation.

We have observed the Simulation results are presented including offset voltage, power dissipation, clock frequency and noise calculation.

Through simulation we have obtained parameters of the comparator like offset voltage is 280.7 nV. As the clock frequency of comparator is achieved 100 MHz and low power dissipation is 0.27mW.

INDEX TERMS— Analog to Digital Converter, Comparator, Tanner EDA

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1. INTRODUCTION

In today’s world, where demand for portable battery operated devices is increasing, a major thrust is given towards low power methodologies for high speed applications. This reduction in power can be achieved by moving towards smaller feature size processes. One such application where low power dissipation, low noise, high speed, less Offset voltage is required is Analog to Digital converters for mobile and portable devices. In high speed ADC, comparators influence the overall performance of ADC directly. This thesis describes a high speed, low offset and low power dissipation preamplifier-latch comparator very useful for pipeline ADC design. The preamplifier latch comparator, which combine of an amplifier and a latch comparator can obtain high speed and high resolution. The amplifier which is added before the latch can reduce offset voltage to obtain a high speed. Thus, by considering factors of speed and offset voltage, preamplifier-latch comparator is the choice for a high speed ADC.

2. BASIC OF COMPARATOR

2.1 COMPARATOR OPERATION - The comparator is a circuit that compares an analog signal with another analog signal or reference and outputs a binary signal based on the comparison. The comparator is widely used in the process of converting analog signal to digital signals. In the analog to digital conversion process, it is necessary to first sample the input. This sampled signal is then applied to a combination of comparators to determine the digital equivalent of the analog signal.

2.2 COMPARATOR PARAMETERS

2.2.1 OFFSET VOLTAGE - The offset of this stage is dependent on both the input amplifiers and the latching stage. Input-offset voltage can be a particularly difficult problem in
comparator design. Figure 2.1 shows the offset-cancellation arrangement for offset voltage measurement. Thus, the proposed offset cancellation achieves not only low offset voltage but also low Power consumption. Moreover, the proposed circuit topology can improve the comparator noise and reduce the clock driving requirement compared with a conventional comparator.

![Figure 1: Offset-cancellation arrangement for offset voltage measurement](image)

The comparator connected in the unity-gain configuration so that the input offset is available at the output [14]. In order for this circuit to work properly, it is necessary that the comparator be stable in the unity-gain configuration. This implies that only self compensated high-gain amplifiers would be suitable for auto zeroing.

The offset-voltage of the comparator is reduced, using either input offset storage (IOS) or output offset storage (OOS) around the comparator preamplifier. In the IOS configuration, the preamplifier must be stable in the unity feedback configuration. Also, the MOSFETs of the preamplifier must remain in saturation when the offset voltage is stored on the capacitors. For the IOS scheme the input storage capacitance must be much larger than the input capacitance of the preamplifier, so that the storage capacitors don’t attenuate the input signals. The total offset voltage of the comparator consists of the sum of both source coupled pairs. The offset of one differential pair has the well-known dependency on the mismatch of the threshold voltage $\Delta V_T$, load resistance $\Delta R_L$, and transistor dimensions $\Delta \beta$ and their corresponding average values $V_T$, $R_L$, and $\beta$ [17]

$$V_{OS} = \Delta V_T + \frac{V_{oc} - V_T}{2} \left( \frac{\Delta R_L}{R_L} + \frac{\Delta \beta}{\beta} \right)$$

2.2.2 NOISE- Moreover, a comparator noise determines the signal to noise ratio of ADCs. This is especially true for a high speed pipeline ADC which requires a sufficiently low noise comparator to prevent conversion errors. The noise generated in MOSFETs is due to thermal and flicker noise ($1/f$ noise, pronounced “one over f noise”). For hand calculation, the thermal noise effects due to the parasitic resistances will be neglected. If this is the case, the only noise sources we will evaluate using hand calculations are the channel thermal and flicker noise contributions. Both of the noise sources can be reflected back to the gate of the MOSFET. Thermal noise generated due to random thermal motion of electron and is independent of the dc current flowing in the component.

2.2.3 CLOCK FREQUENCY- An analog signal is sampled at regularly-spaced time intervals $T$. The discrete Samples of $x_a(t)$ are denoted by $x(n) = x(nT)$ for $-\infty < n < \infty$ where $x(n)$ is the Discrete-time sample of the continuous-time analog signal $x_a(t)$ every $T$ seconds. The clock frequency “$f_c$” is defined as the reciprocal of the time interval $T$, as [19]

$$f_c = \frac{1}{T}$$

The clock frequency has to be equal or greater than twice of the frequency bandwidth of analog signals.

2.2.4 POWER DISSIPATION- The power dissipated by comparator is simply the product of the sum of the current flowing in the current source with power supply voltage. We were primarily considering high speed and low voltage. Dynamic comparator power dissipation resembles that of digital gates, which have a power dissipation given approximately by [20]:

$$P = f_c V_{DD}^2$$

3. DESIGN OF A COMPARATOR

In pipeline A/D converter, internal comparator must amplify small voltage into logic levels and it is depending on the algorithm use, encoding process can often be pipelined with the comparator function. Since the encoding process is faster...
than the comparator function, the maximum conversion rate for the ADC is limited by the response time of its comparators. Therefore, the design and optimization of the comparators is critically important [30]. The comparator is basically excluded from application to the high speed A/D converters with high resolution owing to its large offset voltage which significantly affects the resolution. As a consequence, the preamplifier-latch comparator topology in which an amplifier is added before a latched comparator, aiming at achieving small offset voltage and high speed, has been developed [31]. The preamplifier latch comparator [32], which combine of an amplifier and a latch comparator can obtain high speed and low power dissipation. This designed comparator consists of the input amplifier and latch stage. The preamplifier stage amplifies the input signal to improve the comparator sensitivity and isolate the input of the Comparator from switching noise coming from positive feedback stage [34]. The latch stage is used to determine which of the input signals is larger and extremely amplifies their difference.

3.1 Preamplifier- The pre-amplifier used in this design is a simple common source differential amplifier with PMOS transistors as active loads. Shown in Fig.3.2 Pre-amplifier is followed by a small circuit which is basically used for two main functions. First it is used to avoid the kick back effect from the latch to the input signal which is made possible by using two NMOS transistors which operation on the clock. Noise observed at the input signal which is produced due to high voltage variations at the regenerative nodes of the latched and is coupled to the input through the parasitic capacitance of the transistors [35]. The second purpose of using the kick back protection circuitry is to create charge imbalance in the latch when it switches from reset mode to regeneration mode.

3.2 LATCH- A latch is defined as the memory unit that stores the charge on the gate capacitance of the inverter. A simple dynamic latch is shown in Fig.3.3.

3.3 DESIGN AND ANALYSIS - The comparator presented in this paper is made up of the preamplifier –latch circuit schematic view of the design is shown in Fig. 3.4. In this design when clk is low, the latch is disabled and difference between the input and reference is amplified by the front-end amplifier. If clk is goes high, the amplifier is disabled and the latch is being to amplify the difference established at its input to generate logic levels at the output. Preamplifier consists of two different inputs, which are made up of NM0, NM6, NM7 and NM5. PM2, PM3, connect crossways in order to turn into positive feedback and also increase the plus
of preamplifier. NM9, NM1, NM4, PM14 are considered as switches. Fig. 2 presents the schematic view of the proposed design. In this when clock (Clk) is low, the latch comparator is reset, and at this time Clk1 is high, latch-comparator can receive the amplified signal of preamplifier. The use of a clock eliminates the need for an output buffer used in level shifting the output of the decision circuit. The discrepant voltage of loading in NM0 and NM6 (port-1) compares the one of the loading in NM7 and NM5 (port-2). This two ports produce different current, after the current passing through the common gate stage, which is connected two output of preamplifier, and produces a voltage difference \((V_{out+}, V_{out-})\), which is sent into of latch comparator. When clk is high, the latch comparator start to work and the voltage difference \((V_{out+}, V_{out-})\) will be amplified by the crossing plus feedback loop and later comparator will keep the state until clk becomes low. The use of a preamplifier before the latch also has the advantage of reducing the input offset voltage of the latch by the gain of the amplifier. The input offset voltage of the comparator will now become that of the preamplifier, which can be autozeroed, resulting in small vales of input offset voltage.

3.4 SIMULATION RESULTS AND DISCUSSION - Finally simulation of the proposed design is done in tanner environment with 32nm UMC Technology and is given in Fig. 6. Simulation results are presented including offset voltage, power dissipation, clock frequency and noise calculation. In this design we have used single power supply i.e. 2.0 V. Through simulation we have obtained parameters of the comparator like offset voltage is 280.7 nV and it is shown in Fig. 3.6 and Fig. 3.7. As the clock frequency of comparator is achieved 100 MHz and low power dissipation is 0.27mW. Fig.3.8, Fig.3.9 and Fig.3.10 are giving the input noise response is 32.84 mV/sqrt (Hz), output noise response is 264.1 nV/sqrt (Hz) and pnoise response is 7.671µV/V respectively. Finally we have obtain the gain is 48.31 Db.

Simulation results:

**Fig 6**: Simulation results of comparator

**Simulation Results**

**W-EDIT**

**Fig 7**: Transient response of comparator
4. 8-bit pipeline ADC Design

The 8-bit ADC consists of 8 stages and 8 comparators for determining the signs of the 8 outputs. Each stage takes its input, multiplies it by 2, and adds or subtracts the reference voltage depending on sign of the previous output. The comparator output from an 8-bit digital representation of the bipolar analog input to the first stage each of the stage of the pipeline ADC are identical. The ith stage takes the output of the previous stage, \( V_{i-1} \), and during the next clock cycle it compares this voltage with ground and outputs the ith-bit. In addition, the voltage \( V_{i-1} \) is multiplied by 2 and the reference voltage, \( V_{ref} \), are added or subtracted depending on the whether the comparator output is low or high, respectively. This is mathematically described as [43]

\[
V_i = 2V_{i-1} - b_{i-1} V_{ref}
\]

Where \( b_{i-1} \) is given as

\[
b_{i-1} = \begin{cases} 
+1 & \text{if } V_{i-1} > 0 \\
-1 & \text{if } V_{i-1} < 0 
\end{cases}
\]

The operation of the ith is graphically portrayed in Fig. 5.2, where the output and input of the ith stage normalized to \( V_{ref} \) are plotted.
4.1 TRANSFER CHARACTERISTIC- The accuracy of pipeline ADC depends on how well the voltage-transfer characteristic of Fig.5.2 can be achieved. The possible errors for the pipeline ADC include gain and offset errors. Gain errors can come from any multiplicative operation such as constants associated with the summing junctions of offset errors can come from the summing junctions

![Output-input characteristics of the ith stage](image)

Fig.12: Output-input characteristics of the ith stage

Where a constant amplitude shift is experienced, independent of the input. Equations (19), (20) and (21) can be rewritten to include the errors as

\[ V_i = A_i V_{i-1} + V_{osi} - b_i A_{si} V_{ref} \]

\[ b_i = \{+1 \text{ if } V_{i-1} > V_{oci}\} \]

\[ b_i = \{-1 \text{ if } V_{i-1} < V_{oci}\} \]

where \( A_i \) is the gain of “2” for the ith stage

\( V_{osi} = \) is the system offset errors of the ith stage

\( A_{si} = \) is the gain of “1” for the summer,

\( V_{oci} = \) is the comparator offset voltage

5. CONCLUSION- Simulation has been done in tanner environment with 32nmUMC Technology under the 2V power supply by Tanner spectre. Comparator able to work at the high clock frequency as 100MHz and clock period was10ns can be used where Low power, high speed and Low offset voltage is the main requirements and it is very much useful for ADC designer. A CMOS comparator utilizing new offset cancellation techniques has also introduced. To achieved a small offset voltage as 280.7nV. Results have been matched with schematic and layout design of the proposed work.

REFERENCES


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