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LOW VOLTAGE FGMOS BASED CURRENT MIRROR

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***Abstract*— This paper presents a high performance current mirror (CM) in which the current range is so high. In this paper, a low power design of current mirror using floating gate MOS transistor is presented. The proposed CM offers extremely high degree of wide operating current range. The proposed CM is being simulated by using CADANCE Virtuoso in TSMC 0.18 µm using CMOS technology, using a single supply voltage of 0.3 V. The circuit is shown to have high current copying accuracy for a range of (0–1000 µA)**

***Index Terms*—.FGMOS, Compliance voltage, Low power, Current mirror.**

I. INTRODUCTION

In today's scenario, the technology has been scaling down. According to the market, there is a growing demand of portable equipment towards the development of low-voltage low-power analog signal processing circuits [4]. The main requirement for low voltage (power) operation is to maintain the same speed, accuracy, and area of current "high-voltage" designs. The low supply voltage increases the battery lifetime and hence reduces the power consumption of the portable equipment [5].

The challenge that are being derived from market requirements is to reduce the power consumption of the circuit. Many new design techniques for low voltage analog circuits are available [3], for instance:-

(a) MOSFETs operating in the sub-threshold region
(b) Bulk driven transistors
(c) self-cascode structures
(d) Floating gate MOS (FGMOS)
(e) The level shifter techniques.

Among these, the low voltage technique FGMOS has gained prior importance due to its ability to reduce or remove the threshold voltage requirement of the circuit.

This paper discusses characteristics of current mirror which is being based on FGMOS. This paper comprises of the following sections, in II (second) section current mirror has been described as per discussed in various literature. The FGMOS have been discussed in section III. The proposed circuit have been discussed in section IV and then in continuation with the simulation result in V.

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II. CURRENT MIRROR

A current mirror is a circuit designed to copy a current through one active device by controlling the current in another active device of a circuit, keeping the output current constant regardless of loading [1, 2]. The current being 'copied' can be, and sometimes is, a varying signal current.

The current mirrors (CM) are the basic element, which are the integral part of VLSI circuits. They are based on analog design. It is one of the basic building blocks in CMOS based analog integrated circuits. The main parameters of current mirror on which its performance depends are input and output impedance, current transfer ratio, bandwidth and input and output voltage requirements [6].

The Current mirror, as known, is a basic building block for various applications like current mode applications and it is also being used in voltage mode applications to bias the circuits like OTA, current conveyers, differential amplifier etc. [3].

It is very useful block in analog and mixed mode circuit applications. Since low power is a very necessary design constraint now a days, so this designed current mirror can be very useful when supply low operation is the primary concern [8, 9].

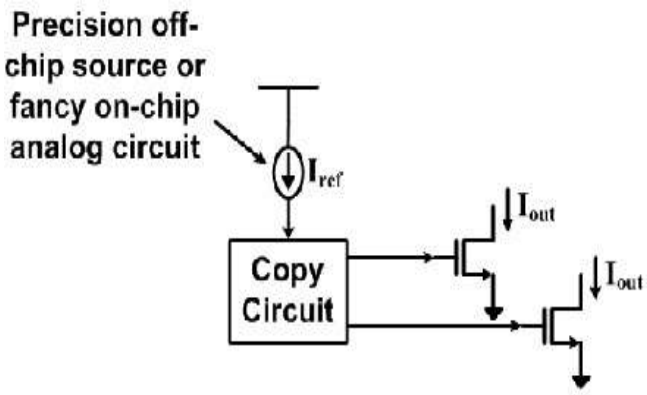
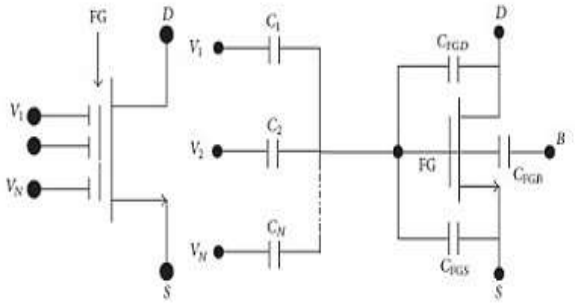


Fig 1: Current Mirror

III. FLOATING GATE MOSFET

FGMOS is a floating gate mosfet or multi input floating gate transistor by which the threshold voltage can be controlled and tuned by the values of capacitors and bias voltage applied [5].



(a) (b)

Figure 2: (a) Symbol of FMGOS; (b) FGMOS equivalent circuit.

The Fig 2 shows the symbol of n-input FGMOS in 2(a) and it equivalent circuit in 2(b). The voltage on floating gate (FG) V_{FG} is given by [7]

$$V_{FG} = \sum_{i=1}^{N} \frac{C_i}{C_T} V_i + \frac{C_{GS}}{C_T} V_S + \frac{C_{GD}}{C_T} V_D + \frac{Q_{FG}}{C_T}$$

Where Ci is the set of input capacitors,

$$C_T = C_1 + C_2 + C_{FGS} + C_{FGD} + C_{FGB}$$

Where C_T is the total capacitance of the gate. C_{FGD}, C_{FGS}, and C_{FGB} are the overlap capacitances of floating gate with drain, source, and bulk. V_D, V_S, V_B are the drain voltage, source voltage and bulk voltage.

Floating Gate MOS technology is a low voltage design technique with its attractive features such as reduced circuit complexity and simplified signal processing chain of a design. [1]. It operates normally below the operational limits of supply voltage levels for a particular technology and thus consumes less power than the minimum power required for a CMOS circuit of same technology without compromising on device performance [2].

There are various applications of FGMOS transistors in neural networks, voltage-controlled resistors, electronic programming, current mirrors, and digital-to analog and analog-to-digital converters, multipliers, squares , operational trans conductance amplifier, etc.

IV. PROPOSED CURRENT MIRROR

In the proposed current mirror the following transistors M2–M4 implement the RGC stage. The over drive voltage ðVDS2Þ of M2 is regulated by M3 and M4 transistors.

In order to yield high output impedance, it follows the same principle as that of cascode but employs a feedback loop amplifier (M4andIB1).This prevents variations in drain-to-source voltage of M2. The Proposed current mirror is realized using conventional gate-driven MOS transistors.

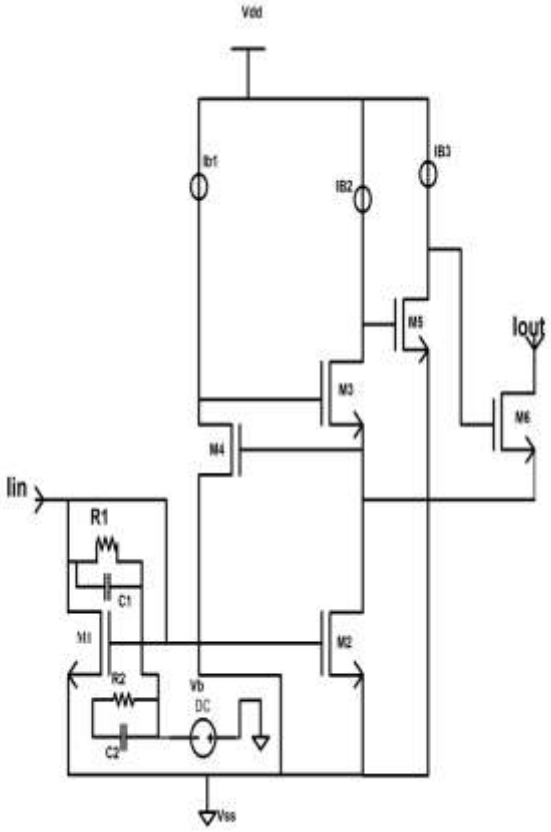


Fig. 3. Proposed current mirror circuit.

The low voltage technique is being used in this circuit for the low power and low supply. The advantage of this technique is linearity.

Table1:W and L of MOS transistors used in proposed CMs.

Transistors	W (μm)	L (μm)	Transistors	W (μm)	L (μm)
M1	25	0.24	M6	5.33	0.24
M2	25	0.24			
M3	10	0.24			
M4	10	0.24			
M5	2.24	0.24			

C1=C2=100pF, R1=R2=100Ff, Vb=0.3V, Vss=±0.3V, Ib1=Ib2=Ib3=10uA

V. SIMULATION

In this section, simulation results of the proposed CM have been presented. The proposed circuit has been simulated by Cadence Virtuoso in TSMC 0.18 lm CMOS technology, using a single supply voltage of 0.3 V.

The fig4 shows the graph between the output current and input current. The current transfer characteristics of proposed circuit from 0to1000 μA is shown in Fig. 4 It shows the input current ranging from 0 to 1000uA as compared to conventional which has range from 0 to 700uA.

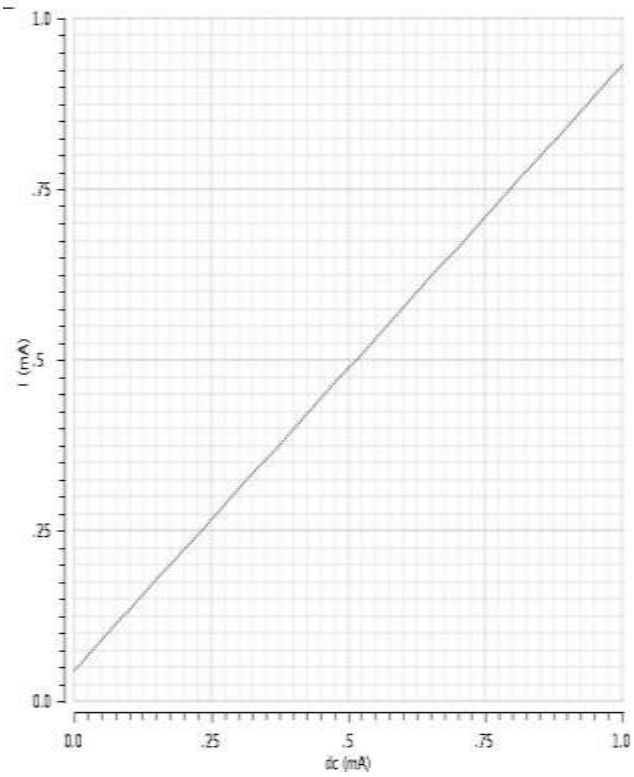


Fig.4 Current transfer characteristics of Proposed for input current ranging from 0to1000 µA.

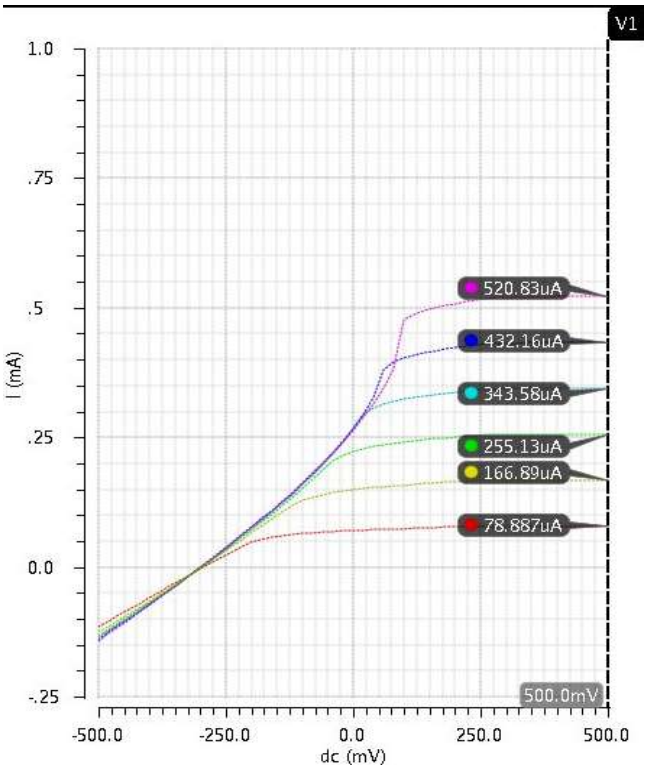


Fig .6 Iout and Vout of proposed CM

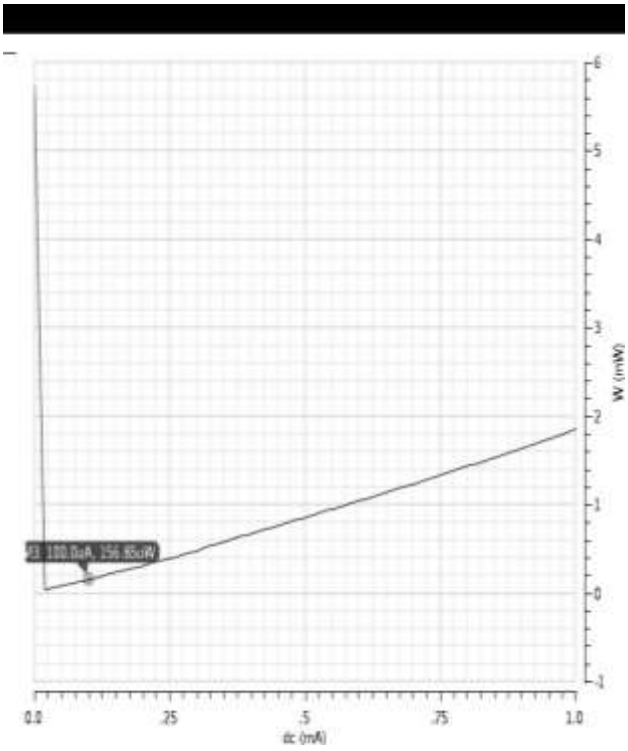


Fig 5: Power consumption of the proposed CM

The fig 5 tells about the power consumption of the proposed CM which is 156.65uW at 100uA.

Table 2: Simulated results for proposed CM

Parameters	Proposed CM
Technology	0.18um
Power supply	0.3V
Input current range	1000uA
Power consumption	156.65uW

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