ISSN:2278 – 7798
International Journal of Science, Engineering and Technology Research (IJSETR)
Volume 5, Issue 9, September 2016

Design and Implementation of Multiple Memory IP Subsystem with Optimal I/O Count

B. HARIKA, MTECH VLSI DESIGN, JNTUK

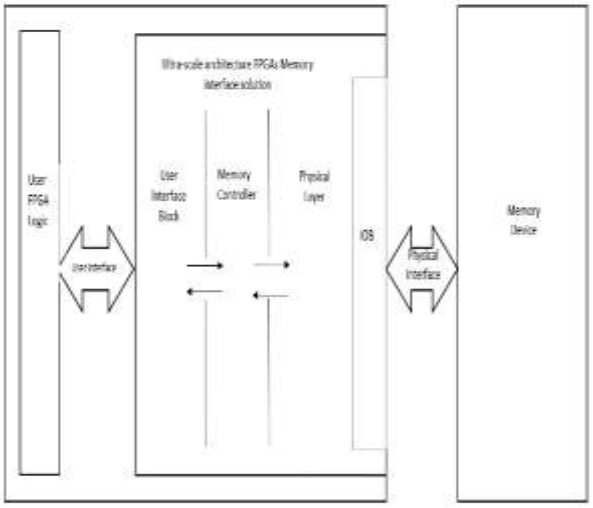
K.RAMA DEVI, MTECH, ASSISTANT PROFESSOR, JNTUK

***Abstract*—Today every design in Field Programmable Gate Array/Application Specific Integrated Circuit (FPGA/ASIC) has multiple memorycontrollers and IPs associated with it. Input/output (I/O) pins count is the major issue in the design of large systems, for selection of Programmable devices FPGAs. Chip I/O pins are an increasingly limited resource and significantly affect the performance, power and cost of multi-core processors. Reduction of I/O count is of major concern for designs at the system level.Here, we present set of rules to optimize I/O count required for implementing multiple memory IPs without violating timing constraints. This will allow users to leave more I/Os available for other peripherals in the system.**

***Index Terms*— Device view analysis, FPGA Interfacing, I/O Banks, I/O pin planning, I/O utilization count, Memory IP, Timing Constraints.**

INTRODUCTION

An external memory interface is a bus protocol for communication from an integrated circuit, such as a microprocessor, to an external memory device located on a circuit board. The memory is referred to as external because it is not contained within the internal circuitry of the integrated circuit and thus is externally located on the circuit board. The external memory interface enables the processor to interface with third level caches, peripherals, and external memory. Some common external memory interfaces includes: DDR4 SDRAM, DDR3 SDRAM, RLDRAM3, QDRII+ SRAMetc.



Memory Interfacing with FPGA devices

As operating speeds increase, device geometries must shrink, increasing the number of circuit elements per chip and thereby increasing the I/O requirement. Increasing speed requirements will also result in a trend away from multiplexed I/O toward dedicated I/O will also have a significant impact on chip I/O counts.

In many high speed data processing applications, packaging technology is the factor that determines

or limits performance, cost, and reliability. Packaging the logic chips presents a greater challenge than the memory devices because they dissipate more power and require more I/O for logic signal communication.

I/O pin planning rules are developed to optimize I/O count utilized while interfacing multiple memory IPs with FPGA. In an FPGA device I/Os are grouped into BANK, and BYTE.

Ultra-scale FPGA device architecture has4 bytes in every I/O BANK, each I/O byte has 13 I/O pins.

When an IP is interfaced with an FPGA, IP I/Os will be connected to FPGA I/Os in the form of banks. All I/Os of a single bank will have same I/O voltage level standards. Earlier if one I/O pin of a bank is utilized during IP interface, then that bank cannot be used to interface any other IP.

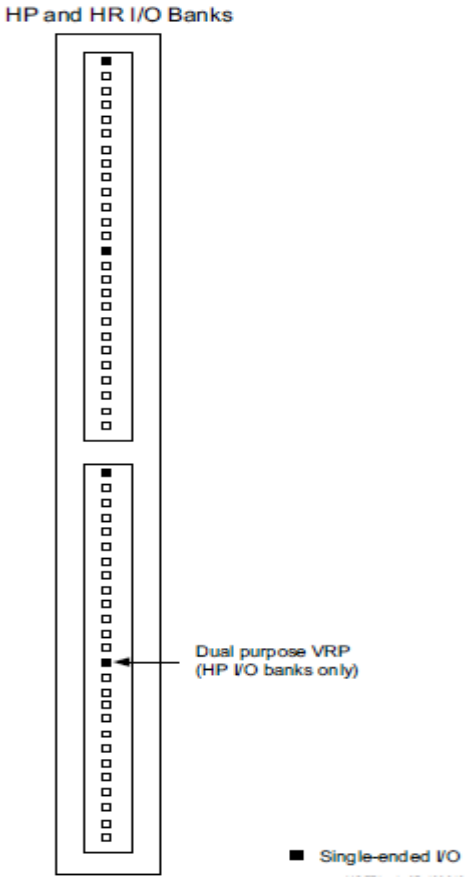
When multiple memory IPs DDR3, DDR4 and QDR-II+ need to be interfaced with FPGA I/O bank utilized by one memory IP during interface cannot be used for interface by other 3 IPs.

For some interfaces there will be unconnected bytes of a bank where not a single I/O pin is used and also there are some pins left un-connected within a byte (interfaced). Earlier these unused I/O pins cannot be used for other purpose. This leads to in-efficient utilization of I/O resources.

Using I/O pin planning rules which allows effective utilization of I/O pins and close dense packing. Now I/O pins which are left unconnected or un-utilized during interface can be used to connect other peripherals. User can interface different Ips in the same bank. Un-connected pins within a byte (utilized) can be used for interface.

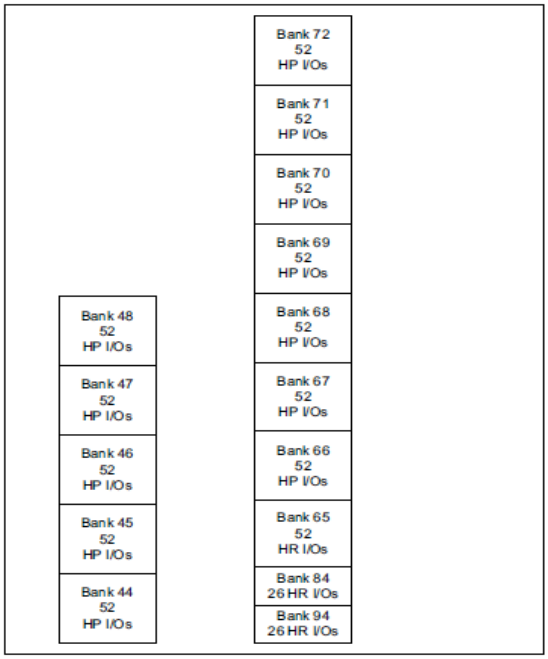
METHODOLOGY

I/O pin planning rules are based on one or more fundamental things of I/O standards. The type of I/O standard to be used for interface depends on electrical characteristics like output drivers and input receivers. FPGA offers both High Performance (HP) and High Range (HR) I/O banks. The HP I/O banks are designed for high-speed memory interfacing and other chip-to-chip interfaces with voltages up to 1.8V. The HR I/O banks are designed to support a wider range of I/O standardswith voltages up to 3.3V.



When a memory IP is interfaced with FPGA I/O standard should be chosen based on voltage levels supported by IP. All I/O pins within a byte will have same voltage standards. When multiple-memory IPs are interfaced, IPs with same I/O standard can share I/O banks.

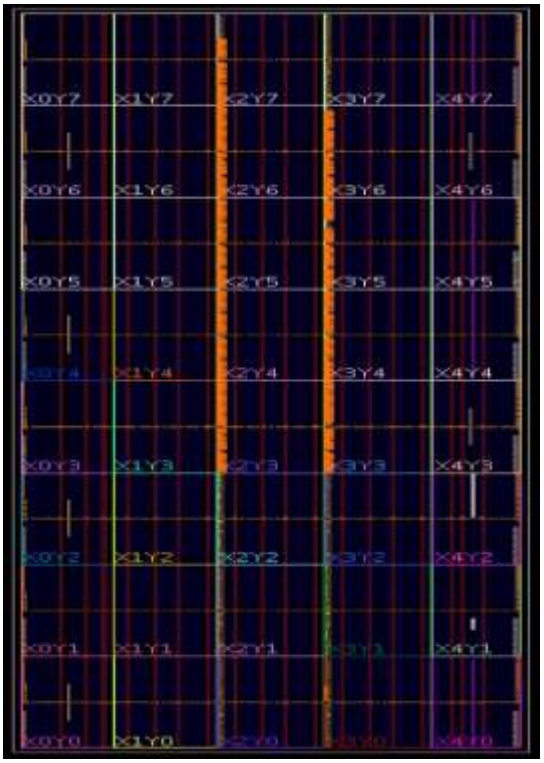
Output standards with the same output requirement can be combined in the same bank.Output standards and cannot be combined within the same I/O bank. Input standards with the same VCCO and VREF requirements can be combined in the same bank.Input standards and output standards with the same VCCO requirement can be combined in the same bank.



Example I/O BANKS

Output standards with different differential standards cannot share an I/O bank. One IP cannot be mixed within another IP interface. Memory IPs with compatible I/O standards should only be used for bank sharing.

FPGA architecture is divided into clock regions. Each clock region consists of I/O BANK, 36 Mb RAM blocks, 1 MMCM, 2 PLL and 1 DSP. Each clock Region is designated with a unique name.System clock pins must be allocated in middle bank to minimize clock skew.



Clock Regions of an FPGA Device

Banks used for Interface should be continuous. Skipping of Bank is not allowed as it results in wastage of I/O pins. Data strobe pins must be associated with their corresponding data byte pins.

Here we have used DDR3 (64 bit), DDR4 (72bit,56bit) and QDR-II+(18 bit) memory IP for interface with FPGA. Normal I/O planning of these four IPs require 6I/O banks for DDR4 and 5 I/O banks for DDR3 and QDR-II+.

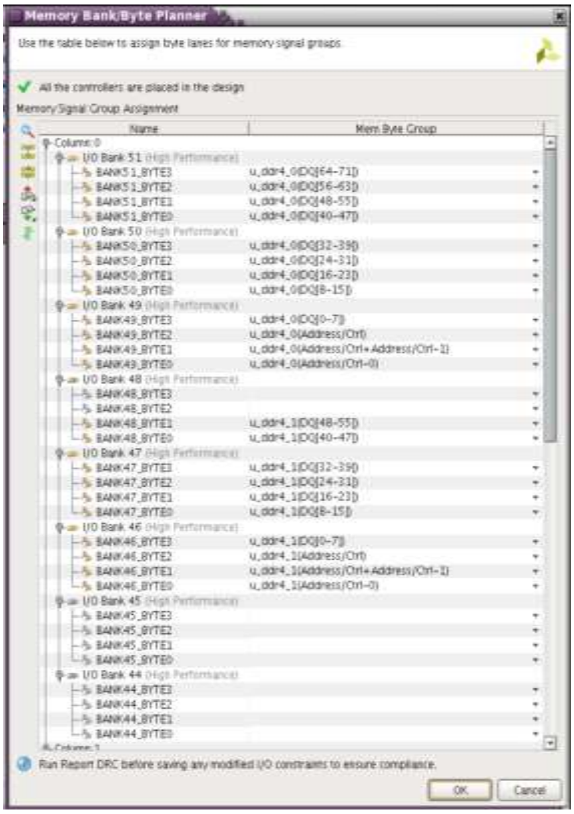
Not all the bytes of a bank(interfaced) are used. after applying I/O BANK sharing rules interface requires 5 and 4 I/O BANKS for two DDR4 and DDR3 with QDR-II+ respectively. The unused bytes of banks (interfaced) are effectively utilized.

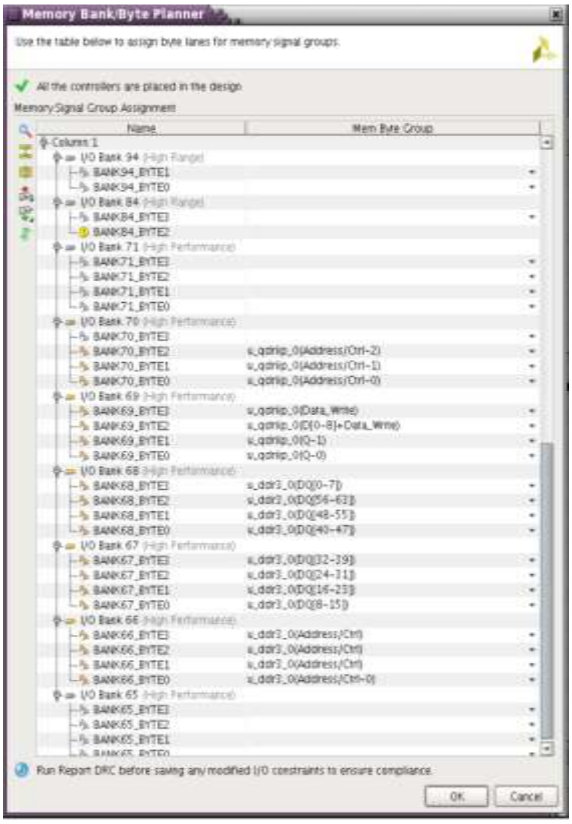
I/O bank sharing resulted in saving of 2 I/O banks i.e. 2*52 I/O pins= 104 pins. This resulted in close or dense packing. Device view shows the difference between the two cases.

ISSN:2278 – 7798
International Journal of Science, Engineering and Technology Research (IJSETR)
Volume 5, Issue 9, September 2016

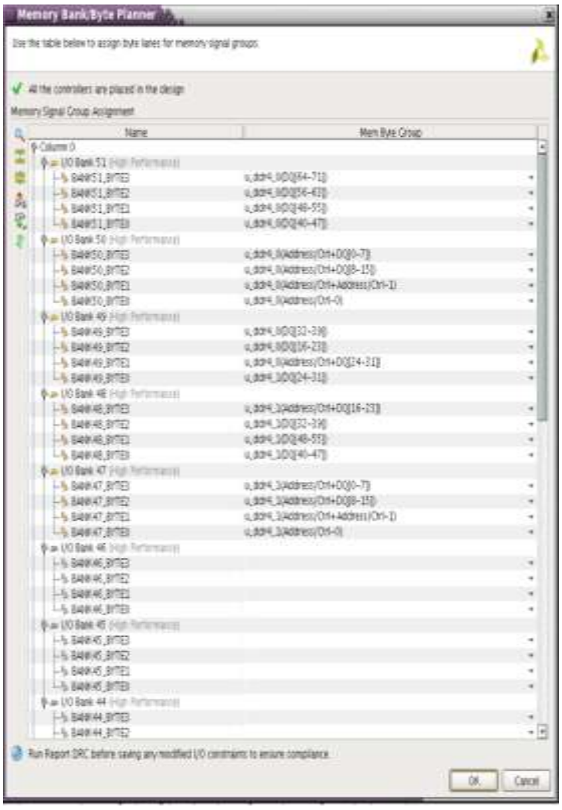
RESULTS

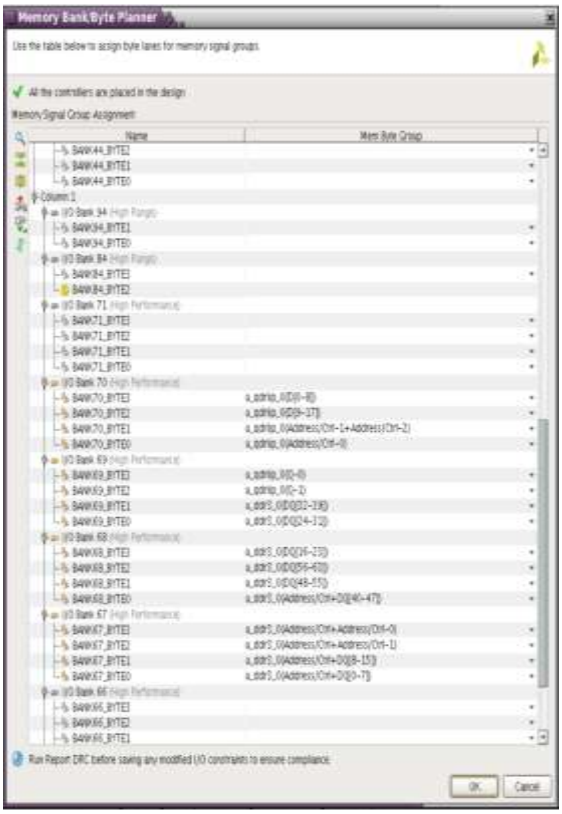
NORMAL I/O PIN PLANNING



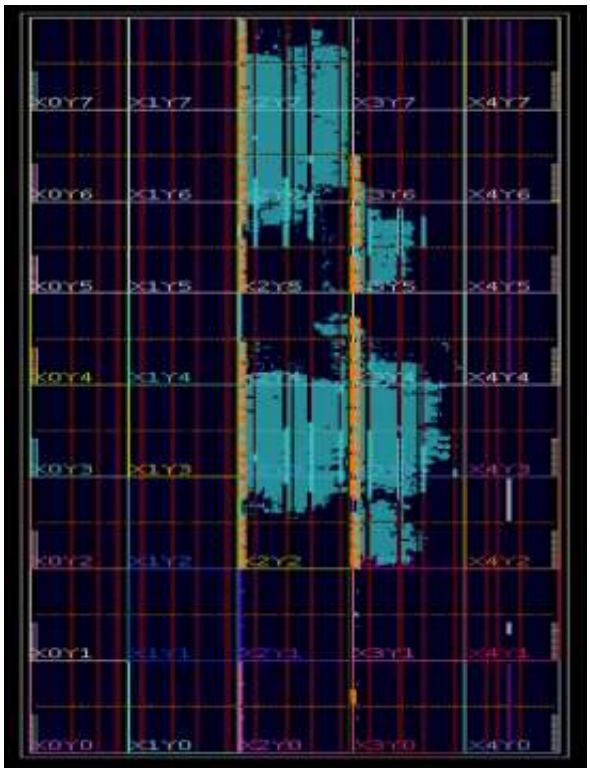


I/O BANK SHARED PIN PLANNING

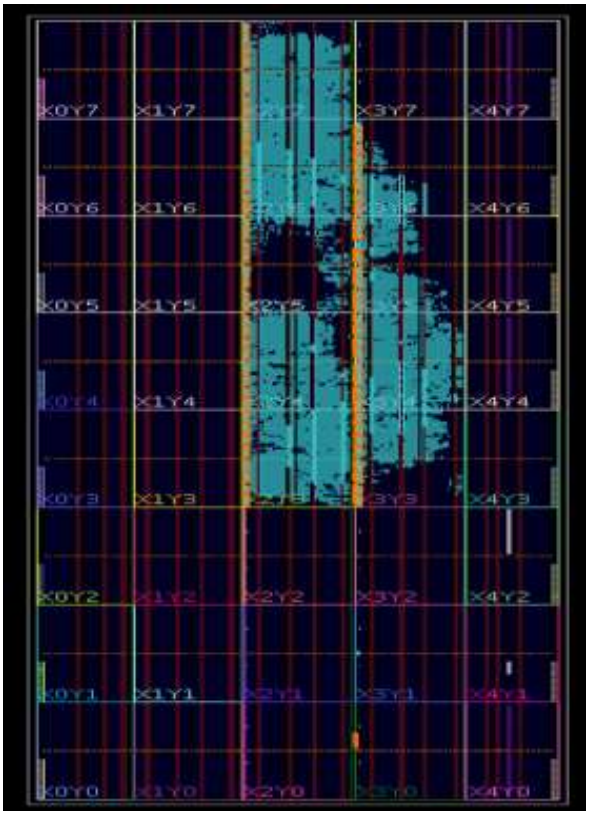




DEVICE VIEW OF NORMAL PLANNING



DEVICE VIEW OF SHARED I/O BANKS PIN PLANNING



CONCLUSION

We have presented I/O BANK sharing rules which are used to optimize I/O count when multiple-memory IPs are interfaced with FPGA. Here we analyzed I/O BANKs utilized for both the methods and compared their closeness in design packing using Device view for both the methods.

REFERENCES

1. www.xilinx.com/support/documentation/data_sheets/ds890-ultrascale-overview.pdf
2. www.xilinx.com/support/documentation/user_guides/ug571-ultrascale-selectio.pdf
3. www.xilinx.com/support/documentation/ip.../mig/v6_0/pg150-ultrascale-mis.pdf
4. www.jedec.org/sites/default/files/docs/JESD79-3E.pdf
5. https://www.micron.com/~/media/documents/products/.../ddr4/4gb_ddr4_sdram.pdf
6. www.samsung.com/global/business/.../file/2011/.../923535ds_k7s32xxt4c_rev13.pdf
7. http://seekdl.org/nm.php?id=172
8. airccse.org/journal/jcsit/0811csit08.pdf
9. https://nwlogic.com/products/docs/DDR4_SDRAM_Controller_Core.pdf
10. http://ieeexplore.ieee.org/document/5702625/?tp=&arnumber=5702625&url=http:%2F%2Fieeexplore.ieee.org%2Fxpls%2Fabs_all.jsp%3Farnumber%3D5702625