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Design of Reverse Converter Hybrid Parallel Prefix Adders Using Majority Gates

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***Abstract*:** In microprocessors and digital signal processing, adders play a major role. Different structures perform the addition operation but the logic differs from each other. Out of these several structures parallel prefix adders are fastest adders. But these parallel prefix adders won't support the reverse converters when these adders are directly implemented. So, the hybrid adders are used in reverse converters and these hybrid adders are structured using parallel adders. HRPX and HMPE structures are designed and simulated in Xilinx with BK and KS adders.

***Keywords* –** Adders,Addition, Parallel prefix, Reverse converters, Hybrid adders.

I.INTRODUCTION

In digital system, binary adders are the most essential elements and are useful in ALU. The main drawback of binary adder is the carry chain. If the width increases the carry chain also increases and the operation of each bit depends on the next preceding bits. Binary adders exhibit logarithmic delay. Parallel prefix adders speed up the carry operation which improves the overall performance of structure.

Wherever fast operation is required, parallel prefix adders are preferred. Residue numbers (RNS) use the residue of the numbers to perform the operation. The RNS mainly consists of forward converters, arithmetic operations and reverse converters.

In RNS an integer is divided into a set of smaller integers which is processed individually and parallel. The forward converter consists of binary to residue conversion and the reverse converter consists of residue to binary conversion. Reverse converter consists of a nonmodular and complex structure. Therefore, more attention should be needed for designing to prevent slow operation. The conversion algorithm and the characteristics of the moduli set have significant effects on the reverse converter performance.

The rest of the paper is organized as follows: section II describes adder structures and types of parallel prefix adders. Section III presents the hybrid adders. Section IV deals with the proposed method followed by results and conclusion in section V and section VI respectively.

II. ADDER STRUCTURES

A basic binary adder circuit can be made from standard AND and Ex-OR gates allowing us to add together two single bit binary numbers. The addition of these two digits produces an output called the SUM of the addition and a second output called the CARRY or Carry-out, (C_{OUT}) bit according to the rules for binary addition. One of the main uses for the binary addition is in arithmetic and counting circuits.

A carry look ahead adder improves speed by reducing the amount of time required to determine carry bits. In ripple carry adder the carry bit is calculated at the time of sum bit and each bit should wait until previous carry is propagated. Whereas the carry-look ahead adder calculates one or more carry bits before the sum and no wait time is required in this adder.

The below diagram shows the structure of parallel prefix adder (PPA). PPA consists of three parts i.e. preprocessing, carry calculation and post processing units.

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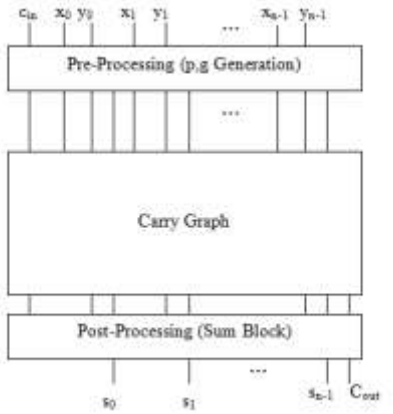


Fig 1 Structure of Parallel Prefix Adder

It is a parallel form of obtaining the carry bit that makes it performs addition arithmetic faster. The pre-processing generates the propogate and generate bits by using the following equations

$$P = a \text{ xor } b$$

$$G = a \text{ and } b$$

The calculated values are passed to next stage i.e. calculation of carries. In this the components are seen in the prefix graph.

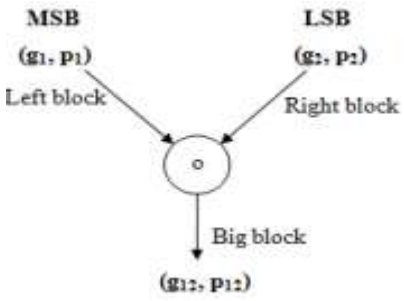


Fig 2 Carry calculation block

$$(g1, p1) \text{ o } (g2, p2) = (g1+g2 \cdot p1, p1 \cdot p2)$$

Whereas g1 and g2 are generate bits and p1 and p2 are propagate bits.

The fundamental carry operator (FCO) consists of associative operator(o) for generate and propagate bits in carry graph. The bits obtained from preprocessing unit are taken by FCO and calculates the operation. This operation contains two AND gates and one OR gate. The arrangement of blocks differs for different PPA adders.

The PPA adders that are used in this are Brent kung (BK) and Kogge Stone (KS) adders.

BK Adder

The operational speed is reduced in these adders by having large number of levels. It has high logic depth with minimum area.

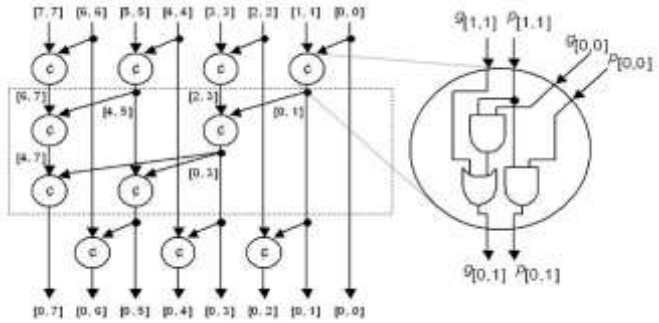


Fig 3 8-bit Brent Kung adder

For BK adder high fanout is required. The dealy required is (2*log2n)-2 and the area required is (2*n)-2-log2n.

KS adder

This adder requires more area than BK adder. In KS adder wiring congestion is problem. As it has low fanout, the performance is increased.

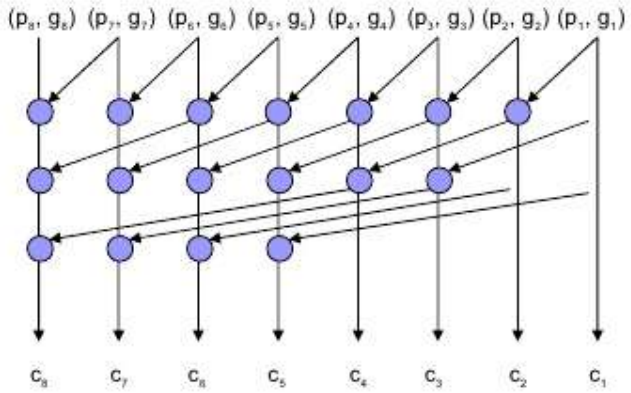


Fig 4 8-bit Kogge Stone adder

Here each vertical stage produces a propagate and generate bit. In the last stage the cumulative generate bits are XORed with initial propagate to produce sum bits.

III. HYBRID ADDERS

Hybrid Regular Parallel Prefix Xor/Or BK Structure

HRPX structure uses a small bit BK adder and binary addition is done in first part and simplified logic with ripple carry adder addition in second part.

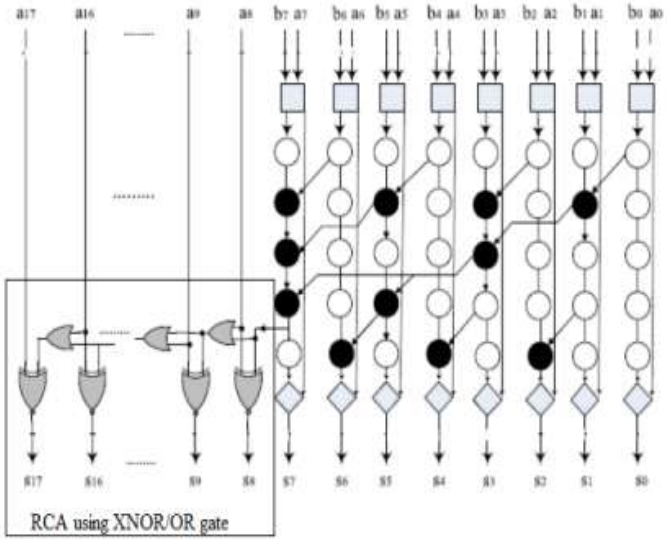


Fig 5 HRPX with BK

Full adders are used in ripple carry addition. But here XOR/OR gates are used instead of full adders. This structure performs the addition operation for (4n+1) bits.

Hybrid Modular Prefix Adder Structure

HRPX structure exhibits high power consumption and consumes more area. So, instead of RCA, excess one unit is used. This circuit consists of two units. 1. Prefix adder 2. Excess one unit.

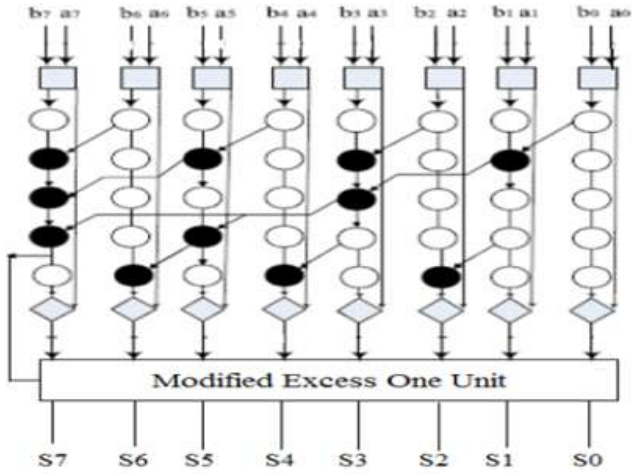


Fig 6 HMPE with BK

The addition obtained from this as follows. The addition operation obtained from prefix adders are forwarded to modified excess unit. The inputs to the modified unit are the outputs of prefix adder and the output of carry calculation stage.

IV. PROPOSED METHOD

The prefix adders which are used in hybrid adders are implemented using majority gates. The functionality and truth table of 3- input majority function are given below.

A	B	C	F
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

F = AB+BC+CA

The symbol for 3-input majority gate is

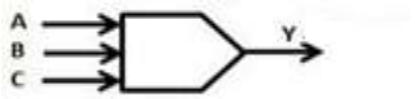


Fig 7 3-bit majority gate

The functionality of majority gates is applied to prefix adders. By using majority gates the power consumption is low and area required is less.

PREFIX ADDERS WITH MAJORITY GATES

The schematic for the BK adder is shown below. Totally it consists of 11 levels. For each level the output is calculated and applied to next levels till the final carried are obtained.

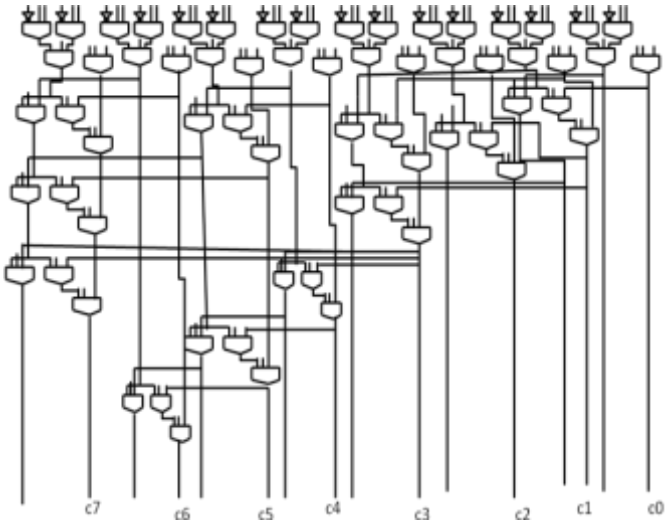
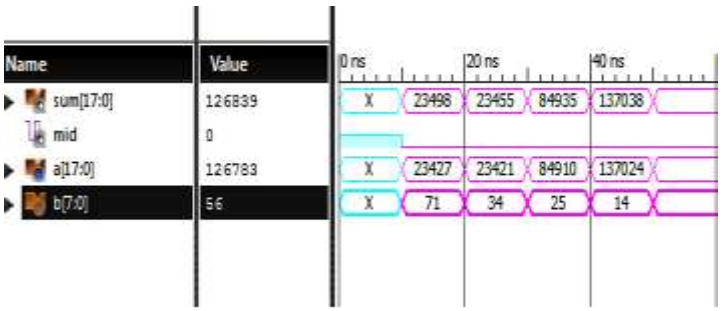


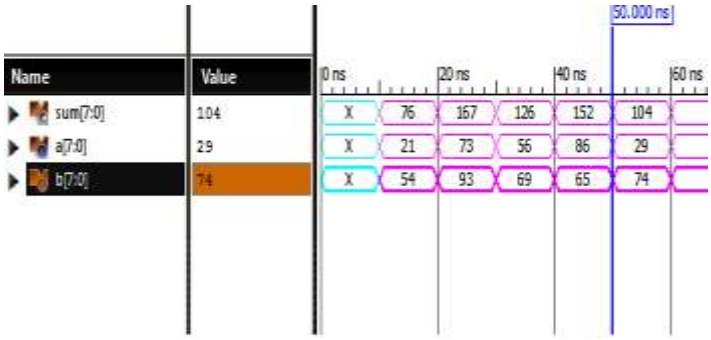
Fig 8 BK adder with majority gates

V.RESULTS

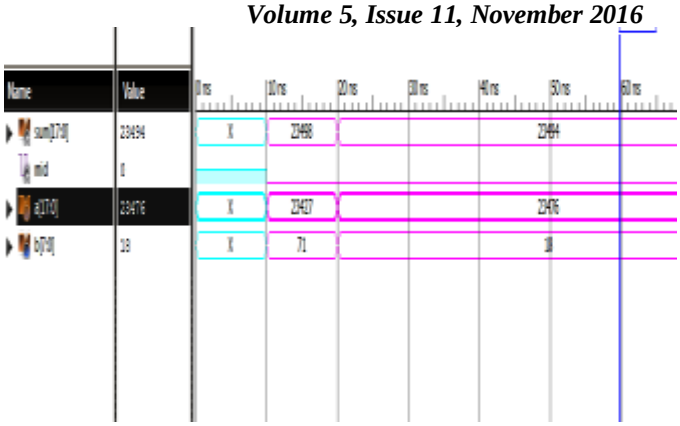
V.1.Simulation Result of HRPX Structure



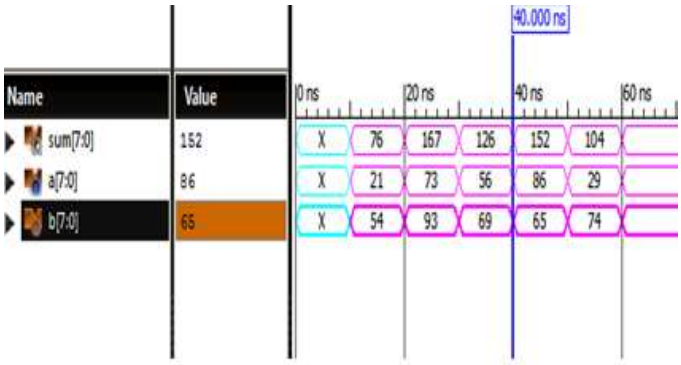
V.2.Simulation Result of HMPE Structure



V.3 Simulation result of HRPX with majority gates



V.4 Simulation result of HMPE with majority gates



VI. CONCLUSION

Hybrid structures HMPE and HRPX are designed using verilog and are simulated using Xilinx 13.4. In order to decrease the power and area, these structures are designed with majority gates.

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