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Design of 3D Mesh Network-On-Chip for a Single cycle Router

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Abstract- Silicon Integrated technologies provides a new opportunity for three-dimensional (3D) Network-on Chip (NoC) design in Systems-on-Chip (SoCs).The communication is through node routers in NoC. The signal delay and power is reduced by decreasing the number of hops. One method is to achieve such goals is to implement efficient router architectures capable of fast packet switching and routing for parallel and scalable Networks-on-Chip (NoC). In order to reduce the wire length in 3D ICs, a single cycle router implementation for 3D mesh NoC with two arbitration schemes is proposed.

***Index Terms*— Network on chip, On-chip communication, integrated circuits, 3D network .**

I. INTRODUCTION

Networks-on-chip (NoC) has emerged as a promising interconnection architecture for multiprocessor system-on-chip (MPSoC) platforms. With scaling of process technology, it has been a reality to integrate multicore and eventually many core on a single chip. The chip multiprocessors (CMPs), which contain tens to hundreds of homogeneous cores on chip, and the multiprocessor system-on-chips (MPSoCs), which are composed of many different types of processors for embedded system, are proposed as the architectures of future microprocessors.

Technology scaling has allowed Systems-on-Chip (SoCs) designs to grow continuously in count of components and complexity. This significantly leads to some very challenging problems, such as power dissipation and resource management. Particularly, the interconnection network starts to play an important role in determining the performance and power of the entire chip . These challenges have led conventional bus-based-systems that are not reliable architectures for SoC, due to lack of scalability and parallelism integration, high latency and power consumption, in addition to their low throughput .

In this sense, three-dimensional (3D) NoCs have emerged to reduce the length and number of global interconnections and the number of hops that packets must pass through, and consequently, decreasing the network latency. This paper introduces OcNoC. The OcNoC's router may be implemented according to two different arbitration models.

This remaining paper is organized as follows. : Section II discusses the architecture of OCNOC. In Section III, we present OcNoC's architecture, emphasizing its differences with respect to a Lasio NoC. Section IV presents the experimental setup elaborated for evaluating OcNoC performance and design characteristics. Section V discusses the simulation results. Lastly, Section VI presents our conclusions and future works.

II. ARCHITECTURE OF OCNOC

NoC structure consists of processing elements (PE), network interfaces (NI), routing nodes and links. The OCNOC router implements the routing algorithm with wormhole switching techniques which reduces the network latency and depth of buffers.

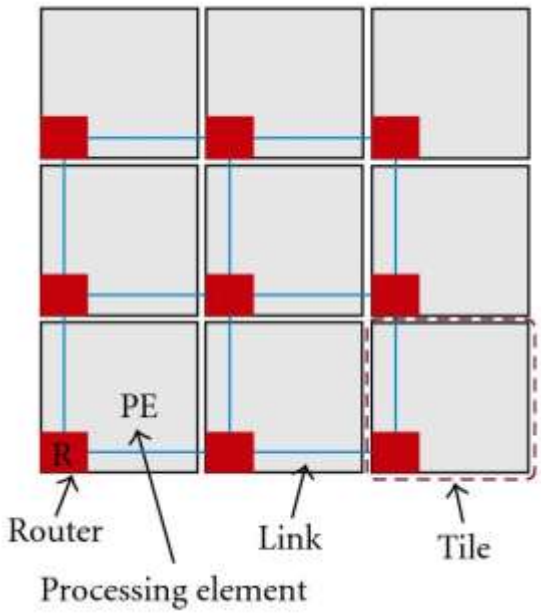


Fig 1: 2D network topology

Routers arbitrate the data between the source and destination PEs through the links. In two layer architecture, a simple packet algorithm can be used as the deterministic XY routing. The 3D network is shown below. The second layer is used for implementing of NoC, while the 1st and 3rd are used for IP

cores. The vertical connections between routers and IP cores are realized through silicon vias(TSV).

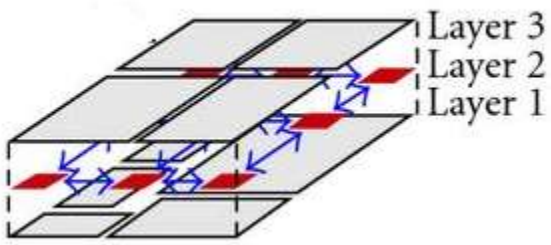


Fig 2: 3D architecture

One advantage of 3D NoC architectures is the 3D fabrication will be simpler compared to 2D architectures. The 3D mesh NoC implements the deterministic XYZ routing algorithm with wormhole technique.

III. ROUTER INTERFACE

The router interface is a full duplex communication which supports bidirectional links. For router interface there are source router and destination router and again these routers have input and output ports respectively.

The input port consists of clockRX, datain, rx and creditout signals.

Similarly the output also consists of clockTX, dataout, creditin and tx signals.

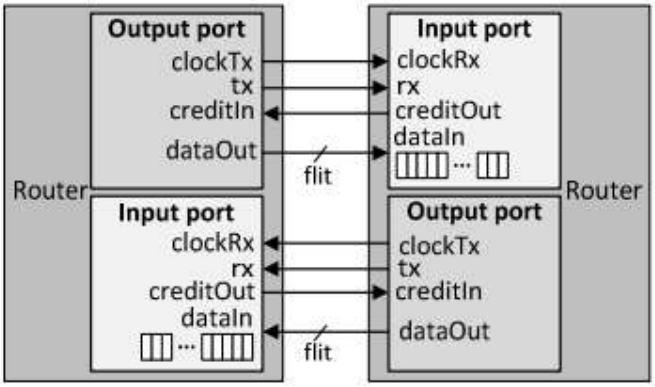


Fig 3: control and data signals

IV. ARBITRATION ALGORITHMS WITH FSM

The arbitration schemes consist of three different schemes.

(i) Round robin priority scheme.

(ii) weighted/dynamic priority scheme.

(iii) Fixed priority scheme.

Round robin scheme is mostly used algorithm in computing in networks. The time slices are divided to each process in equal blocks with circular order, handles all processes same. It is easy to implement, simple and free from starvation.

In dynamic priority algorithm, all devices will have an opportunity that place the request for grant to communicate with other device.

In fixed priority scheme, the processor executes the highest priority task of all the tasks that are ready to execute.

By using the above algorithms, the FSM with four states is presented below.

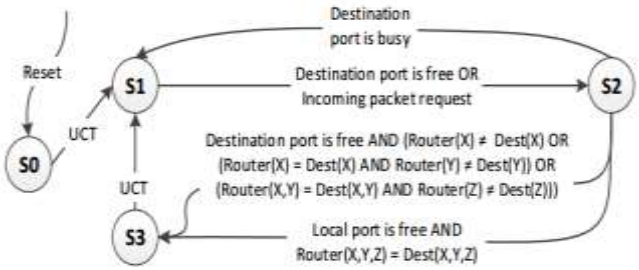


Fig 4: FSM diagram

The four states of router are

S0: This is the initialize state form where the router starts its processes and switches to next stage after a clock cycle.

S1: As the input router sends the packets, this stage waits for the packet to send it to destination port.

S2: Here the packet destination address is verified with routing address. If the destination port is free, then the switching is done and moves to s3 else it moves to s1 for re-switching.

S3: In this stage both the flits delivering and switching process is done by clearing the incoming port. After that it moves to S1 for next switching and requests.

V. DIFFERENT ARBITER APPROACHES

The port availability and pack destination is decided using two approaches.

1. Centralised scheme: Switching requests from input to destination is done using single arbiter. In one cycle the pack is passed to destination if request is granted.

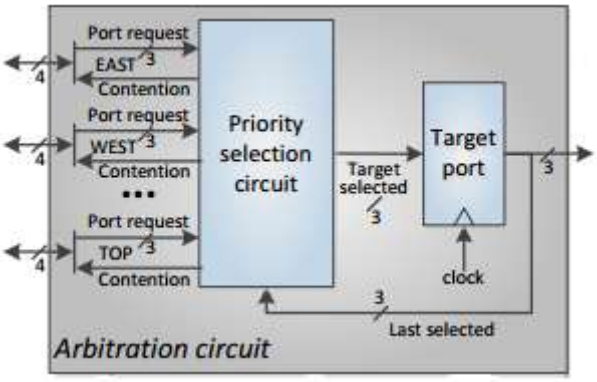


Fig 5: Arbitration circuit

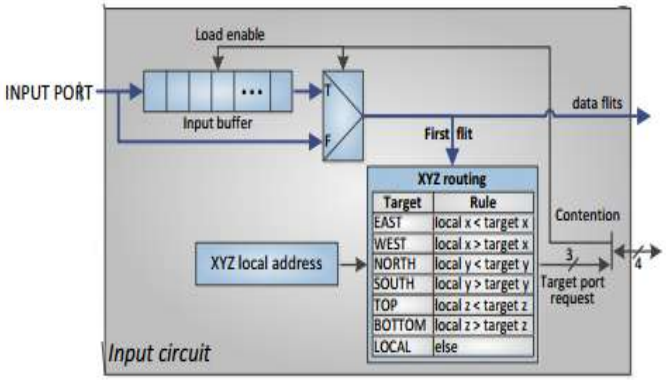


Fig 6: Input control

2. Distributed Scheme:

Distributed scheme is same as centralized scheme, but the switching requests is done by three arbiter circuits based on priority.(i.e. using the arbiter algorithms).

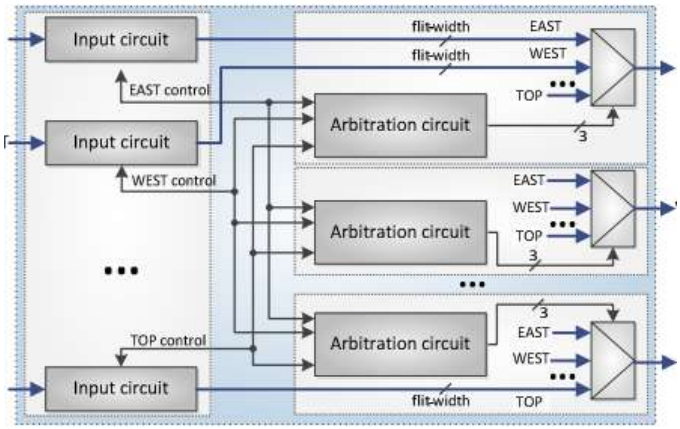


Fig 7: Distributed scheme

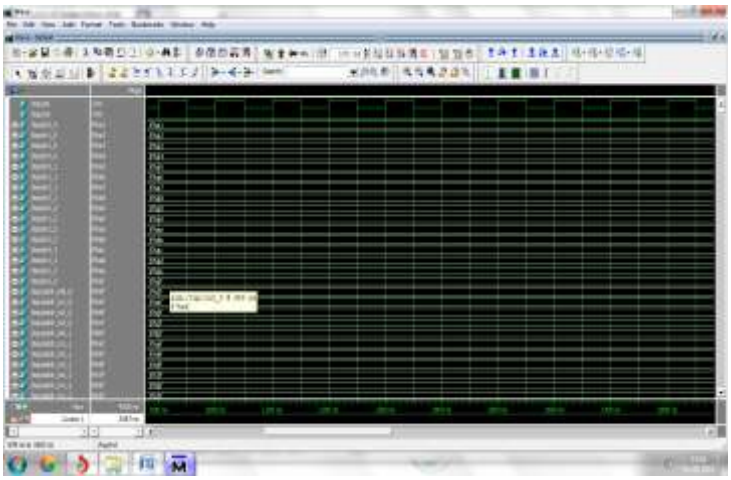
VI. RESULTS

Simulation Result of OCP

Input addr_in 3_2 = 8'h4f;output addr_out 3_3_2 =4'h4f;

Input in 3_3 =8'haf;output out 3_3_2 =8'haf;

Input req_in 3_3 = 1'h1;output req_out 3_3_2 =1'h1;



Schematic View of OCP

VII. CONCLUSION

The on chip NoC is designed using verilog language in Xilinx tool, supports the traffic alternatives in MPSoC applications. By using the circuit-switching approach, combined with dynamic path-setup scheme under a Mesh network topology, the proposed design offers an arbitrary traffic permutation in runtime with compact implementation overhead. By using Circuit Switching technique we can have a dedicated path delay from source Node to Destination Node.

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