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A Review on Design of Parallel Self-Timed Adder

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Abstract—Adders being core building blocks in different VLSI circuits like microprocessors, ALU's etc. performance of adder circuit highly affects the overall capability of the system. In this paper we will present the design and performance of Parallel Self-Timed Adder. It is based on a recursive formulation for performing multibit binary addition. The operation is parallel for those bits that do not need any carry chain propagation. A practical implementation is provided along with a completion detection unit. The implementation is regular and does not have any practical limitations of high fanouts. The proposed work mainly aimed at minimizing the number of transistors and estimation of various parameters viz., area, power, delay for PASTA.
Simulations have been performed using MICROWIND 3.1software and DSCH tool in 45nm CMOS technology that verify the practicality and superiority of the proposed approach over existing asynchronous adders.

Index Terms— Asynchronous circuits, binary adders, CMOS design.

I. INTRODUCTION

Addition is the most common and often used arithmetic operation in microprocessor, digital signal processor, especially digital computers. Also, it serves as a building block for synthesis all other arithmetic operations. Thus performance of any circuit is mainly determined by speed of adder circuit. Circuits may be classified as synchronous or asynchronous. Synchronous circuits are based on clock pulse whereas an asynchronous circuit, or self-timed circuit, is not governed by a clock circuit or global clock instead, they often use signals that indicate completion of operations [1] [6]. Such a system tends to have better noise and electromagnetic compatibility properties than synchronous systems due to the absence of a global clock reference [4]. Asynchronous operation by itself does not imply low power, but often suggests low power opportunities based on the observation that asynchronous circuits consume power only when it is active. The synchronous adders perform slowly due to its incremental nature of operation and therefore it is not recommended for fast and parallel adders. The basic building block of combinational digital adders is a single bit adder. The simplest single bit adder is a half adder (HA). The full adders (FA) are single bit adders with the carry input and output. The full adders are basically made of two half adders in terms of area, interconnection and time complexity .This paper proposes the design of parallel self timed adder (PASTA). The design of PASTA is regular and uses half adders along with multiplexers with minimum interconnection requirement. The interconnection and area requirement is linear which makes it feasible to fabricate in a VLSI chip. The design operates in a parallel manner for those bits that do not require any carry propagation. It is self timed, which means that as soon as the addition is done, it will signal the completion of addition thereby overcoming the clocking limitations.

II. RELATED WORK

1]Jens Sparso et al., **2001** [1] this book aims to introduce us from background in synchronous digital circuit design to the fundamentals of asynchronous circuit design Also it provide the basis to clear need for asynchronous circuits and its performance parameters and their implementation.

2]Ashivani Dubey and Jagdish Nagar et al., **2013** [2] this paper presents the comparison between serial adder and parallel adder. The author compared the serial adder and parallel adder for speed of operation and power consumption parameters. Serial adder consumes low power but are slow as compare to parallel adder. Whereas parallel consume more power as compared to serial adder but as parallel adder add all bit simultaneously they give fast response.

3]N. Weste and D. Harris et al., **2005** [3] this book explains the fundamental theory behind CMOS VLSI Designs. This include brief description of CMOS logic ,CMOS Processing Technology, Circuit Characterization and Performance Estimation , Combinational & Sequential Circuit design, Circuit Simulation and various tools for testing and verification.

4]David Geer et al., **2005** [4] this paper present that Clockless/asynchronous chips offer an advantage over the synchronous counterparts because asynchronous chips have no clock and each circuit powers up only when used, asynchronous processors use less energy than synchronous

chips by providing only the voltage necessary for a particular operation. Clockless chips offer power efficiency, robustness, and reliability.

5]Masashi Imai Takashi Nanya et al., **2008** [5] this paper compared self-timed asynchronous circuits with synchronous circuits in the view point of speed performance and energy dissipation in the future technologies based on the Technology Roadmap of Semiconductors.

6]N. R. Poole et al.,**1994** [6] in this paper Some of the key principles behind self-timed operation are reviewed. Two main architectural styles have been adopted for the design of self-timed processors: time-stationary and data stationary. Both rely on a pipelined approach. The associated technology has the potential to solve a number of problems which are on the horizon, if not yet critical, for large-scale digital systems.

7]Mark A. Franklin and Tienyo Pan et al., **1994** [7] this paper presents performance comparison of asynchronous adders where six adder designs are studied, and their influence on asynchronous system performance are compared. In asynchronous systems, average function delays principally govern overall throughput.

8]Manisha, Archana et al., **2014** [8] in this paper 1-bit CMOS full adder cells are studied using standard static CMOS logic style. The comparison is carried out using several parameters like number of transistors, delay, power dissipation and power delay product (PDP). Different full adders are studied in this paper like Conventional CMOS (C-CMOS), Complementary pass transistor logic (CPL), Double pass transistor logic (DPL), Transmission gate (TGA), Transmission function (TFA), New 14T, Hybrid CMOS, HPSC, Pseudo nMOS, GDI full adders.

9]Akansha Maheshwari, Surbhit Luthra et al., **2015** [9] this paper presents low power full adder circuit implementation using transmission gate. In this paper, the power consumption of a conventional full adder circuit is reduced by using transmission gate at the place of pass transistor logic (NMOS or PMOS). This circuit is designed using 100nm technology parameters.

10]Swaranjeet Singh et al., **2013** [10] in this paper comparative analysis of CMOS transmission gate based adders is presented. Three different types of 4-bit transmission gate based adders namely Ripple Carry Adder, Carry Select Adder and Carry Lookahead Adder are designed. The different adders are compared on basis of no. of transistors, the average power consumption and delay. The simulation results are taken for 180nm technology with the help of Tanner (T-spice) simulation tool.

11]M. Z Rahman, L.Kleeman, and M A.Habib et al., **2014** [11] this paper presents a parallel single-rail self-timed adder. It is based on a recursive formulation for performing multibit binary addition. The operation is parallel for those bits that do not need any carry chain propagation. A practical implementation is provided along with a completion detection unit.

12]P. Choudhury, S. Sahoo, M. Chakraborty et al., **2008** [12] this paper presents hardware architecture to perform the basic arithmetic operation addition using Cellular Automata (CA) and it is possible to perform addition with the help of CA circuits. Each of these circuits is purely combinational in nature and their complexity is centered on the number of logic gates and the associated gate delays.

III. DESIGN OF PASTA

The architecture and theory behind PASTA is presented in this section. The adder first accepts two operands to perform half-additions for each bit. Subsequently, it iterates using earlier generated carry and sums to perform half-additions repeatedly until all carry bits are consumed and settled at zero level.

A] Architecture of PASTA

The general block diagram of the PArallel Self-Timed Adder (PASTA) is presented in Fig.1. Multi bit adders are often constructed from single bit adders using combinational and sequential circuits for asynchronous or synchronous design. The sequential circuits are often serial/chain adders and are not the match for high speed combination adder.

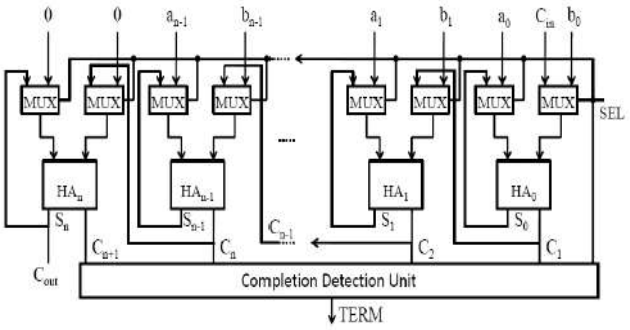

Fig.1: General block diagram of Parallel Self-Timed Adder

B] State Diagrams

In Fig.2, two state diagrams are drawn for the initial phase and the iterative phase of the proposed architecture. Each state is represented by (*Ci*+1 *Si*) pair where *Ci*+1, *Si* represent carry out and sum values, respectively, from the *i*th bit adder block. During the initial phase, the circuit merely works as a combinational HA operating in fundamental mode. It is apparent that due to the use of HAs instead of FAs, state *(*11*)* cannot appear. During the iterative phase (SEL = 1), the feedback path through multiplexer block is activated. The carry transitions (*Ci*) are allowed as many times as needed to complete the recursion.

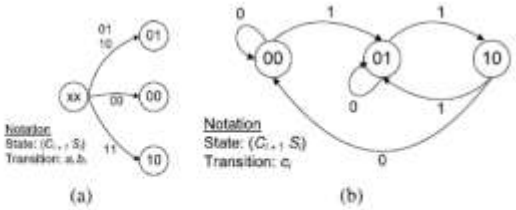

Fig.2 : State diagrams for PASTA. (a) Initial phase. (b) Iterative phase.

C] Proposed Approach

In this paper a Parallel Self-Timed Adder is proposed so as to overcome the drawbacks of existing approaches. The architecture of PASTA which is shown in fig1. consist of three main circuits viz., half adder, multiplexer and completion detection circuits. We have optimized the half adder and multiplexer modules of PASTA so that performance parameters like power, area/size, delay, etc. should be reduce. For this reason we have use a very important and effective technique i.e. transmission gate which gives better result. Transmission gate require lower switching energy and it reduces the count of transistors as compared to conventional CMOS designs. i.e we will design a parallel self-timed adder using CMOS technology for lesser number of transistor count and improved performance parameters.

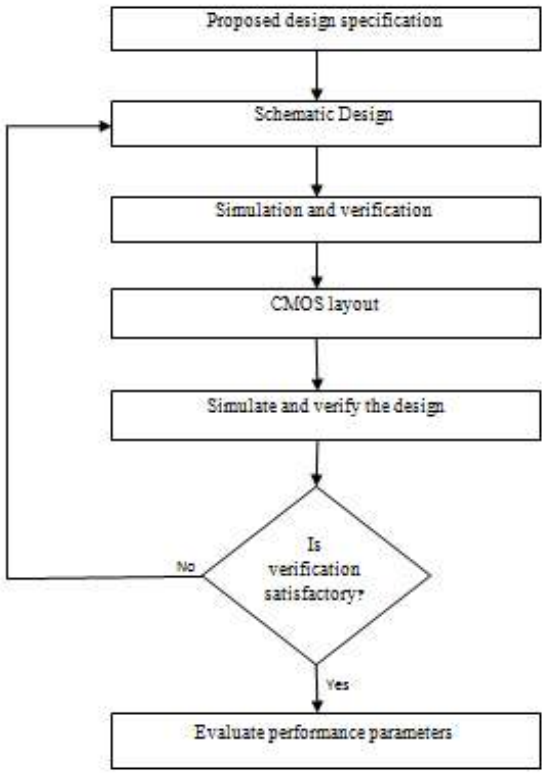

Fig.3:Proposed System Design Flow

Above Fig.3 shows stepwise working of the proposed system. In this model, first we have to define the proposed system design specification. Then we have to design the schematics of PASTA using DSCH tool. This basically include designing of half adder , 2-1MUX and completion detection circuit using conventional CMOS and using optimized approach. The schematics are then simulated and verified. The CMOS layout are then design ,simulated and verified for desired results using MICROWIND3.1tool. If the circuits are correctly verified, performance parameters viz., area, power, delay and maximum frequency are evaluated for proposed approach.

IV. CONCLUSION

In this brief we present the Modified PASTA. The new design using transmission gate and CMOS transistor is proposed and implementation is done using 45nm CMOS technology. With the proposed design, the reduction in number of transistor count is achieved as compared with previous CMOS implementation of PASTA. This achieves a very simple n-bit adder that is area, power consumption wise much more efficient than the previous self timed adder. Moreover, the circuit works in a parallel manner for independent carry chains, and thus achieves logarithmic average time performance over random input values. The completion detection unit for the proposed adder is also practical and efficient. The PASTA is analyzed for various performance parameters. Simulation results are used to verify the advantages of the modified self timed adder.

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