# LOW POWER MULTIPLIERS FOR DCT APPLICATIONS

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***ABSTRACT*: Power, speed and area are prime design constraints of portable electronics devices and signal processing applications. Multiplier plays an important role in DSP applications. Improved column by passing scheme is presented by using low power and high speed multiplier. When operands of the multiplicands are zero to primary power reduction is obtained by disabling the supply voltage of non-functional blocks. By architecture and circuit level modifications is achieved through power reduction. The proposed multiplier consists of new adder architecture for reducing the power consumption and propagation delay. Simulation result is obtained with UMC 90nm and 0.9 V CMOS technology with the cadence specter simulation tool. In proposing multiplier it has been compared by popular multipliers and performance parameters in terms of power dissipation,speed and it is definitely a better choice for low frequency (50 MHz) applications.**

**KEYWORDS**

**Area overhead, Adder, multiplier, Delay, Low power, switching transitions**

## I INTRODUCTION

It is a very challenging problem for the hardware designers to develop low power, high speed and area efficient portable electronic design. Mobile phones, smart cards such as hearing aids and PDAs are the example of portable consumer electronic products. It is the main concern for operating hours of the battery and residing in it but also greater computational capacity.

At the circuit level voltage scaling, threshold voltage, Transistor sizing, network restructuring power down strategies and logic style are used to achieve low power. In addition to this, this technique also contributes to the reduction of propagation delay and area occupancy as well. Digital Signal Processors (DSPs) are used to perform the most common operations such as video processing, filtering and fast flourier transform (FFT). Such modules perform an extensive sequence of multiply and accumulate computations. Multiplication is the most fundamental operation of digital computer systems and digital signal processors.

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A large number of transistors with high switching transitions is used to perform a variety of multiplication operations. In 64 point radix-4 pipelined FFT processor the multiplier consumes 30% power and also occupies 46% chip area. Multiplier is most critical, power hungry arithmetic unit that requires more area and Computational time. Array based multipliers consumes low power as compared to Wallace tree multipliers.

In order to improve the performance in tree based multiplier the additional hardware is required, but at the cost of increased layout and parasitic. On the other side, array multiplier has smaller and regular layout. Therefore, array multiplier is a better choice due to its optimized with lesser hardware as small area leads to less switching transitions. An Adder is the fundamental unit of the multiplier and it has significant impact on the overall performance of the system for power dissipation, delay and area occupancy. In this paper, array multiplier is proposed to achieve low power and high speed multiplication operation.

## II LITERATURE REVIEW

The following section consists of several Low power multiplier designs with improved Column By passing scheme of operation.

### A.THE MERGING ARCHITECTURE

The following section consists of several Low power multiplier designs with improved Column By passing scheme of operation. The 4:2 compressors inputs are fed by accumulated data bit .The multiplication circuit bits in accumulation operation are merged and it will save the cost of the additional accumulator. By increasing overall speed in MAC operation and result is obtained. Feeding the bits of the accumulated operand into the summation tree accumulation operation is implemented and it is based on the advantage of the three input lines of the available 4:2 compressor for 8-bit MAC unit architecture and to insert the bit Z7 determines the number of modified 4:2 compressors.

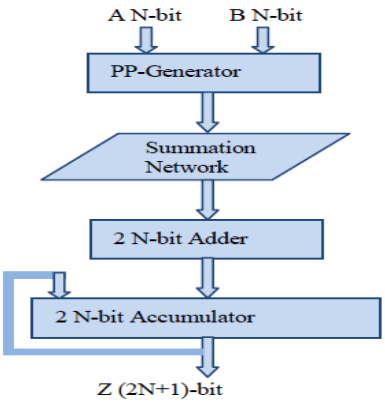


**Fig .1 Flow chart**

A MAC unit of 8th bit has design comprises in two pressure stages. To suit the additional piece is to embed to eighth segment bits in square "A" stage and utilize for changed 4:2 compressor in this area. Adjusted 4:2 compressor utilized will produce an extra complete piece that should be bolstered to the following segment and it's required for extra changed 4:2 compressor and ninth segment of the principal arrange, also have an additional carry out.

## B. COLUMN BYPASSING FIXED-WIDTH ARRAY MULTIPLIER

Settled Width Exhibit Multiplier and Power dissipation, it can be presented by S. Balamurugan and P. S. Mallick .It can be separated into dynamic and static power dissemination in numerous DSP or other related applications can be lessened. The dynamic power utilization overwhelms the aggregate power utilization furthermore the best method for diminishing element control utilization and exchanging movement is decreased.

The changed full adder cell by passing logic to diminish this exchanging action. The relating line and segment of adders is not initiated when if the information bit coefficient is zero in multiplier plan. In the multiplicand operand, it contain more zeros and higher power decrease can be accomplished utilizing segment by passing multiplier and the multiplier operand contains a bigger number of zeros than higher power lessening can be accomplished utilizing column by passing multiplier.

For a settled width exhibit multiplier outline with a CBA cell for an unsigned and also marked numbers. In this approach, the comparing bit in the multiplicand is zero for the operation segment can be impaired. Accomplishing the sidestep rationale the viper cell comprises of two tri-state cushions and one multiplexer. Consider the incomplete item bit ai.bj if the estimation of is "0" Then the operations comparing corner to corner can be impaired in operation and every one of the yields are known.

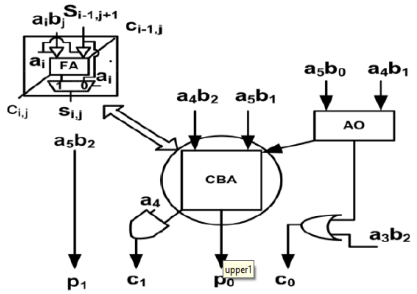


**Fig.2 column bypassing fixed-width array multiplier**

## C. BOUNDS ON SIGNAL TRANSITION ACTIVITY:

In this section, the main results of this paper, namely expected number of transitions for lower and upper bounds. If the process is stationary and argotic the bounds are asymptotically achievable. Asymptotically achieves the bounds in Coding algorithm .

So as to determine limits on move action, Lemmas 1 and 2 displayed beneath. Lemma 1 limits given and Lemma 2 utilizes Lemma 1 to bound the normal number of ones for an arrangement of bits with a specific entropy rate. Hypothesis 1 utilizes and Lemma 2 to bound the quantity of moves per image of a procedure with a specific entropy rate given that every image is coded utilizing a normal number of bits.

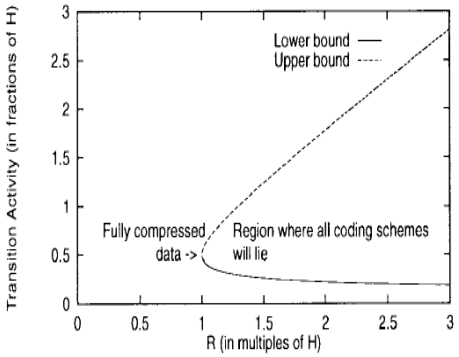


**Fig.3 Transition Activity Graph**

## D. MULTIPLIER DESGIN

New ASIC configuration is presented by Shilling Lu, Xi Huang, Li Cui and it is created to propose a changed Shannon viper based multiplier. We have outlined and investigated for convey spare snake (CSA) multiplier circuit utilizing in light of Shannon's adder cell. The marked element size is 20µm and comparing supply voltage is 5v .The convey spares multiplier is a straight exhibit increased and it spreads information down through the cluster cell. It adds one extra fractional item to the incomplete aggregate for every column of CSA. In the operand estimate builds, the straight exhibit develops at a rate equivalent to the square of the operand measure on the grounds that the quantity of lines in the cluster is equivalent.

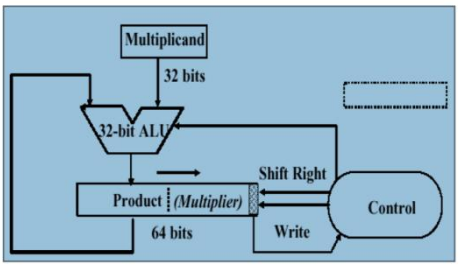


**Fig.4 Shift and add multiplier**

## E. COMPRESSOR DESIGN

Ming-Chen Wen, Sying-Jyan Wang, and Yen-Nan Lin is created by the additional parasitic postpone originates from the NMOS/PMOS stacks are tended to. The enhanced 3:2 compressor that eases the parasitic postponement of a similar flag .The proposed compressor utilizes a 2:1 multiplexer to choose amend aggregate flag. At the point when all data sources are consistent low (A=0,B=0, and C=0), the flag way is NOR3+IMUX21. Correspondingly, when the information sources are all coherent high (A=1, B=1, andC=1), the flag way is NAN3 +IMUX21. For whatever remains of the info blends, the flag ways are CL(Carry Rationale) + IMUX21.

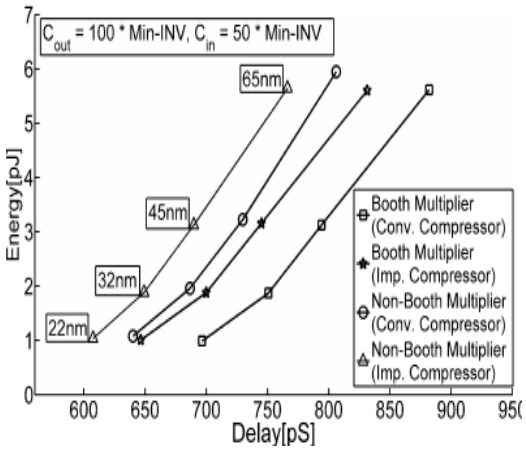


**Fig.5 Multiplier Graph**

The postpone estimation is done utilizing the logical defer display. For vitality estimation, spatially and transiently uncorrelated data sources are action is utilized to gauge the vitality utilization of every outline under the presumption of absolutely irregular information vectors. The normal exchanging movement of 25% is gotten after correlation of assessed and H-spice comes about. Absolutely irregular info vectors are utilized as a part of H-spice vitality reproductions.

The entryway measuring is an iterative methodology and it is completed in MATLAB. The sizes of passages are streamlined under working conditions (deferment and data/yield stacking). Each multiplier is stacked with 100*Min-INV and deferment are upgraded for an information capacitance that is cleared from 20*Min-INV to 100*Min-INV. At that point, insignificant vitality enhancement calculation is utilized to estimate the doors for negligible vitality at the postpone targets got from defer advancement vitality and postpone space of 16x16-piece multipliers with the p/n proportion of 2.0 at 65nm CMOS innovation.

**TABLE 1 COMPARISON OF LITERATURE REVIEW**

| Ref. No | METHODOLOGY | PROS | CONS |
|---|---|---|---|
| [1] | Soft sensor in the process industry | It is efficient and very easily. | No spatial information used. |
| [2] | Peer to peer architecture | Derived by trying to assess early In the design process. | It will occur reputation effect. |
| [3] | Binary arithmetic in the computing system | High speed digital computers in the arithmetic operation. | Small increases in the complexity |
| [4] | Energy delay analysis of partial product reduction methods | It making the number of partial Product into half of multiplier. | Decreases of power consumption, delay circuit. |
| [5] | Low power parallel multipliers | It keeps up the first exhibit structure without presenting additional limit cells | low power design comes from mobile applications. |

## CONCLUSION

A low power, high speed proposed multiplier architecture with improved column by passing scheme has been presenting this work. A new adder with optimized hardware is also proposed. The architecture of this adder reduced the power consumption and propagation delay, when ICBS is not in use. Simulation results show that the proposed multiplier architecture facilitates reduction of switching transitions and leakage power. It is also found better in terms of area occupancy and propagation delay. While testing, the input test pattern is taken randomly with an equal occurrence probability of zero's and one's. Power can be saved more in the proposed multiplier, if the input test pattern has more no. of zero's than the no. of one's is achieved.

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