Research Trends in Area Optimized FIR filter Implementation on FPGA

Sejal D. Patel
Department of Instrumentation & Control Engineering
L.D. College of Engineering
Ahmedabad

Prof. M.C. Patel
Assistant Professor
Department of Instrumentation & Control Engineering
L.D. College of Engineering
Ahmedabad

***Abstract* – Now a day, optimization Of Area of FIR filter is one of the Challenging Task and growing fields in the area of Very Large Scale Integrated Circuits (VLSI). As we know that for getting desired frequency response of filter order of filter increase so ultimately more memory (Area) required to implement FIR filter on VLSI chip. This paper deals with the Literature survey of design and implementation of FIR filters in which MAC operation of FIR filter is replaced by DA (Distributed Arithmetic) algorithm that use LUT that is part of FPGA. The evaluation of area and speed for different types of Modified DA given for FIR filter has been proposed. The performance analysis of different method in terms of speed, area, power consumption and hardware requirements.**

Keywords – FIR Filter, MAC operation, DA algorithm, Area, Speed

I. INTRODUCTION

Digital filtering is one of the most versatile tools of DSP.As advantage over the analog filter that it consist of error associated with passive component such as temperature, drift etc. In addition, the characteristics of a digital filter can be easily changed under software Control. So, they are widely used in adaptive filtering applications in communications such as echo cancellation in modems, noise cancellation, and Speech recognition. Digital filter are basically characterized by two types that is Finite Impulse Response (FIR) and Infinite Impulse Response (IIR). There are lots of advantage such as linearity and stability are most basic property of FIR filter that is popular over IIR filter.[11] But one drawback of FIR filter is that for getting desired frequency response means narrow transition width as we know that this width is inversely proportional to order of filter so achieving this criteria order of filter is higher and ultimately it required more Area for implementation on embedded platform. So in many application we require phase linearity such as speech recognition then it must to use FIR filter and keep in mind area constraint. If phase linearity is not issue then it is better recommended to use IIR filter because it achieve desired frequency response with less order so no area optimization issue.

As there is challenging task to implement FIR filter on embedded platform with area constraint. There are lots of research technique available for implementing FIR filter on embedded platform. Most of research are available on Field Programming Gate Array (FPGA). The advantages of the FPGA approach to digital filter implementation include higher sampling rates than are available from traditional DSP chips, lower costs than an ASIC for moderate volume applications, and more flexibility than the alternate approaches. In particular, multiple multiply-accumulate (MAC) units may be implemented on a single FPGA, which provides comparable performance to general-purpose architectures which have a single MAC unit. The design of FIR Filter involves multipliers and adders (MAC) which consumes an efficient technique for calculation of sum of products or vector dot product or inner product or multiply and accumulate (MAC) MAC operation is very common in all Digital Signal Processing Algorithms. Distributed Arithmetic was first brought up by Croisier , and was extended to cover the signed data system by Liu , and then was introduced into FPGA design to save MAC blocks with the development of FPGA technology.[10][13].

This paper is organized as follows. Section II presents Basic DA algorithm Section III presents study of different modified DA algorithm for FIR filter implement as Area optimized. Section IV presents conclusion.

II. BASIC DA ALGORITHM

If the length of the impulse response is finite, the filter is an FIR (finite impulse response) filter. Otherwise, the filter is an IIR (infinite impulse response) filter.For a FIR filter of order *N*, each value of the output sequence is a weighted sum of the most recent input values: [2]

Y[n]$= \sum_{i=0}^{N} h_i . x[n-i]$ ………(1)

Where X[n] = input signal Y[n]= output signal. Where h[n] is the filter coefficient and x[n] is the input sequence to be processed. The FIR structure consists of a series of

Multiplication and addition units, and consume N MAC blocks of FPGA, which are expensive in high speed system. Compared with traditional direct arithmetic, Distributed Arithmetic can save considerable hardware resources through using LUT to take the place of MAC units [2]. Another virtue of this method is that it can avoid system speed decrease with the increase of the input data bit width or the filter coefficient bit width, which can occur in traditional direct method and consume considerable hardware resources [2].

Distributed Arithmetic is introduced into the design of FIR filters as follows.

In the two's complement system, x[n] can be described as:

$$x[n] = -2^B\, x_B[n] + \sum_{b=0}^{B-1} 2^b x_b[n] \ldots (2)$$

Substitute this eq (2) in eq(1)

$$y[n] = -2^B x_B[n]h[n] + \sum_{b=0}^{B-1} h[n] \sum_{n=0}^{N-1} 2^b x_b[n] .. (3)$$

Final Form of Distributed arithmetic is :

$$y[n] = -2^B x_B[n]h[n] + \sum_{b=0}^{B-1} 2^b \sum_{n=0}^{N-1} h[n]x_b[n] .. (4)$$

Now as observing right part of equation (4) we can store the possible combination of h[n] and every bit of input signal x[n] that is indicated as xb[n] is stored to LUT unit and call out relevant data according to input to save MAC blocks[10] And then the weighted sum of is calculated through shift

Registers. In signed system, the signed bit should be taken into consideration so is also added. As a result, the final form of Distributed Arithmetic is define as equ. (4) And the implementation as shown in Fig 1[2] can be achieved on FPGA through LUT units.

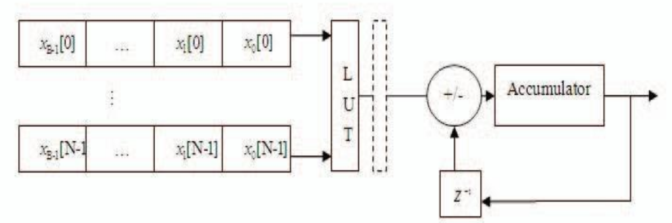

Fig: 1 DA basic structure

So according to combination of different input signal and filter coefficient value precalculated sum stored to LUT and depending upon combination of different input signal value is fetched and passed to accumulator until all bit are processed.

III DIFFERENT MODIFIED DA ALGORITHM

Basic DA structure is used to increase the resource usage while pipeline structure is used to increase the system speed. Now when we use DA that replace the MAC by LUT but when order of filter is higher then required LUT size is increased so cost and more time to look up the table and more memory to store the values so LUT is divided in to small more LUT to solve this problem [2].so because of pipeline structure increase the system speed but due to pipeline structure increase the time delay. Due to this type of arrangement there is 50% save hardware resources. Basic Divided LUT concept is shown in Fig 2[2].It is shown in Fig 2 that is insert the register in middle parts to increase the system speed.

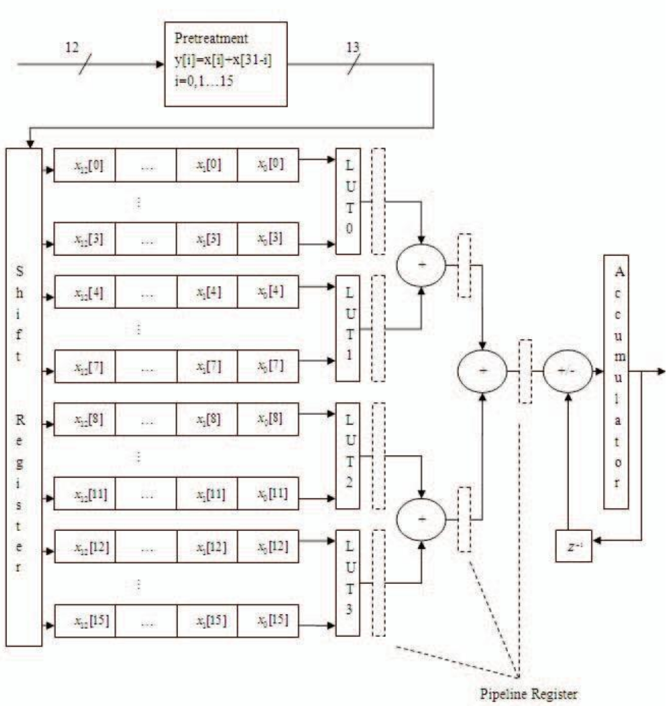

Fig 2 LUT divided architecture

Another approach is also used to cure from major disadvantage of DA that expontial growth of LUT as filter order increase that LUT size is independent of input variable because the LUT contents are not precalculated before implementing the design, instead the only needed location contents are calculated while processing the input data [4]. Two main block used in this approach that is carry look ahead adder (CLA) and tri state buffer. Only needed location are calculated whereas basic DA technique if the location content is zero it will fetched and added to partial sum whereas on-line LUT no add operation when it is zero so that directly effect on execution time. On-line DA-LUT is show in Fig 3[4]

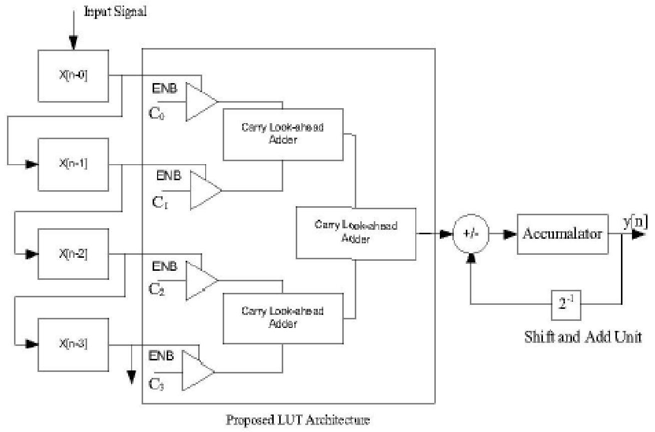

Fig 3: On-line DA-LUT architecture

As CLA and RCA both get good result in terms of area saving but CLA is much better when number of bit increses.so this concept can easily used to implement high order FIR filter with different coefficient word length without suffering from large LUT construction[4]. As we know there are lots of application where we require adaptive FIR filter in which filter coefficient are not fixed so in such type of filter implementation also DA is popular. So if replace shift accumulation block of DA by carry save accumulation(CSA) block then reduced significant critical path[1].so this concept throughput is increased by parallel LUT update and CSA help to reduce the area complexity. Power consumption can be reduced by fast bit clock to CSA and slower clock to other. For fourth order adaptive filter implement using this modified DA as shown in Fig 4.[1]

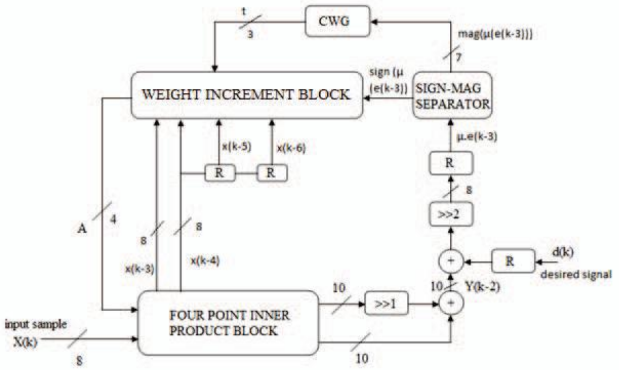

Fig 4: Block diagram of DA technique used for adaptive filter

As shown in fig 4 theThe magnitude and sign values are separated from the SIGN-MAG block. The magnitude of the computed error is decoded to generate the control word *t* for the barrel shifter. The weight-increment unit consists of barrel shifters and adder/subtractor cells. The barrel shifter shifts the different input values *xk* for $k = 0, 1, . . ., N - 1$ by appropriate number of locations. The barrel shifter yields the desired increments to be added with or subtracted from the current weights. The sign bit of the error is used as the control for adder/subtractor cells such that, when sign bit is zero or one, the barrel-shifter output is respectively added with or subtracted from the content of the corresponding current value in the weight register.so using this approach there is significant reduction in Area Delay Product(ADP).

We know that discrete wavelet transform (DWT) used for time-frequency analysis. In DWT there are two basic parts that is low pass filter (LPF) and High pass filter (HPF).when LPF or HPF is implemented on FPGA using DA technique then there is significant reduction in area compare to conventional multiplier architecture (CMA) [6].One limitation is reduction in speed because of DSP48ES are replaced by LUT so when speed is no matter then this low cost approach is best [6].

Building adaptive DA filters requires recalculating the LUTs for each adaptation which can negate any performance advantages of DA filtering. To implement DA based LMS adaptive filter using the DA architecture that updates each weight individually and then regenerates the DA-F-LUT using the new weights, will be computationally expensive and time consuming, causing significant reduction in the filter throughput.so one approach is use auxiliary LUT with special addressing for fast updating of DA base adaptive filter [5].Fig 5 indicate this approach [5].

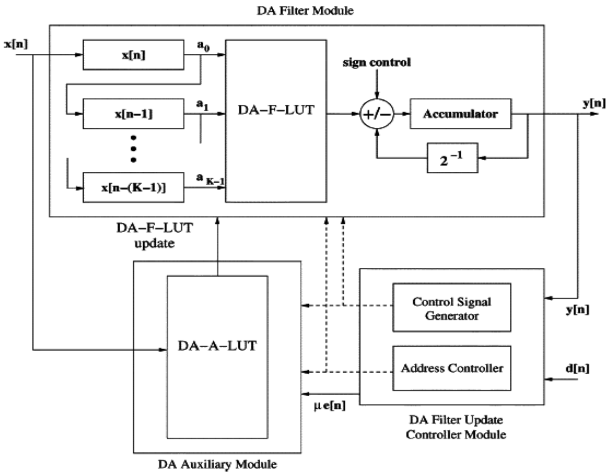

Fig 5 DAAF sructure

The DA filter module in Fig. 5 performs the filtering operation on the incoming data samples with the current values of the weights using the DA-F-LUT. In addition to the DA filter module that implements the filtering operation, the proposed DAAF structure consists of a DA auxiliary module. The DA filter update controller module generates the addresses and control signals for updating the DA-A-LUT and subsequently, the DA-F-LUT. Hence the throughput of DADF remains almost constant regardless of filter size K.Compare the number of logic elements used in MAC based and DA based adaptive filers.MAC based adaptive filters has larger number of logic elements.The DAAF is approximately twice as area efficient as the MACAF[5].

FIR filter structure is based on slicing of LUT. m slice are taken for K-tap filter, so as to form m smaller units ,each of with k-tap DA base units(K=m*k).Hence total memory requirement of for K-tap FIR filter drastically reduced from 2^K to $(m*2^k)$ memory elements with additional (m-1) adder[7].

DA algorithm greatly reduced logic resource by replacing MAC operation by LUTs but as seen earlier that LUT size increases exponentially as order of filter increase so as shown in [8] size of LUT reduced to half due to fact that right half of LUT is mirror version of left half of LUT,but with reversed sign[8].

IV. CONCLUSION

MAC operation is common for implementing FIR filter. But due to its implementation require more Area and more challenging task is when implement on FPGA because of limited resources in it. Where DA algorithm is efficient technique for implementing FIR filter on FPGA. In DA algorithm Main issue regarding to growth of LUT size as order of filter increases so using different modification done in DA algorithm get advantage over MAC operation in terms of Area. Time delay is also issued in basic DA because of Accumulator So by using Parallel structure of DA we will get balance structure of FIR filter in terms of Area and time delay.

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