One bit Full adder design in Sub threshold region with low Power Delay Product (PDP)

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***Abstract*— In this paper, we designed one bit full adder with ultra-low power, high speed logic family, that is DMTGDI logic. The entire design is implemented under sub threshold region. This logic family is implemented based on the advantages of both Gate Diffusion Input (GDI) and Dual Mode Logic (DML). Simulations have been performed on a single bit full adder and compared with other sub threshold logic families. In this work, it is proved that a single bit full adder can be implemented with very less number of transistors using GDI compared to the previous work. And DMTGDI takes less number of transistors compared to conventional CMOS logic and shows better performance improvement over conventional DML, and significant reduction of power-delay product (PDP) in Static and Dynamic modes. The schematic is implemented in Mentor Graphics tool and results of these logic families are compared. This shows that the DMTGDI is having better performance characteristics over conventional sub threshold logic families.**

***Index Terms*— Gate Diffusion Input (GDI), Sub threshold, Dual Mode Logic (DML), DMTGDI.**

I. INTRODUCTION

Nowadays, all electronics appliances working under low power consumption. To achieve low power, instead of using components working under threshold region, its better to use sub threshold devices. Sub threshold device means, the logic functions will be implemented below threshold voltage. Because of this minimum energy point can be achieved [1]. The voltage ranges varies between 300mV to 500mV. But, with this type of subthreshold circuits there are some issues that depends on the power limitations when compared with devices work above threshold region. Among these power limitations, the important limitation is the performance that is affected by supply voltage. Hence the performance should be improved for subthreshold [9] circuits to meet the requirements of the market. For this purpose, several logic families have been introduced and compared.

II. GDI AND TGDI LOGIC FAMILIES

One of the low power logic family is Gate Diffusion Input(GDI) logic which consists of only two transistors and has the ability to implement a wide range of two input logic functions [7], with less power consumption and higher speed compared to the standard CMOS or pass transistor logics.

The Fig.1 shows the basic GDI cell and Table.1shows how various logical functions can be derived from the basic GDI cell. The main advantage of the GDI cell over normal CMOS is, only two transistors are enough to implement some logic gates such as Inverter, AND, OR, MUX, XOR and XNOR in addition to two other functions as shown.

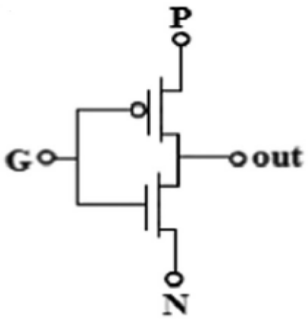

Fig 1. Basic GDI cell

N	P	G	OUTPUT	FUNCTION
0	1	A	A'	INVERTER
0	B	A	A'B	F1
B	1	A	A'+B	F2
1	B	A	A+B	OR
B	0	A	AB	AND
C	B	A	A'B+AC	MUX
B'	B	A	A'B+B'A	XOR
B	B'	A	AB+A'B'	XNOR

Table 1. Functions of GDI Logic

In GDI logic output swing is reduced for some input combinations. Therefore, additional buffer stage is required to solve this issue which in turn increases power consumption. To overcome this limitation, the circuit is modified by taking transmission gates in place of single pass transistors. We can say it is an enhanced version of GDI logic family. This logic is known as Transmission Gate Diffusion Input (TGDI) [1]. Here, the reduction of output voltage swing has been fixed without additional buffer stage.

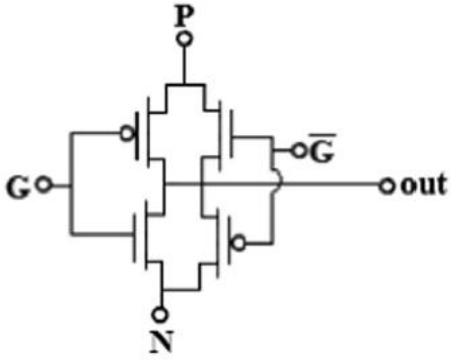

Fig 2. TGDI logic cell

As the GDI logic consists of only two transistors, the switching speed may be reduced during charging and discharging modes due to the existence of capacitor. This problem can be avoided in case of TGDI, as it is implemented with pass transistor logic. The comparison of power and delay and power delay product are shown in Table.2 for AND, OR and MUX logics. The delay means the average delay which can be calculated as the critical path delay, the is the highest path in the total logic circuit. Both logic families have been simulated with same size in 130nm CMOS technology in sub threshold region with supply voltage [1] of 300mV and 500mV. It can be observed from this table that delay of TGDI logic is lower than GDI. But the TGDI requires double the transistors in comparison with GDI logic, which requires more area and power consumption. This means that power and delay of TGDI should be compared with the average of GDI gates. It is shown that the delay of TGDI is reduced compared to the GDI logic as shown in Table 2.

LOGIC FUNCTION	SUPPLY VOLTAGE (V_{DD})	GDI				TGDI			
		POWER (mW)	DELAY (ps)	PDP(pJ)	#Tr	POWER (mW)	DELAY(ps)	PDP(pJ)	#Tr
AND	0.3v	0.128	487.15	0.0624	2	64.585	25.363	1.638	4
	0.5v	0.113	485.27	0.0549	2	63.486	67.492	4.284	4
OR	0.3v	643.05	327.21	210.4	2	965.54	67.486	65	4
	0.5v	583.75	302.31	176	2	901.06	49.13	44.2	4
MUX	0.3v	642.75	391.93	251	2	900.76	391.75	352.8	4
	0.5v	583.51	372.15	217	2	837.28	371.87	311.3	4

Table. 2. PDP of GDI and TGDI

III. Dual Mode Logic (DML)

Another type of Sub threshold logic family is Dual Mode Logic (DML) which can be operated in static and dynamic modes [4]. DML logic is designed with an additional transistor M1 is connected at the output of static CMOS logic. But due to this, the logic requires more number of transistors when going of higher realizations.

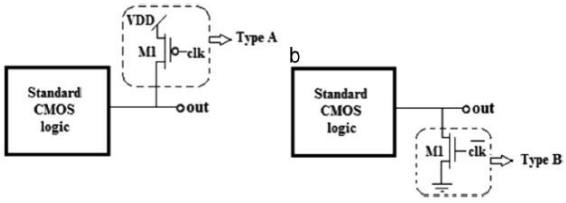

Fig. 3. DML structure

This logic family consumes very less power (proved experimentally) and shows high performance. The basic idea of DML structure is shown in Fig.3. Based on the structure of DML, it can be operated in two types namely Type-A and Type-B. Each type is having static and dynamic modes of operation. In DML, the additional transistor connected at the output will come in parallel with the pull up transistors in Type-A mode and it will be in parallel with pull down transistors in Type-B. As the number of transistors increased in DML, the size of transistors are also considered as an important factor as in the case of CMOS logic [6].

In static mode, the clock is applied with a constant input that's why the name static). For clk= V_{DD}, the transistor M1 goes off DML will look like a CMOS logic with an extra parasitic capacitance of M1 transistor. In dynamic mode of operation, the clock is not constant and which varies between two logic values 0 and 1 continuously for a specific period, so the clock is an asymmetric clock. When the clock is logic 1, the DML acts in pre-charge mode and when the clock is logic 0, the DML acts in evaluation phases [1].

The following table shows the comparison of DML logic families for Type-A and Type-B in static and Dynamic modes of operation for both 300mV and 500mV.

LOGIC FUNCTION	SUPPLY VOLTAGE (V_{DD})	DML Static(Type A/ Type B)				DML Dynamic(Type A/ Type B)			
		POWER (nW)	DELAY (ps)	PDP (aJ)	#Tr	POWER (nW)	DELAY (ps)	PDP (aJ)	#Tr
AND	0.3V	1.8919/ 2.0491	0.049/ 0.049	94/ 10	7	5.5963/ 3.7278	96.410/ 445.98	0.539/ 1.66	7
	0.5V	3.9947/ 4.3028	115.85/ 125.87	0.462/ 0.541	7	100.09/ 6.6611	22.396/ 429.44	2.24/ 28	7
OR	0.3V	1.9938/ 2.2186	0.087/ 0.087	174/ 194	7	2.5744/ 7.7697	9.3766/ 445.76	0.23/ 3.46	7
	0.5V	4.0348/ 4.4156	238.06/ 248.58	0.96/ 0.097	7	4.2843/ 0.012	165.50/ 0.05	0.708/ 60700	7
MUX	0.3V	2.1605/ 2.4106	0.046/ 0.047	101/ 113	15	4.0857/ 25.768	0.047/ 0.046	192/ 1200	15
	0.5V	5.1220/ 5.4131	153.20/ 160.87	0.784/ 0.87	15	76.945/ 0.0112	210.22/ 0.049	16.1/ 55600	15

Table 3. PDP of DML static and Dynamic

IV. Dual Mode TGDI Logic

Next, we propose to use TGDI as a basis for a new dual mode logic family called "Dual Mode TGDI logic" or DMTGDI logic[1]. Finally, performance and power consumption of conventional DML, GDI and TGDI has been investigated and compared to DMTGDI logic for implementation of a single bit full adder block.

By replacing static CMOS circuit with TGDI in DML structure DMTGDI logic is obtained as shown in Fig. 4. Using this structure, one may implement wide range of logical functions with few transistors in the unit cell. Therefore, it would be reasonable to expect that power consumption and delay would be less than conventional DML.

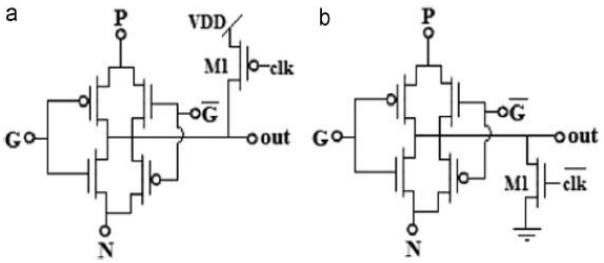

Fig. 4. DMTGDI logic cell a) Type-A, b) Type-B

V. Proposed Work

In this work, one bit full adder is designed in all the stated logic families like GDI, TGDI, DML and DMTGDI. The average power and delays are measured and compared with each other.

Generally, the full adder is designed with two XOR gates, two AND gates and one OR gate. But due to this, the area is increased. So, to reduce area the full adder can be designed with two XOR gates and one multiplexer only.

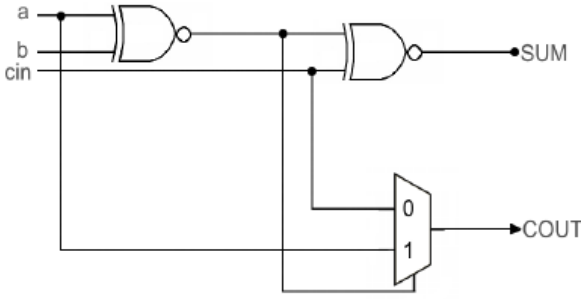

Fig.5. Full adder circuit

As shown in the figure, the full adder can be realized with three logic gates. The proposed structure is developed with the help of basic cell GDI which means each logic function takes only two transistors. Hence, as shown in fig.6, for basic GDI design the full adder needs only 10 transistors.

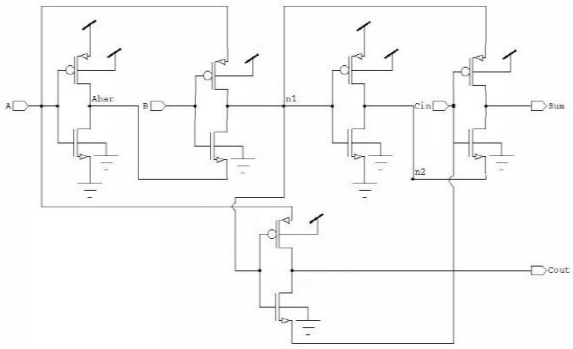

Fig. 6. Full adder using GDI

The TGDI logic is implemented to avoid the limitation in GDI, and which needs 28 number transistors. But though the number of transistors increases, the output voltage swing can be achieved greatly. The same full adder is also implemented using Dual Mode Logic in static and dynamic modes.

To achieve less power consumption, less delay and very less area, here we combine all these logic families and introduced a new logic family DMTGDI. The proposed one bit full adder design using DMTGDI logic is done with less number of transistors. The comparison table also shown to compare the results of various subthreshold logic families for both 300mV and 500mV.

Full adder for VDD= 300mV	POWER (nW)	DELAY (ns)	PDP (aJ)	#Tr
GDI	5.14	35.87	180.4	10
TGDI	4.3165	60.86	262.7	28
DML (Static)	5.98	0.047	28.64	28
DML (Dynamic)	5.356	0.047	25.5	28
DMTGDI (Static)	4.3165	59.948	258.7	35
DMTGDI (Dynamic)	4.3167	29.749	128.4	35

Table 4. performance comparison of logic families for 300mV

VI. Simulation Results and Conclusion

A single bit full adder which demonstrated in Fig. 7, has been implemented in conventional DML, GDI, TGDI and DMTGDI logics. These circuits have been used for simulation and comparison of performance, power consumption and area of logic families.

Full adder for VDD= 500mV	POWER (nW)	DELAY (ns)	PDP (aJ)	#Tr
GDI	4.67	26.49	123.6	10
TGDI	4.0028	25.82	103.3	28
DML (Static)	12.22	49.906	66	28
DML (Dynamic)	2.26	209.54	47.3	28
DMTGDI (Static)	4.0028	27.382	109.6	35
DMTGDI (Dynamic)	4.0031	270.43	108.2	35

Table 5. Performance comparison of logic families for 500mV

The Schematic diagram of proposed full adder in DMTGDI logic is shown in Fig. 7. The DMTGDI logic required 35 transistors for full adder implementation. The critical path delay and power consumption are shown in Table 5. And power delay products (PDP) of different logics are compared in Table 5. The Fig. 8 shown the performance characteristics of various logic families compared each other. In these simulations supply voltage has been varied between 300mV to 500mV for power measurements. Here, the performance comparison is done for all logic families for 300mV, which leads to a conclusion that the proposed family DMTGDI gives very less delay and moderate power consumption. Hence the Power Delay Product (PDP) of DMTGDI, in Dynamic mode of operation, is also very less compared to all other families. And it is also observed that the DMTGDI logic performance in Static mode is similar to the performance of TGDI logic family as shown in Fig 8., because in static mode the clk is constant which makes the M1 transistor OFF in Type-A and ON in Type-B topology.

Hence finally the one bit full adder is designed with cascade of Type-A and Type-B topologies to achieve better performance. The area of the transistor is also reduced to 19.5nm^2.

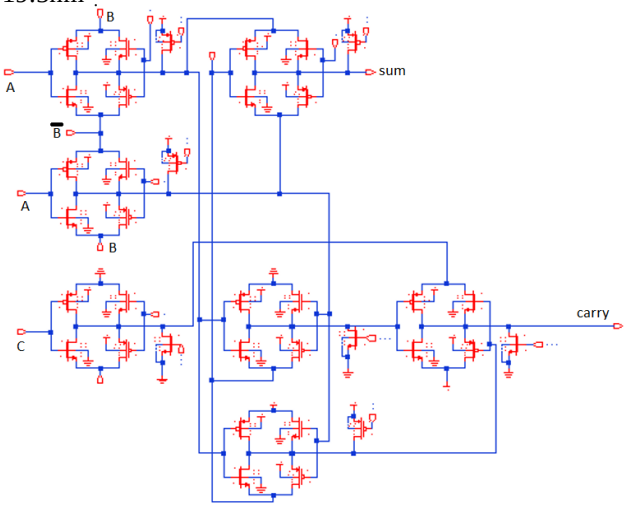

Fig. 7. DMTGDI Full Adder

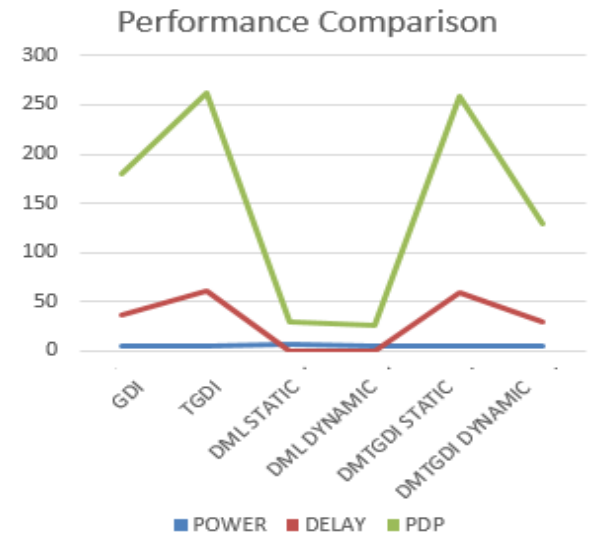

Fig. 8. Performance comparison of various logic families for 300mV

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